2-Stage Operational Amplifier Design

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1 Requirements

Schematic and Specification

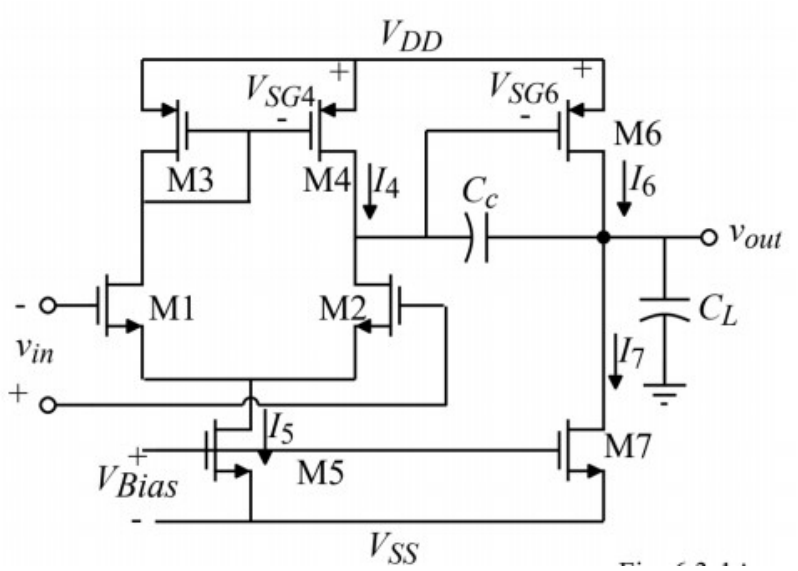


Figure 1: Two-stage CMOS Op-Amp schematic with compensation capacitor C_c and load capacitor C_L.

As shown in Fig. 1, the circuit consists of input transistors M_1, M_2, current mirror load M_3, M_4, biasing transistor M_5, output stage M_6, and current sink M_7.

Assume the channel length is to be $0.5\,\mu m$, load capacitor is $C_L = 10\,\text{pF}$.

$$A_v > 3000\,\text{V/V} \qquad V_{DD} = 0.9\,\text{V},\ V_{SS} = -0.9\,\text{V}$$
$$GB = 10\,\text{MHz} \qquad SR > 12\,\text{V}/\mu s$$
$$\text{Phase margin} = 60^\circ \qquad -0.5\,\text{V} < V_{out} < 0.5\,\text{V}$$
$$ICMR = -0.5\,\text{V to } 0.5\,\text{V} \qquad P_{diss} \leq 3\,\text{mW}$$

2 Calculate Kn, Kp from library 180nm

$$V_{TN} = 0.393; \quad V_{TP} = -0.4; \quad \lambda_N = 0.07; \quad \lambda_P = 0.07$$

$$K_n = \mu_n \times C_{ox} = 280.575\,\mathrm{cm}^2/\mathrm{Vs} \times \left(\frac{\varepsilon_{ox}}{T_{ox}}\right)$$

$$C_{ox} = \frac{3.9 \times 8.854 \times 10^{-12}}{4.1 \times 10^{-9}}\,\mathrm{F/m}^2$$

$$\Rightarrow C_{ox} = 8.422 \times 10^{-3}\,\mathrm{F/m}^2 = 0.8422\,\mu\mathrm{As}/V(\mathrm{cm})^2$$

$$\Rightarrow K_n = 280.575\,\mathrm{cm}^2/\mathrm{Vs} \times 0.8422\,\mu\mathrm{As}/V(\mathrm{cm})^2 = 236.3\,\mu A/V^2$$

$$K_p = \mu_p \times C_{ox} = 116.169\,\mathrm{cm}^2/\mathrm{Vs} \times \left(\frac{\varepsilon_{ox}}{T_{ox}}\right)$$

$$\Rightarrow K_p = 116.169\,\mathrm{cm}^2/\mathrm{Vs} \times 0.8422\,\mu\mathrm{As}/V(\mathrm{cm})^2 = 97.837\,\mu A/V^2$$

3 Transistor Sizing Calculations

3.1 Calculation W1, W2

$$g_{m1} = GB \times C_c \times 2\pi = 10\,\mathrm{MHz} \times 5\,\mathrm{pF} \times 2\pi = \mathbf{314}\,\mu\mathbf{S}$$

$$\Rightarrow \frac{W_1}{L_1} = \frac{(g_{m1})^2}{2K_n I_D} = \frac{(314\,\mu S)^2}{236.3\,\mu A/V^2 \times 60\,\mu A \times 1.5} = 6.954$$

$$\Rightarrow W_1 = W_2 = 6.954 \times 0.5\,\mu m = \boxed{3.477\,\mu m}$$

3.2 Calculation W3, W4

- With L of PMOS and NMOS are 0.5 µm

$$C_c > 0.22C_L = 0.22 \times 10\,\mathrm{pF} = 2.2\,\mathrm{pF} \Rightarrow \text{Choose } C_c = \mathbf{5}\,\mathrm{pF}$$

$$I_S = SR \times C_c = 12 \times 10^6 \times 5 \times 10^{-12} = \mathbf{60}\,\mu\mathbf{A}$$

$$\frac{W_3}{L_3} = \frac{I_S}{K_p(V_{DD} - V_{CM(\min)} - |V_{T3}|)^2} = \frac{60\,\mu A}{97.837\,\mu A/V^2 \times (0.9 - 0.5 - 0.4 + 0.393)^2} = 3.97$$

$$\Rightarrow W_3 = W_4 = 3.97 \times 0.5\,\mu m = \boxed{1.985\,\mu m}$$

3.3 Calculation W5

$$V_{DSS} = V_{CM(\min)} - \left(\sqrt{\frac{I_5}{K_n(W_1/L_1)}} - V_{T1}\right) - V_{SS}$$

$$= -0.5 - \left(\sqrt{\frac{60\,\mu A}{236.3\,\mu A/V^2 \times 6.954}} - 0.393\right) + 0.9 = -0.18480\,V$$

$$\Rightarrow \frac{W_5}{L_5} = \frac{2I_5}{K_n(V_{DS5})^2} = \frac{2 \times 60\,\mu A}{236.3\,\mu A/V^2 \times (-0.18480)^2} = 14.986$$

$$\Rightarrow W_5 = 14.986 \times 0.5\,\mu m = \boxed{7.493\,\mu m}$$

3.4 Calculation W6

$$\text{Phase margin} = 60^\circ \Rightarrow g_{m6} = 10 g_{m1} = 10 \times 314\,\mu S = 3140\,\mu S$$

$$g_{m4} = \sqrt{2K_p(W_4/L_4)I_4}, \quad I_4 = 0.5 I_S$$

$$\Rightarrow g_{m4} = \sqrt{2 \times 97.837\,\mu A/V^2 \times 3.97 \times 60\,\mu A} = 152.66\,\mu S$$

$$\frac{W_6}{L_6} = \frac{W_4}{L_4} \times \frac{g_{m6}}{g_{m4}} = 3.97 \times \frac{3140\,\mu S}{152.66\,\mu S} = 81.66$$

$$\Rightarrow W_6 = 81.66 \times 0.5\,\mu m = \boxed{40.83\,\mu m}$$

3.5 Calculation W7, Power Dissipation and Voltage Gain

$$I_6 = \frac{(g_{m6})^2}{2K_p(W_6/L_6)} = \frac{(3140\,\mu S)^2}{2 \times 97.837\,\mu A/V^2 \times 81.66} = 617\,\mu A$$

Choose $I_C = 315\,\mu A$ **, reduce** I_6 **to increase** A_v

$$P_{diss} = (V_{DD} + |V_{SS}|)(I_5 + I_6) = 1.8 \times (60\,\mu A + 315\,\mu A) = 0.675\,mW < 3\,mW$$

$$A_v = \frac{2 g_{m1} g_{m6}}{I_5((\lambda_2 + \lambda_6)(\lambda_6 + \lambda_7))} = \frac{2 \times 314\,\mu S \times 3140\,\mu S}{0.12 \times 315\,\mu A \times 60\,\mu A} = \boxed{5323\,\text{V/V}}$$

4 Calculate V_{bias}, $V_{\text{out(max)}}$, and $V_{\text{out(min)}}$

$$I_{SS} = 0.5K_n \left(\frac{W_5}{L_5}\right) (|V_{GSS}| - V_{TN})^2$$

$$\Rightarrow 60\,\mu A = 0.5 \times 236.3\,\mu A/V^2 \times 14.986 \times (|-0.9 - V_{\text{bias}} - 0.393|)^2$$

$$|-0.9 - V_{\text{bias}}| = 0.577\,V$$

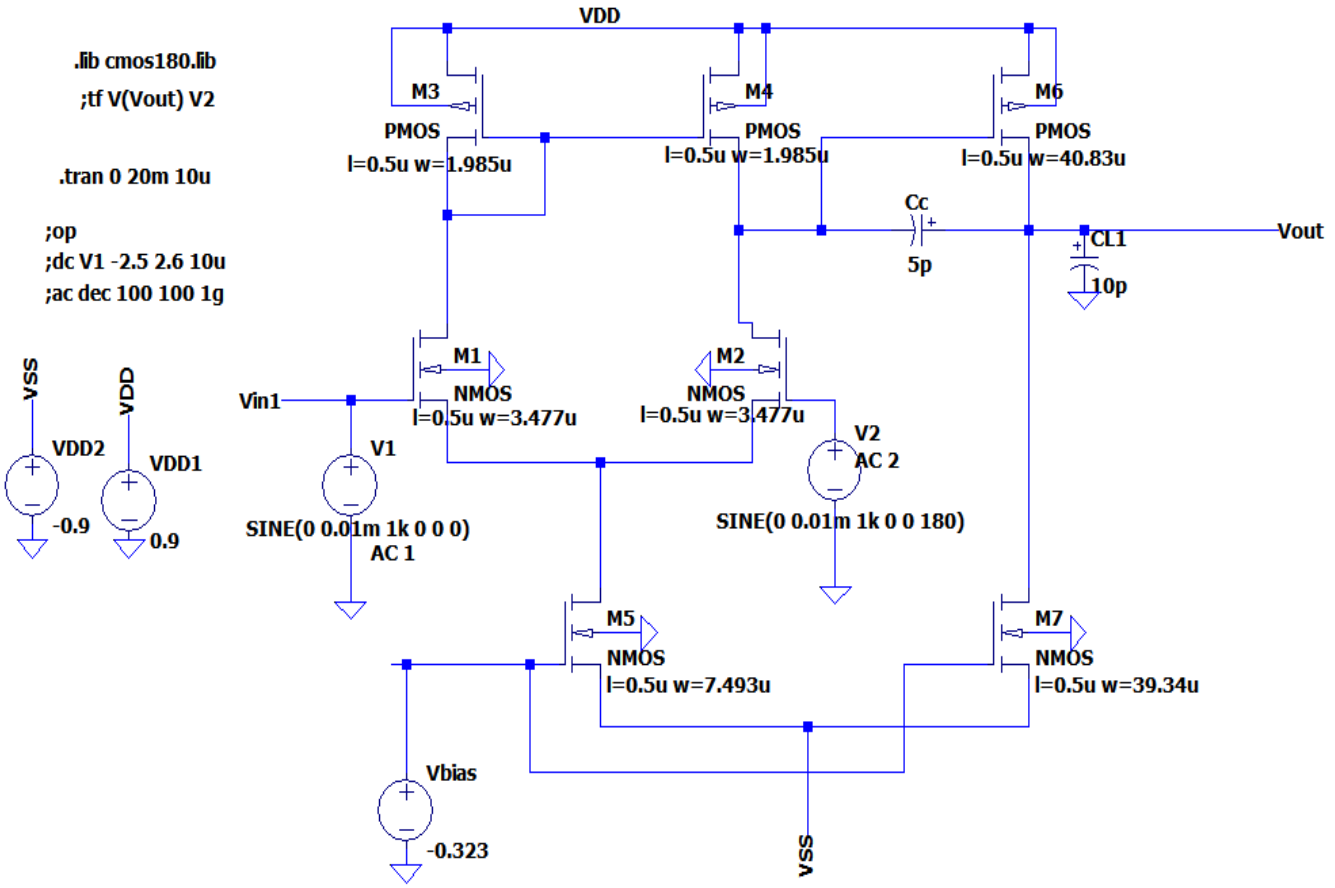
$$\Rightarrow V_{\text{bias}} = \boxed{-0.323\,V}$$

$$V_{\text{out(max)}} = V_{DD} - V_{DS6(\text{SAT})} = 0.9 - \sqrt{\frac{2I_6}{K_p(W_6/L_6)}} = 0.9 - 0.28 = \boxed{0.62\,V}$$

$$V_{\text{out(min)}} = V_{SS} + V_{DS7(\text{SAT})} = -0.9 + \sqrt{\frac{2I_6}{K_n(W_7/L_7)}} = -0.9 + 0.18 = \boxed{-0.72\,V}$$

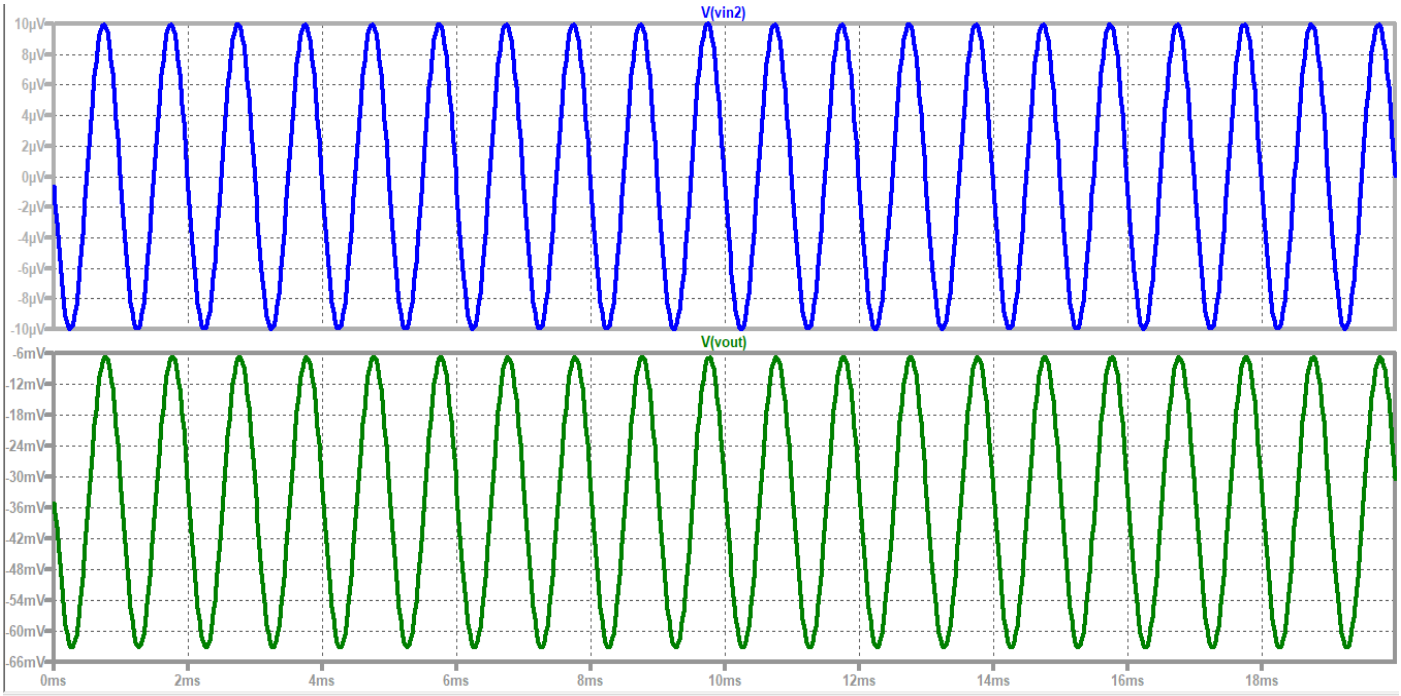
❖ Results

- **LTSPICE schematic:**



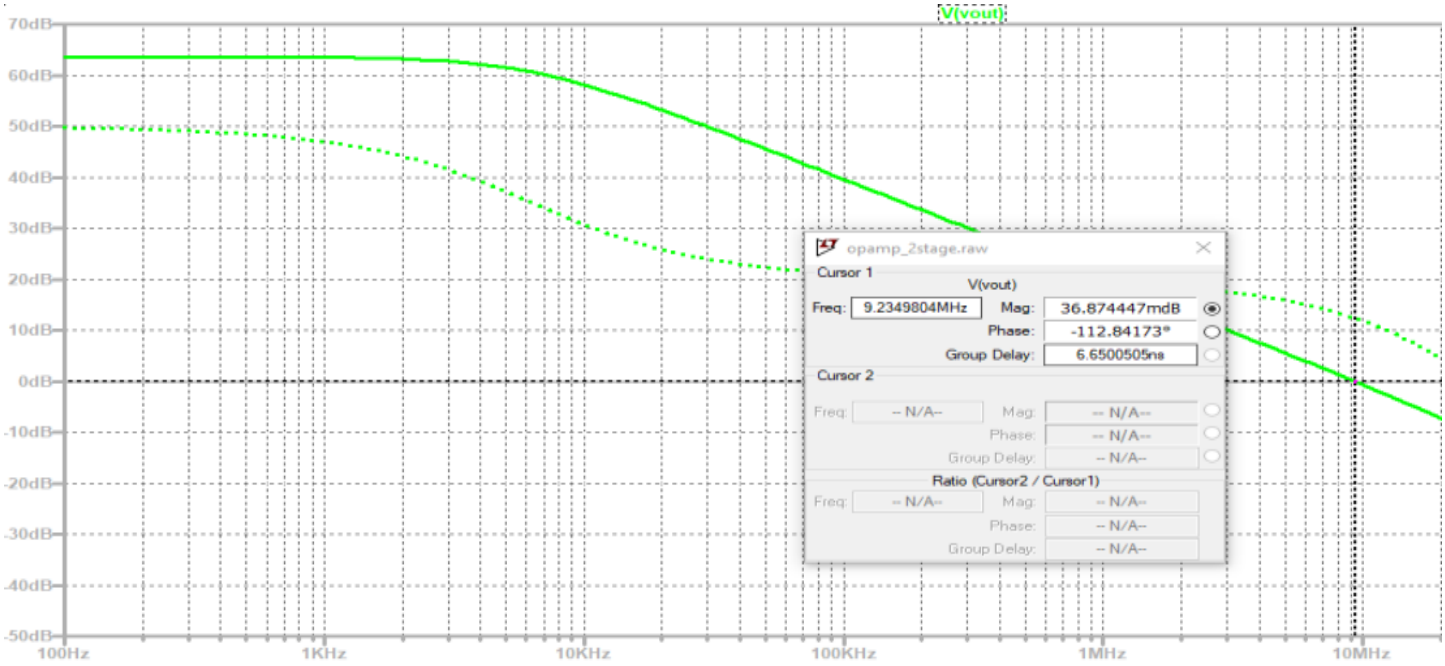
- **Simulation of Av**: Vpp of Vin is 10uV, Vpp of Vout is 56.3mV

Av = 56.3mV / 10uV = 5630 V/V



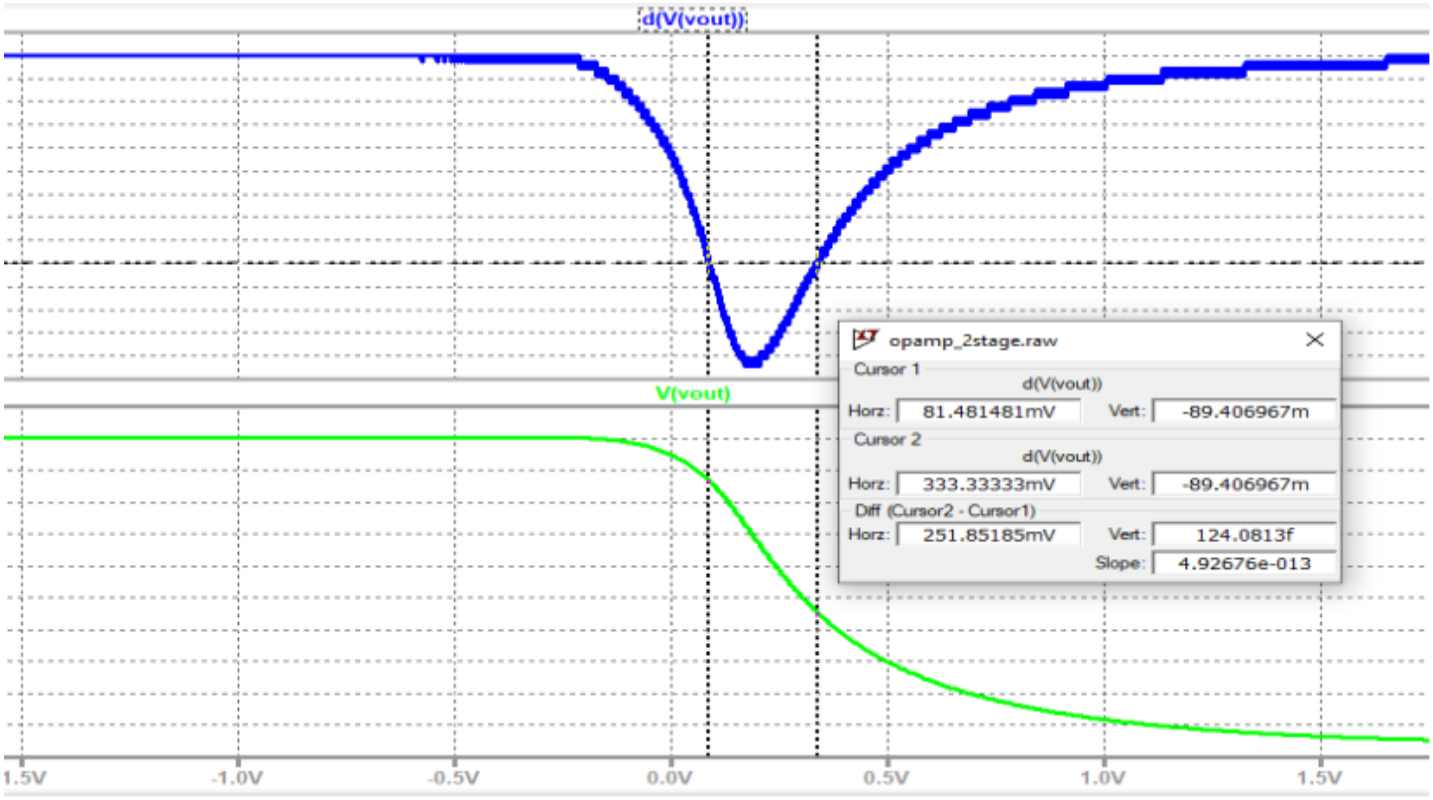
- **Simulation of Gain Bandwidth and Phase Margin:**

  At 0dB have GB = 9.23MHz and PM = 180 - 112 = 68 degree



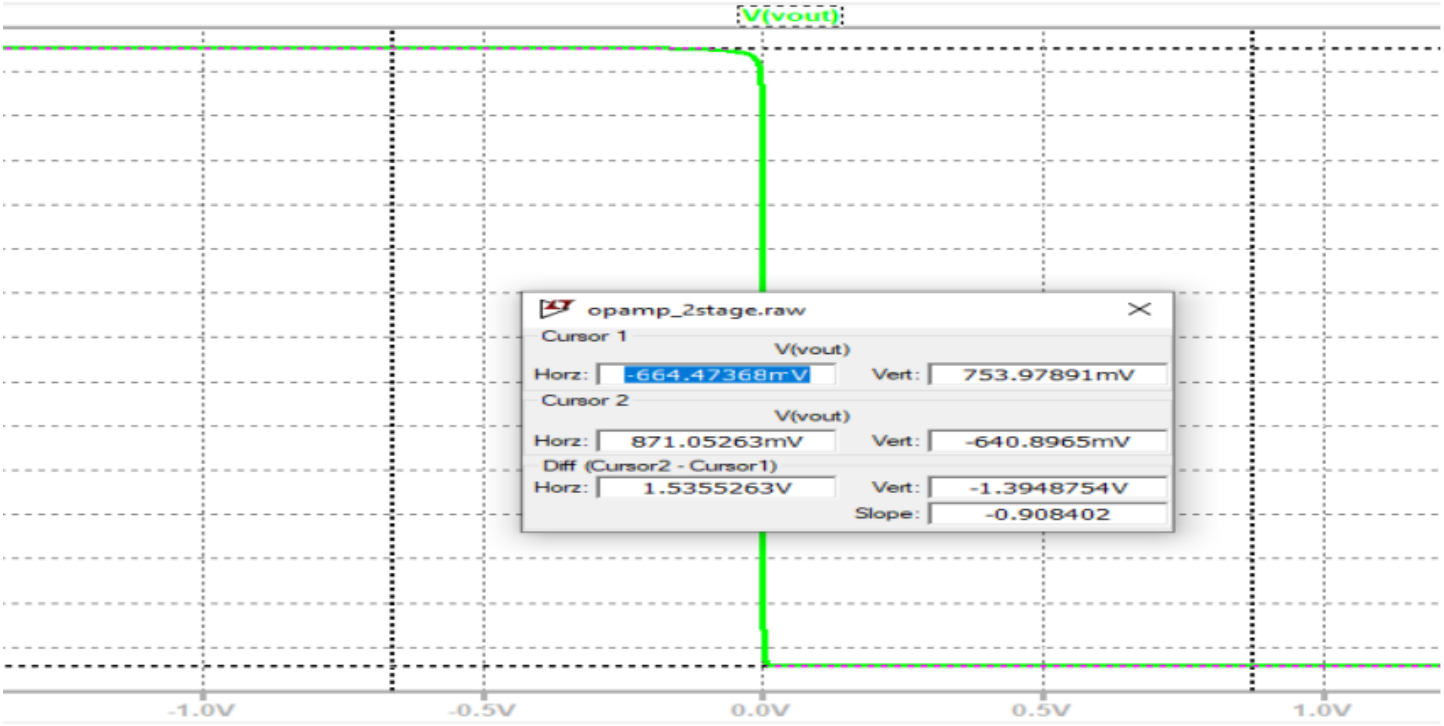
- **Simulation of ICMR:**

  Connect Vout with Vin(-) and simulate in DC mode has ICMR: -0.081V -> 0.333V

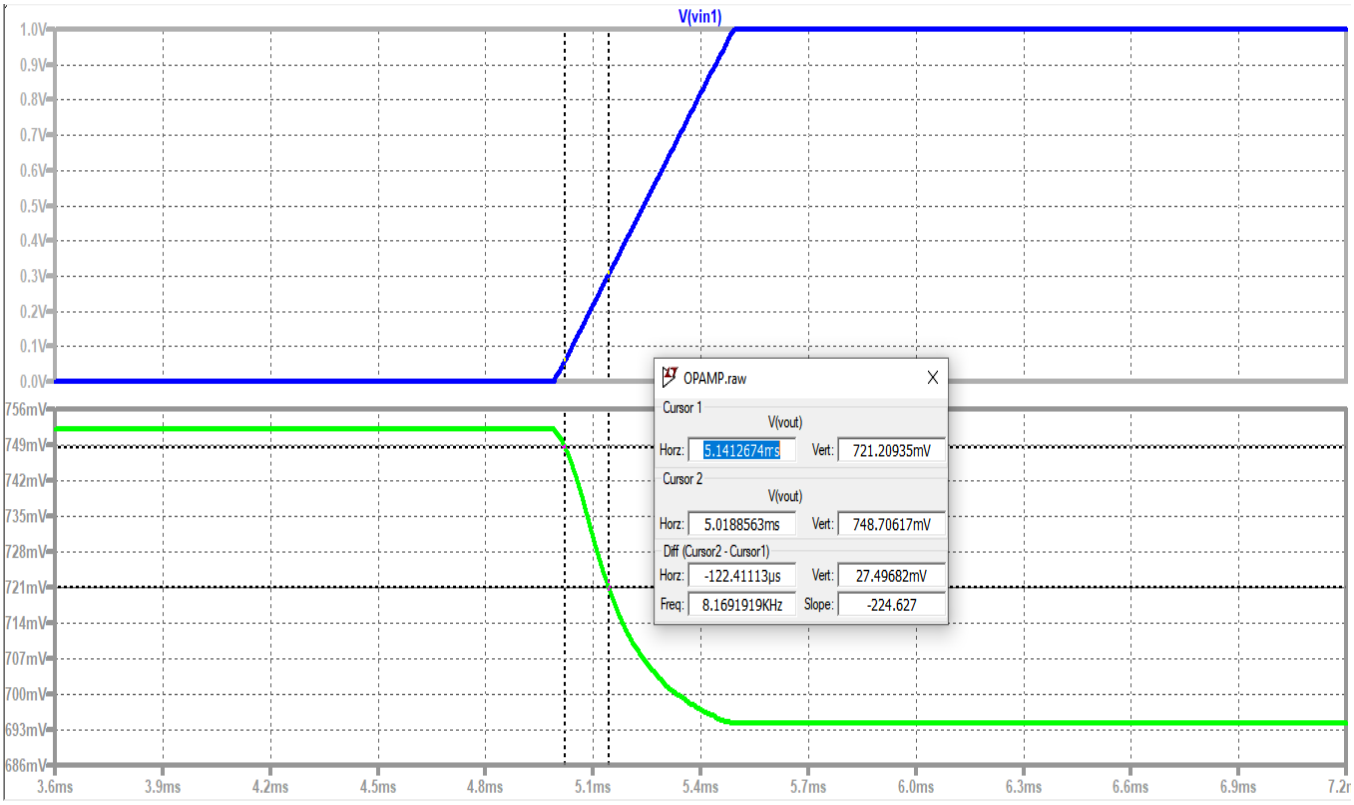


- **Simulation of Vout range:**

  simulate with DC mode has Vout range: -0.64V -> 0.753V



- **Simulation of Slew Rate:**



- **Simulation of Power Dissipation**

$P_{diss} = (V_{DD} + |V_{SS}|) . I_{SS} = (0.9V + 0.9V)$***95.735µA** = **0.1723mW**

Ib(M4):	9.81637e-013	device_current
Is(M4):	-3.02648e-005	device_current
Id(M7):	0.000620031	device_current
Ig(M7):	0	device_current
Ib(M7):	0.586354	device_current
Is(M7):	-0.586975	device_current
Id(M5):	9.57356e-005	device_current
Ig(M5):	0	device_current
Ib(M5):	0.586372	device_current
Is(M5):	-0.586468	device_current
Id(M2):	3.02648e-005	device_current
Ig(M2):	0	device_current
Ib(M2):	1.7603e-005	device_current
Is(M2):	-4.78678e-005	device_current

- **Comparision**

Value	Requirement	Calculation	Simulation
Av	> 3000 V/V	5323 V/V	5630 V/V
GB	10 MHz	10 MHz	9.23 MHz
V_{out} range	-0.5V → 0.5V	-0.72V → 0.62V	-0.64V → 0.753V
ICMR	-0.5V → 0.5V	-0.5V → 0.5V	-0.081V → 0.333V
P_{diss}	≤ 3 mW	0.675 mW	0.1723 mW
Phase Margin	60°	60°	68°
Slew Rate	> 12 V/µs	12 V/µs	0.22 mV/µs