

Article

New High-Gain Transformerless DC/DC Boost Converter System

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Abstract: This article proposes a new high-gain transformerless dc/dc boost converter. Although they possess the ability to boost voltage at higher voltage levels, converter switching devices are under low voltage stress. The voltage stress on active switching devices is lower than the output voltage. Therefore, low-rated components are used to implement the converter. The proposed converter can be considered as a promising candidate for PV microconverter applications, where high voltage-gain is required. The principle of operation and the steady-state analysis of the converter in the continuous conduction mode are presented. A hardware prototype for the converter is implemented in the laboratory to prove the concept of operation.

Keywords: high gain dc/dc converter; low voltage stress; photovoltaic (PV)



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1. Introduction

Currently, dc/dc converters are used in most industrial applications. However, for photovoltaic (PV) energy systems, a step-up dc/dc boost converter is mandatory to boost the low voltage to higher level to enable grid integration or supply power to an islanded load, see Figure 1. In most of the practical cases, the converter is configured to generate output voltage around 400 V, with input voltage only ranging from 18 to 50 V [1–4].

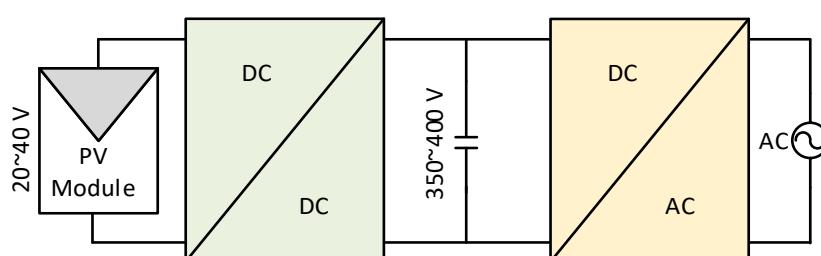


Figure 1. Two stage PV microinverter.

In ideal scenarios, the voltage gain of the classical boost converter is infinite. However, practically, its step-up ability is limited and restricted by the power device's parasitic components, capacitance and inductance, and conduction losses caused by resistances and diode voltage drops. Another limitation for having such a high step-up ratio is that triggering the power switch during the high duty cycle may cause reverse recovery problems and magnetic saturation issues [5–8]. Several papers have been published in the literature, attempting to create boost converters with high gain and high efficiency [9–17]. Step-up dc/dc converters can be classified based on the inclusion of a transformer that is

isolated vs. non-isolated. Topologies that include a transformer can provide high voltage-gain by controlling the turns ratio of the transformer. Moreover, transformers provide isolation between the output and input sides. Transformerless topologies are competitive in terms of cost, weight, and design simplicity [15].

Topology presented in [17], which is based on cascading boost converters, is able to achieve higher voltage gain without an extreme duty cycle as compared to the classical boost converter; however, its switching devices are under high voltage/current stress.

Another possible solution for providing a higher voltage gain is the use of switched inductors/capacitors [18–22]. A switched inductor converter has a voltage gain double of that reported for the classical boost converter; however, its semiconductors are under high voltage stress.

In some papers, voltage lift methodology is applied [23–25] in order to achieve high voltage-gain, as well as reduce voltage/current stress on the switches. However, multiple diodes and capacitors are required when the conversion ratio is high.

Isolated topologies, such as coupled inductors and flyback converters, use the turns ratio, in addition to the duty cycle, to control the converter voltage gain. As the required step-up ratio is performed at moderate duty cycle, the overall efficiency is increased. However, in topologies such as the flyback converter, voltage spikes on the active switch appear due to the discharging energy of leakage inductance. Increasing dissipations are the inevitable result of the discharging energy of leakage inductance on the active switch [25,26]. Different solutions for such problems exist such as the employment of active clamp circuits (considered a costly solution) and passive clamp circuits [26,27].

Switched capacitor converters are used to provide boosting ability without any magnetic components [28–31]. Hard switching switched capacitor boost converters suffer from low efficiency, less than 75%, as reported in [32]. Adding a resonance inductor improves the switched capacitor performance [32,33]. The boosting range is still somewhat limited compared to converters with inductors, the duty cycle of which can be varied for a wide range of boosting.

In certain applications, the PV module is connected directly to its dc-dc converter; in this case, input voltage would be in the range of 33 V to 45 V; hence, a high step-up ability is mandatory. One of the main functions of the dc-dc converter is to elevate module voltage from 33~50 V to 400~700 V. Hence, a high step-up ability is required. In this paper, a new dc/dc converter with high step-up ability is proposed. The proposed converter is well suited for different applications, such as photovoltaic (PV) systems. The proposed topology has some distinct advantages, including a high step-up capability, low voltage-stress on the active devices, and moderate efficiency.

The structure of this paper consists of three subsequent sections. Section 2 discusses the proposed converter operation and the steady-state analysis. Section 3 includes experimental results and discussions. The last section, Section 4, is the conclusion.

2. Proposed High Step-Up Converter

The configuration of the proposed converter is depicted in Figure 2. It consists of two diodes, three inductors, two capacitors, and three switches. The three switches are triggered on and off simultaneously. The two-diodes are operate in a complementary manner to the switches in order to provide a free path for the inductor current. Inductors charge in parallel when the switches are turned on and discharge their energy to the output load once switches are turned off. In the upcoming analysis, the small-ripple approximation is used. The converter is designed to operate in the continuous conduction mode (CCM). The parameters are assumed to be ideal for the upcoming analysis in order to facilitate the analysis of the converter. A graph of the ideal key waveforms of the circuit devices is shown in Figure 3. The two possible operating modes of the converter are discussed as follows:

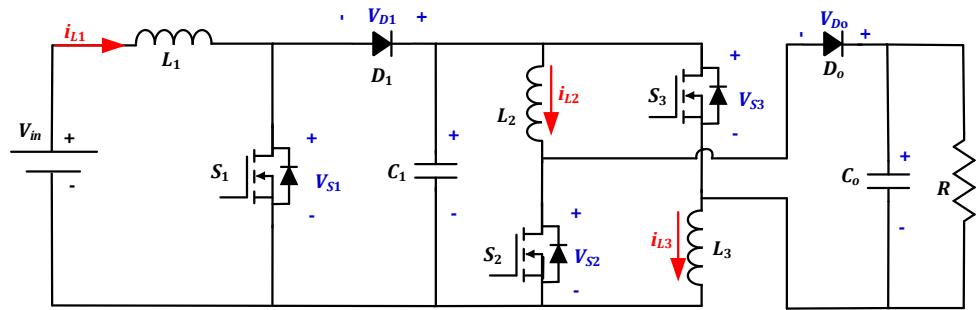


Figure 2. The proposed configuration.

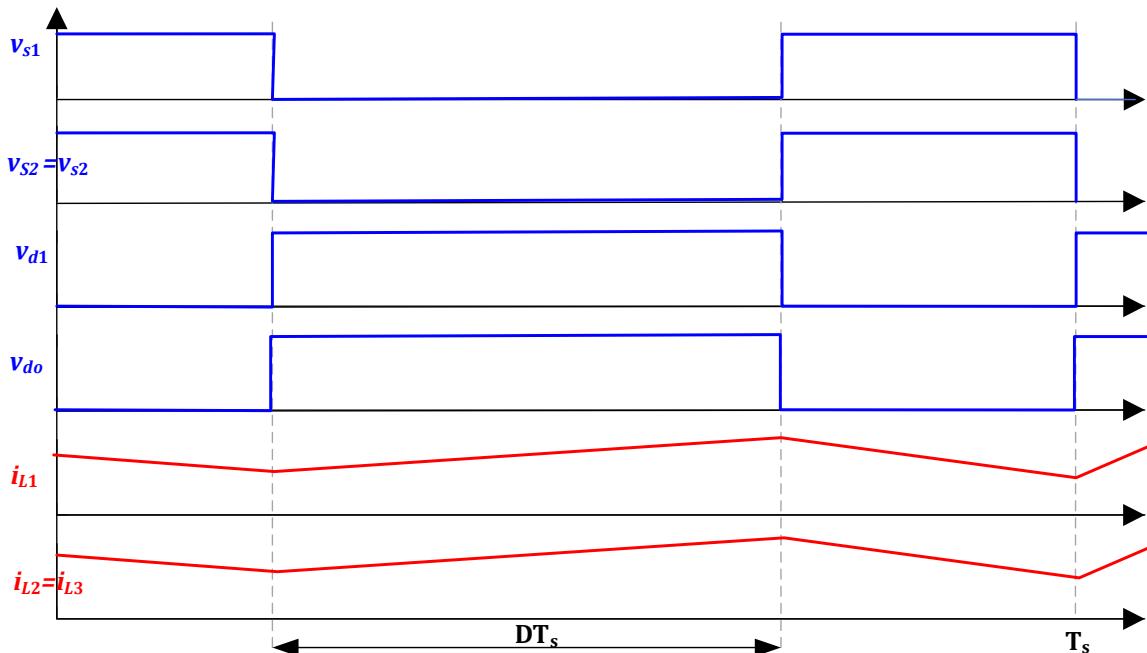


Figure 3. The ideal key waveforms of the converter.

2.1. Mode I

This mode is activated once the switches are turned on, and the depiction of this mode is illustrated in Figure 4. The three switches are turned on simultaneously. In this mode, inductor L_1 is energized from the input dc-source, while inductors L_2 and L_3 are energized from capacitor C_1 . Diodes D_1 and D_o are reversely biased. Output capacitor C_o releases its energy to the load side. The characteristic equations that describe this mode of operation are as follows:

$$\begin{cases} v_{L1}(t) = V_{in} \\ v_{L2}(t) = v_{L3}(t) = V_{C1}(t) \\ i_{co}(t) = -V_o(t)/R \\ i_{C1}(t) = 2i_{L2}(t) \end{cases} \quad (1)$$

where V_{in} , V_o , V_{C1} , D , R , V_{L1} , V_{L2} , i_{co} , i_{L1} , and i_{L2} are denoted to input voltage, output voltage, capacitor C_1 voltage, duty cycle, load resistance, inductor L_1 voltage, inductor L_2 voltage, capacitor C_o current, inductor L_1 current and inductor L_2 current, respectively.

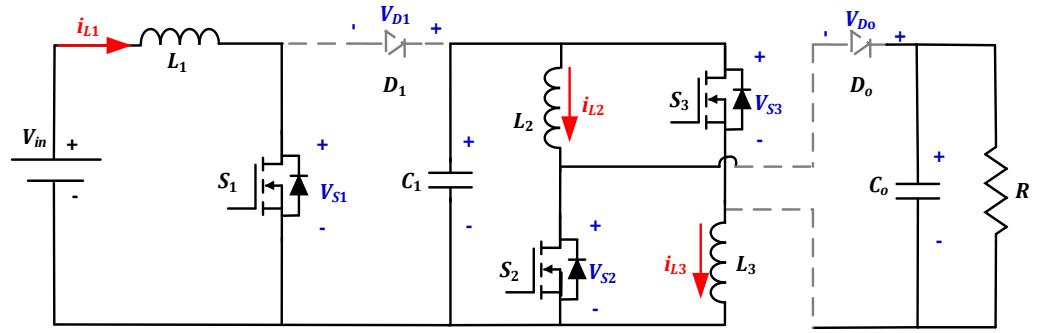


Figure 4. The configuration of mode I.

2.2. Mode II

This mode is activated once the switches are turned off, and the depiction of this mode is illustrated in Figure 5. The three switches are turned off at the same time. In this mode, inductor L_1 is discharging its energy into capacitor C_1 , while inductors L_2 and L_3 are discharging their energy into output load and output capacitor C_o . In order to maintain a continuous path for the inductor currents, diodes D_1 and D_o work as freewheeling diodes when they are turned on. The characteristic equations that describe this mode of operation are as follows:

$$\begin{cases} v_{L1}(t) = V_{in}(t) - V_{C1}(t) \\ v_{L2}(t) = v_{L3}(t) = (V_{C1}(t) - V_o(t))/2 \\ i_{co} = i_{L2} - V_o(t)/R \\ i_{C1}(t) = i_{L1}(t) - i_{L2}(t) \end{cases} \quad (2)$$

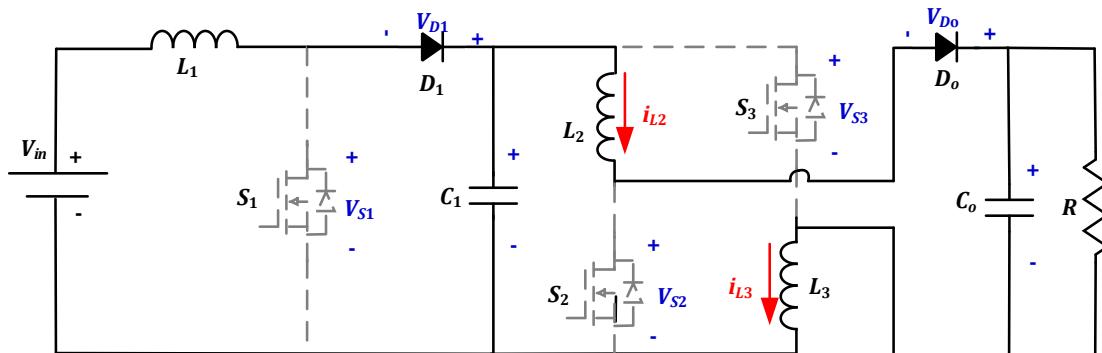


Figure 5. The configuration of mode II.

The steady state voltage of capacitor C_1 is obtained from (1) and (2).

$$\begin{cases} V_{C1} = \left(\frac{1}{1-D}\right) * V_{in} \\ V_{C1} = \left(\frac{1-D}{1+D}\right) * V_o \end{cases} \quad (3)$$

$$\frac{V_o}{V_{in}} = \frac{(1+D)}{(1-D)^2} \quad (4)$$

Equation (3) represents the relationship between the voltage across capacitor C_1 and input/output voltages. The voltage gain of the converter is given by Equation (4).

The voltage and current stresses of each component are depicted in Tables 1 and 2, respectively. All components have a voltage stress lower than the output voltage. This is a distinct advantage of this topology. It enables us to select the devices with low ratings, thus improving the overall efficiency of the system.

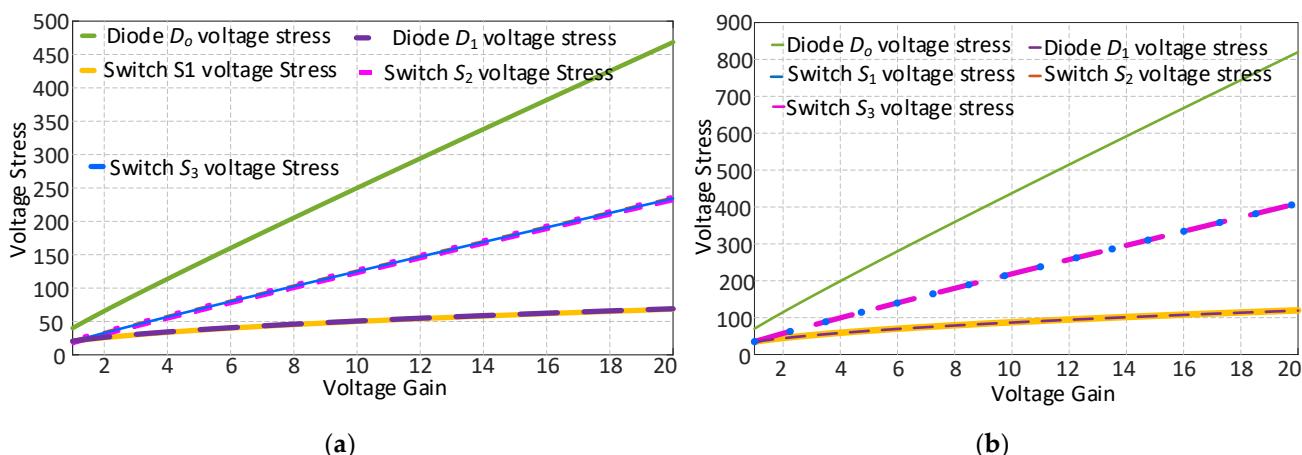
Table 1. The voltage stresses of the switching devices.

Switching Device	Peak Voltage Stress
S_1	$V_o * (1 - D) / (1 + D)$
S_2	$V_o / (1 + D)$
S_3	$V_o / (1 + D)$
D_1	$V_o * (1 - D) / (1 + D)$
D_o	$2 * V_o / (1 + D)$

Table 2. The current stresses of the switching devices.

Switching Device	RMS Current Stress
S_1	$I_{in} * \sqrt{D}$
S_2	$(1 - D) * \sqrt{D} * I_{in} / 2$
S_3	$(1 - D) * \sqrt{D} * I_{in} / 2$
Freewheeling Diodes	Average Current Stress
D_1	$I_{in} * (1 - D)$
D_o	$(1 - D)^2 * I_{in} / 2$

Figure 6 is the depiction of the device voltage stress as a function of the converter voltage gain with a fixed input voltage. The switch S_1 and diode D_1 are under the same voltage stress, while the output diode D_o is the component under the highest voltage stress.

**Figure 6.** The component voltage stress vs. voltage gain at an input voltage of (a) 20 V; (b) 35 V.

The design and selection of converter parameters, such as inductor and capacitor values, are based on the amount of ripple allowed on each element. The design of the proposed circuit parameters are illustrated in the following sections.

2.3. Inductor L_1 Design

The inductor L_1 current is shown in Figure 7. The average value of the inductor L_1 current is defined as I_1 and the difference between the inductor peak and the average current is Δi_{L1} .

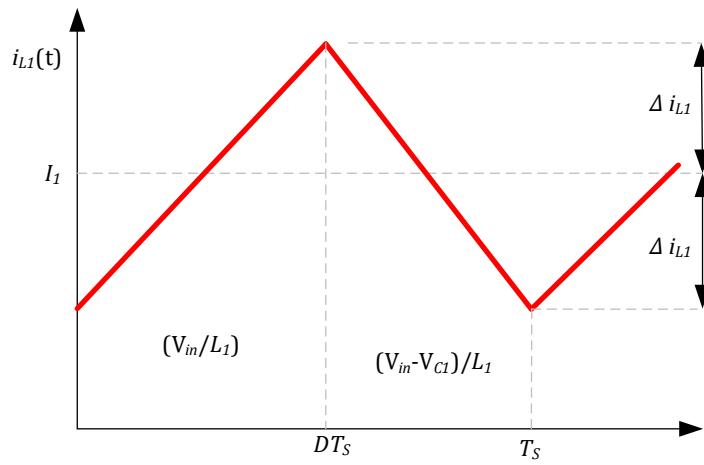


Figure 7. The inductor L_1 current.

Considering the first interval of the switching cycle, the ripple of inductor L_1 is given by

$$2\Delta i_{L1} = \left(\frac{V_{in}}{L_1} \right) DT_S \quad (5)$$

$$L_1 = \left(\frac{V_{in}}{2\Delta i_{L1}} \right) DT_S \quad (6)$$

As Equation (6) describes, the inductance of L_1 depends on the input voltage V_{in} , duty cycle D , sample time T_S , and inductor current ripple Δi_{L1} .

2.4. Inductor L_2 and L_3 Design

The inductor L_2 , which is similar to L_3 , current is shown in Figure 8. The average value of the inductor L_2 current is defined as I_2 and the difference between the inductor peak and the average current is Δi_{L2} . Considering the first interval of the switching cycle, the ripple of inductor L_2 is given by

$$2\Delta i_{L2} = \left(\frac{V_{in}}{L_2} \right) \left(\frac{DT_S}{1-D} \right) \quad (7)$$

$$L_2 = L_3 = \left(\frac{V_{in}}{2\Delta i_{L2}} \right) \left(\frac{DT_S}{1-D} \right) \quad (8)$$

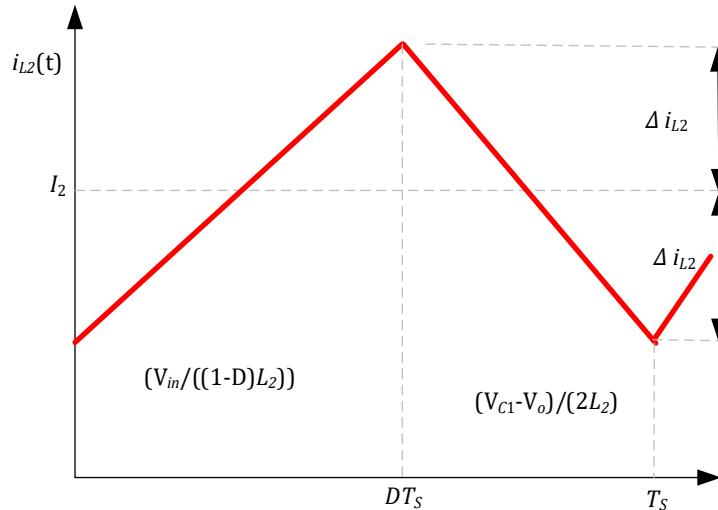


Figure 8. The inductors L_2 and L_3 currents.

As Equation (8) describes, the inductance of inductors L_2 and L_3 depend on the input voltage V_{in} , duty cycle D , sample time T_s , and the inductor current ripple ΔiL_2 .

2.5. Output Capacitor Co-Design

The output voltage ripple of the converter is limited by the amount of ripple permitted on the capacitor C_o voltage. Consequently, capacitor C_o should be designed to ensure that the converter output voltage exhibits ripple within the permitted range.

The capacitor C_o voltage is expressed in Figure 9, where V_o is the capacitor voltage average value and the difference between the capacitor peak and the average voltage is Δv_o . Considering the first interval of the switching cycle, the ripple of capacitor C_o is given by

$$\Delta v_o = \left(\frac{V_o}{2RC_o} \right) DT_S \quad (9)$$

$$C_o = \left(\frac{V_o}{2\Delta v_o} \right) DT_S \quad (10)$$

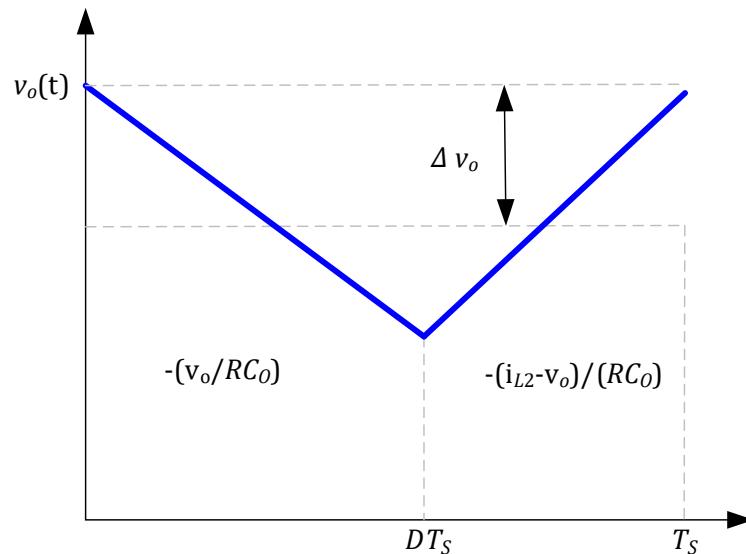


Figure 9. The capacitor C_o output voltage.

As can be seen from Equation (10), the value of capacitor C_o depends on the output voltage V_o , duty cycle D , sample time T_S , and the capacitor voltage ripple Δv_o .

2.6. Capacitor C_1 Design

The design of capacitor C_1 is not straightforward; similar to capacitor C_o , its current is equal to the inductor L_1 current, but without the dc components (see Figure 10). As seen in Figure 9, the capacitor C_1 voltage reaches its maximum and minimum limits at the two zero crossing points of its current waveforms [34].

Let Δv_{c1} be the difference between the average and max value of the capacitor C_1 voltage value; the relation between the total charge q and the peak-to-peak ripple of the capacitor C_1 voltage is

$$q = C_1(2\Delta v_{c1}) \quad (11)$$

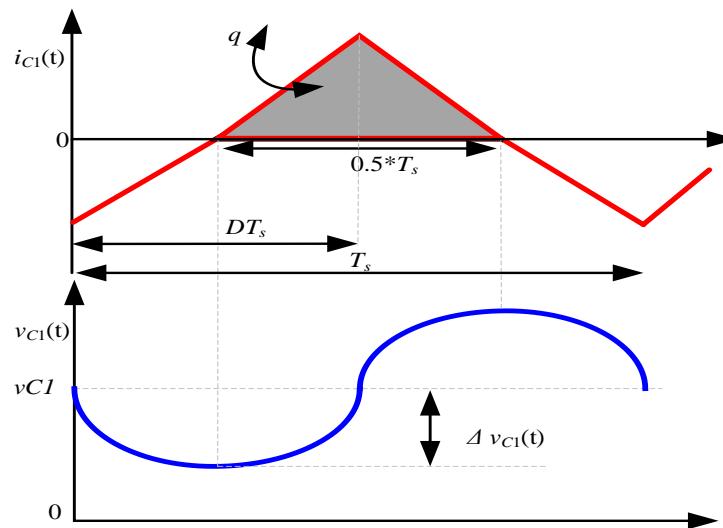


Figure 10. The capacitor C_1 current and voltage.

The value of charge q is obtained by integrating the shaded area of the capacitor C_1 current (see Figure 9), and due to the symmetry of the capacitor, the current waveform q is given by:

$$q = \frac{1}{2} \Delta i_L \frac{T_S}{2} \quad (12)$$

Substitute Equation (12) into Equation (11) and a solution for the voltage ripple peak amplitude yields

$$\Delta v_{C1} = \frac{\Delta i_L T_S}{8C_1} \quad (13)$$

Hence,

$$C_1 = \frac{\Delta i_L T_S}{8\Delta v_{C1}} \quad (14)$$

The capacitor C_1 value depends on the inductor L_1 current ripple, the sampling time, and the permitted ripple on the capacitor C_1 .

3. Results

A testbench for the proposed converter was implemented in the laboratory to verify its operation and characteristics. The parameters used for implementing the proposed converter are given in Table 3. The developed prototype is illustrated in Figure 11.

Table 3. The specification of the system parameters.

Component	Description	Specification
V_{in}	Input voltage	20–35 V
V_o	Output voltage	100–350
L_1, L_2, L_3	Input inductor	3 mH
C_{in}	Input capacitor	260 μ F
C_1	Parallel capacitor	260 μ F
C_o	Output capacitor	260 μ F
S_1, S_2 and S_3	Power MOSFET	IRFP264
D_1	Power diode	BYV72EW-200
D_o	Output diode	BYV72EW-200
F_S	Switching frequency	30 KHz
P_o	Rated output power	175 W

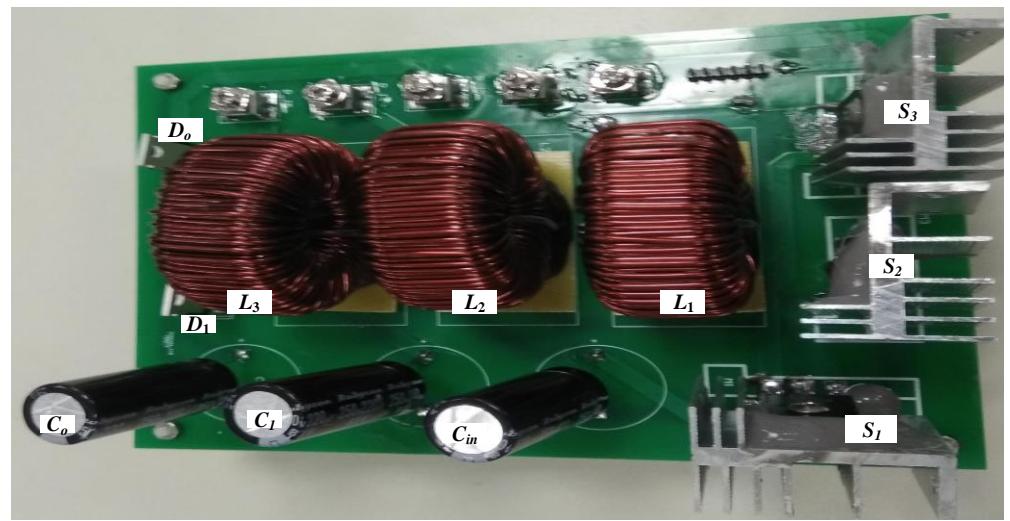


Figure 11. A photo of the hardware.

The three switches are triggered simultaneously to avoid any short circuits; hence, no deadtime is added to the controller. Switches S_2 and S_3 face similar voltage stress, while S_1 encounters a different voltage stress (see Figure 12). Figure 12 is a case of study in which the duty cycle is set to 0.4, the input voltage is 35 V, and the measured output across the converter voltage is around 130 V.

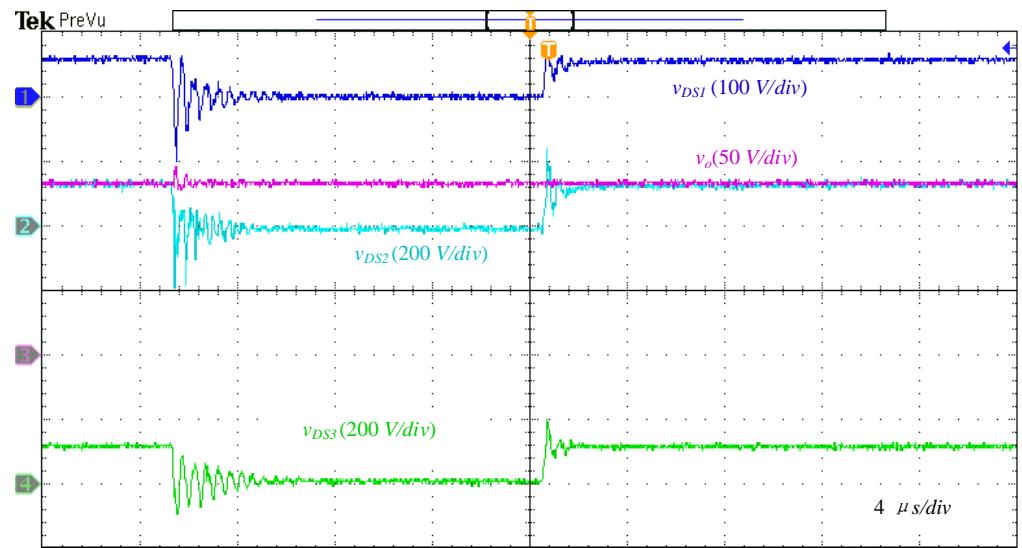


Figure 12. The output voltage, switch S_1 drain source voltage, S_2 drain source voltage, and S_3 drain source voltage at an input voltage 20 V and a duty cycle of 0.4.

The circuit diodes D_1 and D_0 operate as a freewheeling diodes, and both are on when the switches are off. The diode D_1 reverse voltage is illustrated in Figure 13. Figure 13 shows a new case study, where the duty cycle is set to 0.6 with 20 V input voltage, and the output voltage is around 200 V. The inductor L_1 current is illustrated in Figure 14.

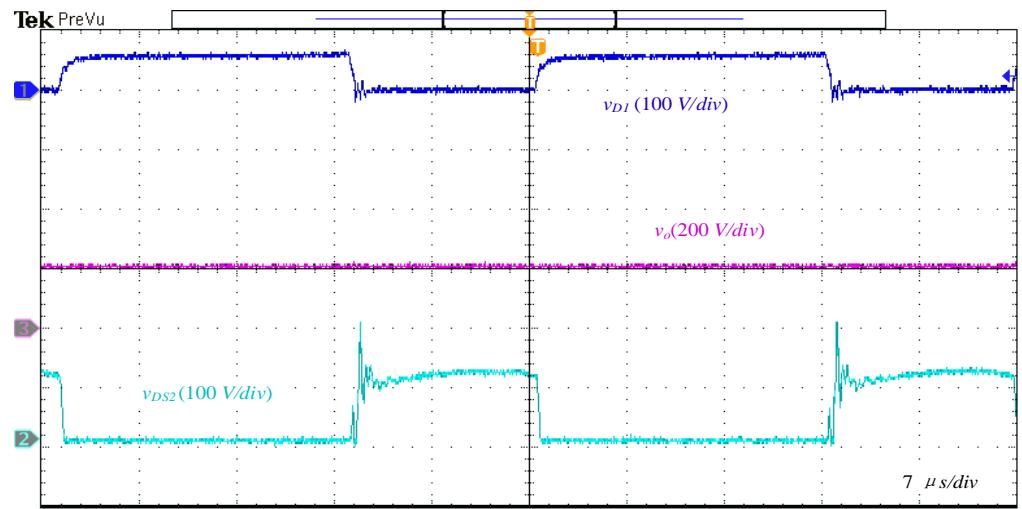


Figure 13. The output voltage, switch S_2 drain source voltage, and diode D_1 reverse voltage at an input voltage of 20 V and a duty cycle of 0.6.

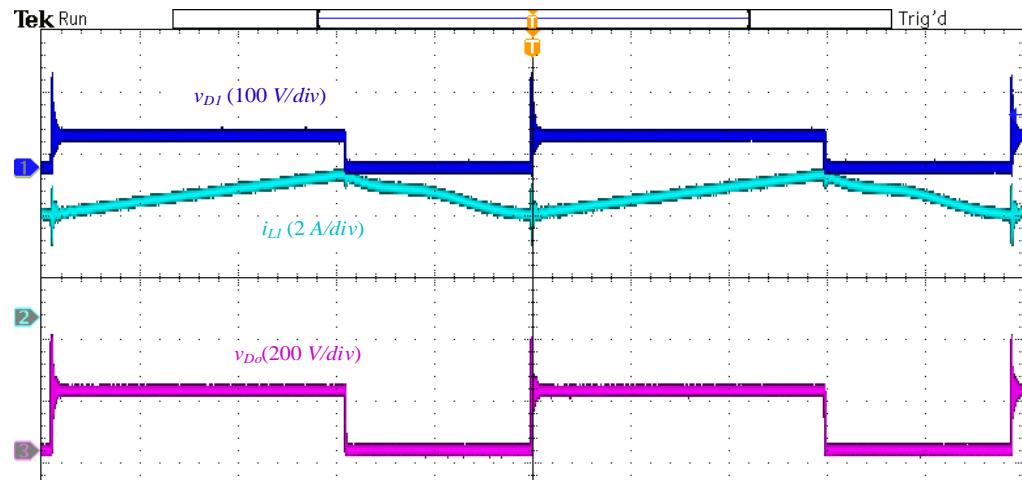


Figure 14. The inductor L_1 current, diode D_1 reverse voltage, and diode D_0 reverse voltage.

In the case study shown in Figure 15, the converter duty cycle is set to 0.6 with 20 V input voltage; the measured output voltage in this case is around 240 V.

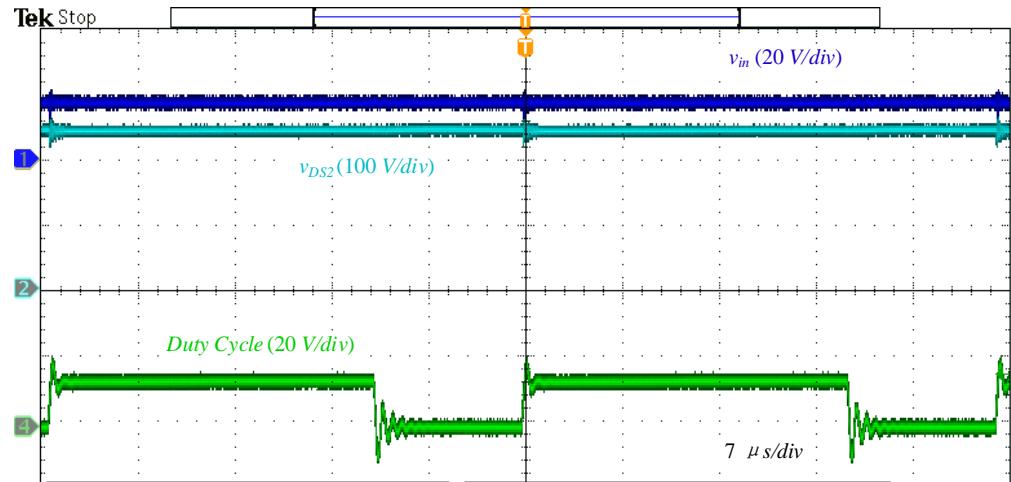


Figure 15. A case of study where the duty cycle is set to 0.65, and the input voltage is 20 V.

An analytical analysis for the converter losses is performed with the help of PSIM thermal modules. A case study is illustrated in Figure 16, where the input power, input voltage, switching frequency, voltage gain and duty cycle are set to 20 V, 240 W, 30 kHz, 3.9, and 0.6, respectively. As illustrated in the figure, the conduction losses are dominant. The switch S_1 is the main source of conduction losses, while inductor L_1 has the highest value of conduction loss compared to L_2 and L_3 .

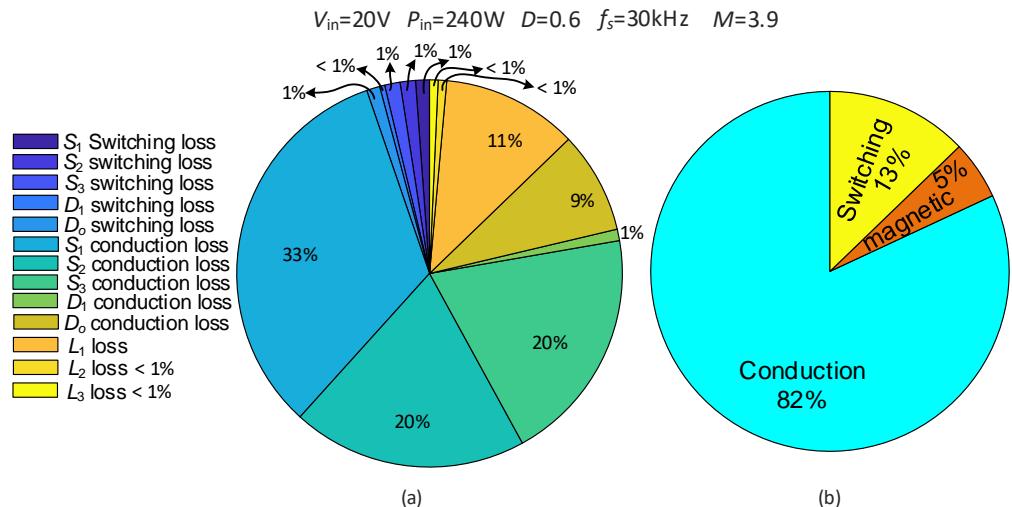


Figure 16. The switching and conduction losses distribution—(a) element losses distribution; (b) total losses distribution.

Figure 17 illustrates the relation between the calculated and measured converter voltage gain; the results are consistent and the slight differences are due to the effect of the losses on the converter voltage gain. Efficiency is a major factor in selecting a converter for a specific application, and achieving higher efficiency at a higher voltage gain is a desirable factor for some applications, such as for PV microconverters. Figure 18 is a depiction of the efficiency of the proposed converter, with the input voltage set to 20 V and the duty cycle set to 0.6; the voltage gain at this point is around 10 times that illustrated in Figure 13. Converter efficiency improves by increasing the input power. Efficiency at 175 W input power is around 88%, which is comparable compared to the results reported in the literature. The main sources for losses are the semiconductors. In Figure 19, two case studies are presented where the converter efficiency is measured using IRFP264 MOSFETs and CREE C3M00211120k. Utilizing silicon carbide switches improves the efficiency due to very low resistance, in a range of $21\text{ m}\Omega$, and very small switching losses. Nevertheless, this comes at a very high cost.

In the literature, several solutions have been presented for integrating PV systems into existing systems. Providing high step-up capability is a mandatory characteristic for any converter used in photovoltaic applications. Figure 20 provides a voltage gain comparison between the proposed topology and other transformerless topologies reported in the literature. The graph plots the voltage gain of all the converters with variable duty cycles. The traditional boost converter has the minimum boosting capability among all presented converters, while the proposed converter has the highest gain among the different topologies. Table 4 compares the different topologies with the proposed topology from the point of view of the number of active switches, number of diodes, and voltage stresses for each device. The proposed converter provides high voltage-gain, while at the same time, imposing small voltage stresses on the active devices. Such features make the proposed converter a very good candidate for PV microconverter applications.

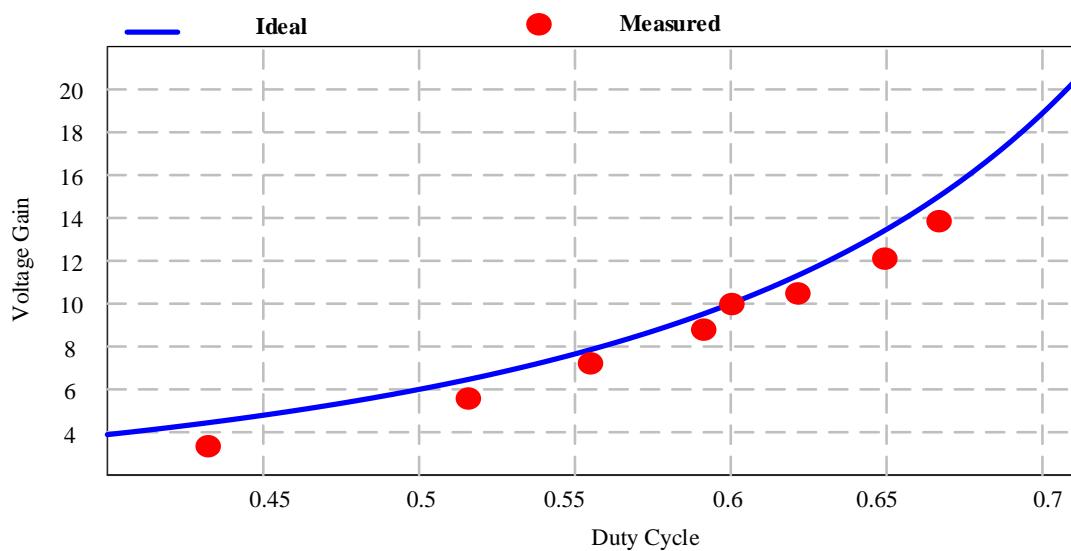


Figure 17. The ideal and measured voltage gain.

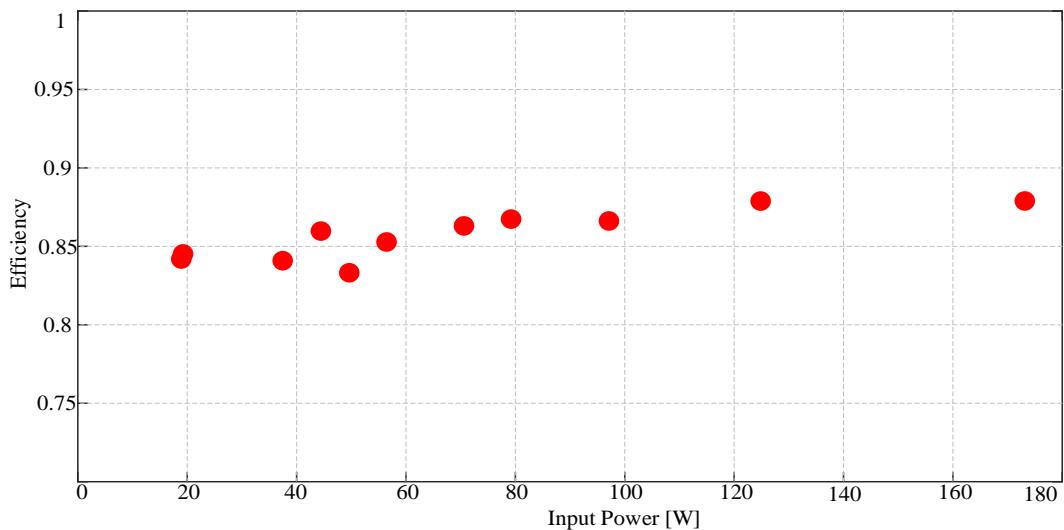


Figure 18. The measured efficiency.

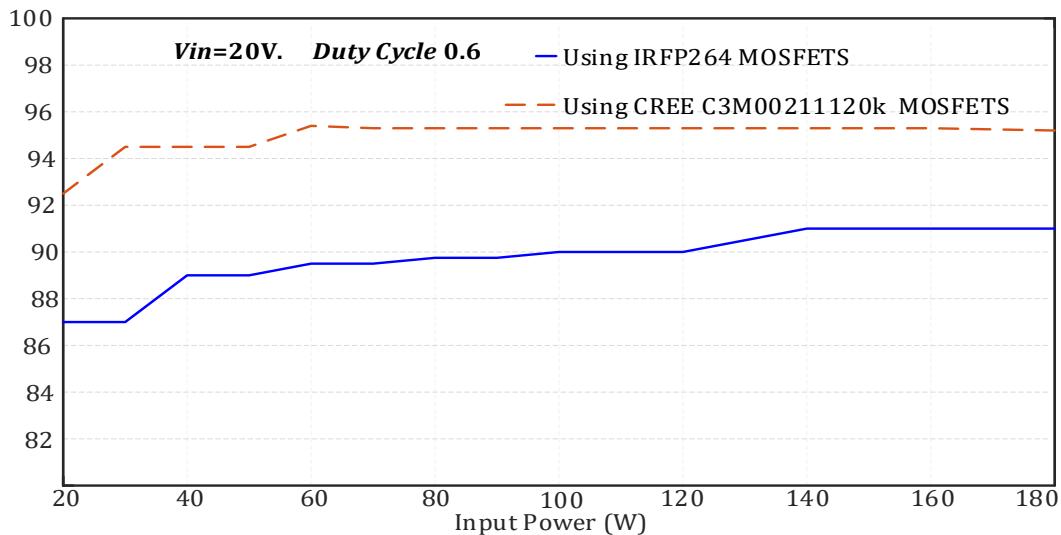


Figure 19. The converter efficiency using IRFP264 MOSFET and C3M00211120k CREE MOSFET.

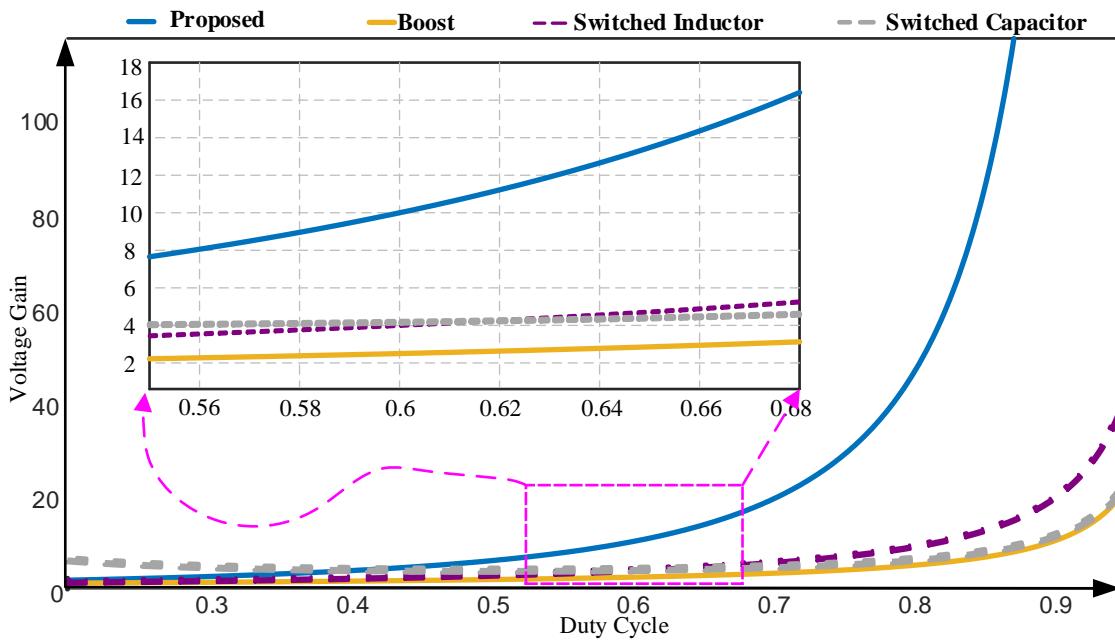


Figure 20. The voltage gain comparison among different dc-dc step-up topologies.

Table 4. The comparison of Step-up Topologies.

Topology	Boost	SL-Boost	SC-Boost	[35]	[36]	[37]	[38]	New
No. Switches	1	1	1	2	4	2	2	3
No. Diode	1	4	3	4	0	6	2	2
Voltage Gain	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$	$\frac{3-2D}{1-2D}$	$\left(\frac{1}{1-D}\right)^2$	$\frac{4}{(1-D)}$	$\frac{1+D-D^2}{(1-D)^2}$	$\frac{1+D}{(1-D)^2}$
Switch Stress	S_1	V_o	V_o	$\frac{V_o}{2}$	$\frac{V_o-V_{in}}{2}$	V_o	$\frac{V_o}{2}$	$\frac{V_{in}}{1-D}$
	S_2	-	-	-	$\frac{V_o-V_{in}}{2}$	V_o	$\frac{V_o}{4}$	$\frac{V_{in}}{(1-D)^2}$
	S_3	-	-	-	-	V_o	-	-
	S_4	-	-	-	-	$V_o(1-D)$	-	-
Diode Stress	D_1	-	V_{in}	-	$\frac{V_o-V_{in}}{2}$	-	$\frac{V_o}{4}$	$\frac{V_{in}}{1-D}$
	D_2	-	$\frac{V_o-V_{in}}{2}$	-	$\frac{V_o-V_{in}}{2}$	-	$\frac{V_o}{4}$	$V_o + V_{in}$
	D_3	-	$\frac{V_o-V_{in}}{2}$	-	$\frac{V_o-V_{in}}{2}$	-	$\frac{V_o}{2}$	-
	D_5	-	-	-	-	-	$\frac{V_o}{2}$	-
	D_o	V_o	V_o	$\frac{V_o}{2}$	$V_o - V_{in}$	-	$\frac{V_o}{2}$	$\left(\frac{2}{1+D}\right)V_o$
Passive component	L	1	2	1	1	2	1	3
	C	1	1	3	3	2	5	2

4. Conclusions

The purpose of this work was to develop a new dc/dc boost configuration with high voltage-gain capability for PV converters. The developed configuration consisted of three switches, two diodes, and three inductors. A theoretical analysis of the converter demonstrated its high voltage-gain, low voltage and current stress on its devices, and moderate efficiency. The experimental results obtained were consistent with the theoretical analysis of the converter. To support our results, a comparison with other topologies presented in the literature is provided.

Author Contributions: O.A.-R. designed and performed the simulations and obtained the results; O.A.-R., H.Y.A. and Z.M.A. analyzed the obtained results; O.A.-R. and Z.M.A. wrote the paper, which was further reviewed by H.Y.A. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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