CS 3340 Computer Architecture

More on Cache Memories

Consider the following cache memory organizations:

- A direct-mapped cache with 16 one-word blocks.
- A direct-mapped cache with blocks of size 4-words and a total size of 16 words.
- A 2-way set-associative cache with one word blocks and 8 sets (making a total of 16 words of cache).
- A 4-way set associative cache with 4 sets of 4 words and a total of 16 words of data.

Here are the total number of bits needed to implement the caches above, assuming byte-addressed memories and 32 bit memory addresses with four bytes per word.

For the direct mapped cache with 16 blocks of one word each, the data content is 16*32 bits = 512 bits; the tag fields make up 16*26 bits = 416 bits and there are 16 valid bits, making a total of 944 bits. (If you include "dirty bits" then the total is 944 + 16 = 960 bits.)

For the direct mapped cache with 4 blocks of four words each, the data content is 4*4*32 bits = 512 bits; the tag fields make up 4*26 bits = 104 bits and there are 4 valid bits, making a total of 624 bits. (If you include "dirty bits" then the total is 624 + 4 = 628 bits.)

For the 2-way set associative cache with 8 sets of 2 words, the data content is 8*2*32 bits = 512 bits; the tag fields make up 16*27 bits = 432 and there are 16 valid bits making a total of 960 bits. (If you include "dirty bits" then the total is 960 + 16 = 976 bits.)

For the 4-way set associative cache with 4 sets and 512 bits of data - left to the reader.

Suppose a computer's address size is k bits (using byte addressing), the cache size is S bytes, the block size is B bytes, and the cache is A-way set-associative. Assume that B is a power of 2, so $B = 2^b$. Here are equations for the following quantities in terms of S, B, A, b and k:

1. The number of sets in the cache

Address size:	k bits
Cache size:	S bytes
Block size:	$B = 2^b$ bytes/block
Associativity:	A blocks/set

$$\begin{aligned} \text{Sets/cache} &= \frac{\text{(Bytes/cache)}}{\text{(Blocks/set)} \times \text{(Bytes/block)}} \\ &= \frac{S}{AB} \end{aligned}$$

2. The number of index bits in the address

$$\begin{aligned}\text{Cache set index bits} &= log_2(\text{Sets/cache}) \\ &= log_2\left(\frac{S}{AB}\right) \\ &= log_2\left(\frac{S}{A}\right) - b\end{aligned}$$

3. The number of bits needed to implement the cache.

$$\begin{aligned}\text{Tag address bits/block} &= (\text{Total address bits}) - (\text{Cache set index bits}) \\ &\quad -(\text{Block offset bits}) \\ &= k - \left(log_2\left(\frac{S}{A}\right) - b\right) - b \\ &= k - log_2\left(\frac{S}{A}\right)\end{aligned}$$

Number of bits needed to implement the cache = sets/cache × associativity × (data + tag + valid):

$$\begin{aligned}&= \frac{S}{AB} \times A \times \left(8 \times B + k - log_2\left(\frac{S}{A}\right) + 1\right) \\ &= \frac{S}{B} \times \left(8B + k - log_2\left(\frac{S}{A}\right) + 1\right)\end{aligned}$$