Realistic View

PUBLIC DOMAIN

CC

+5V IN

X1

SILICONVALLEYGARAGE

MAX V CPLD
DEVELOPMENT BOARD

PRELIMINARY

Document Creation Date: 11/11/2025

Design : Vincent Himpe

SILICONVALLEYGARAGE

Breakout Board for ALTERA 5MXXV in TQFP100 package.

Features :

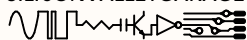On-board USB programmer with external target mode (usb blaster compatible pinning.

Programmer directly supported in Altera Quartus environment 32/64 bit

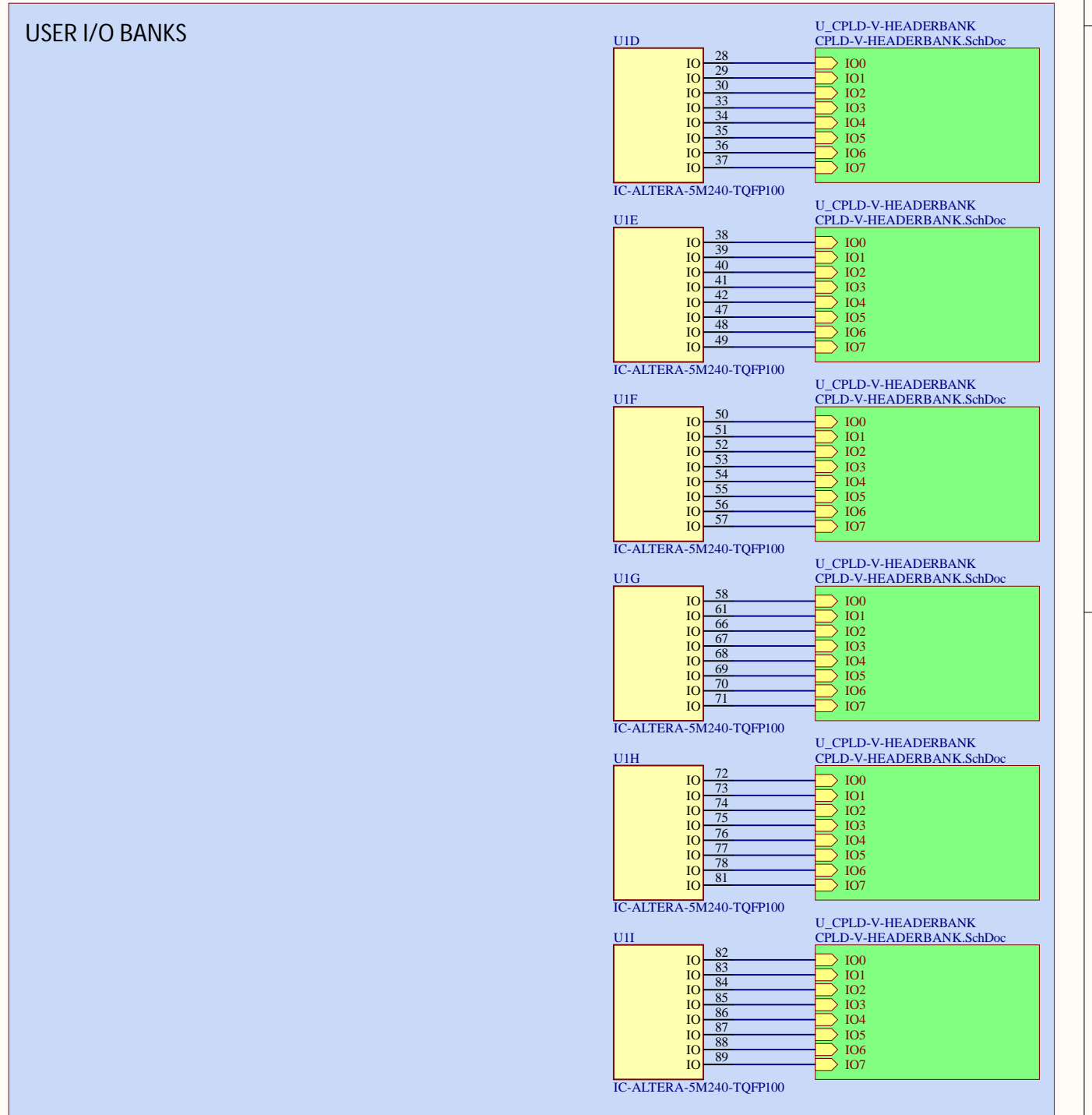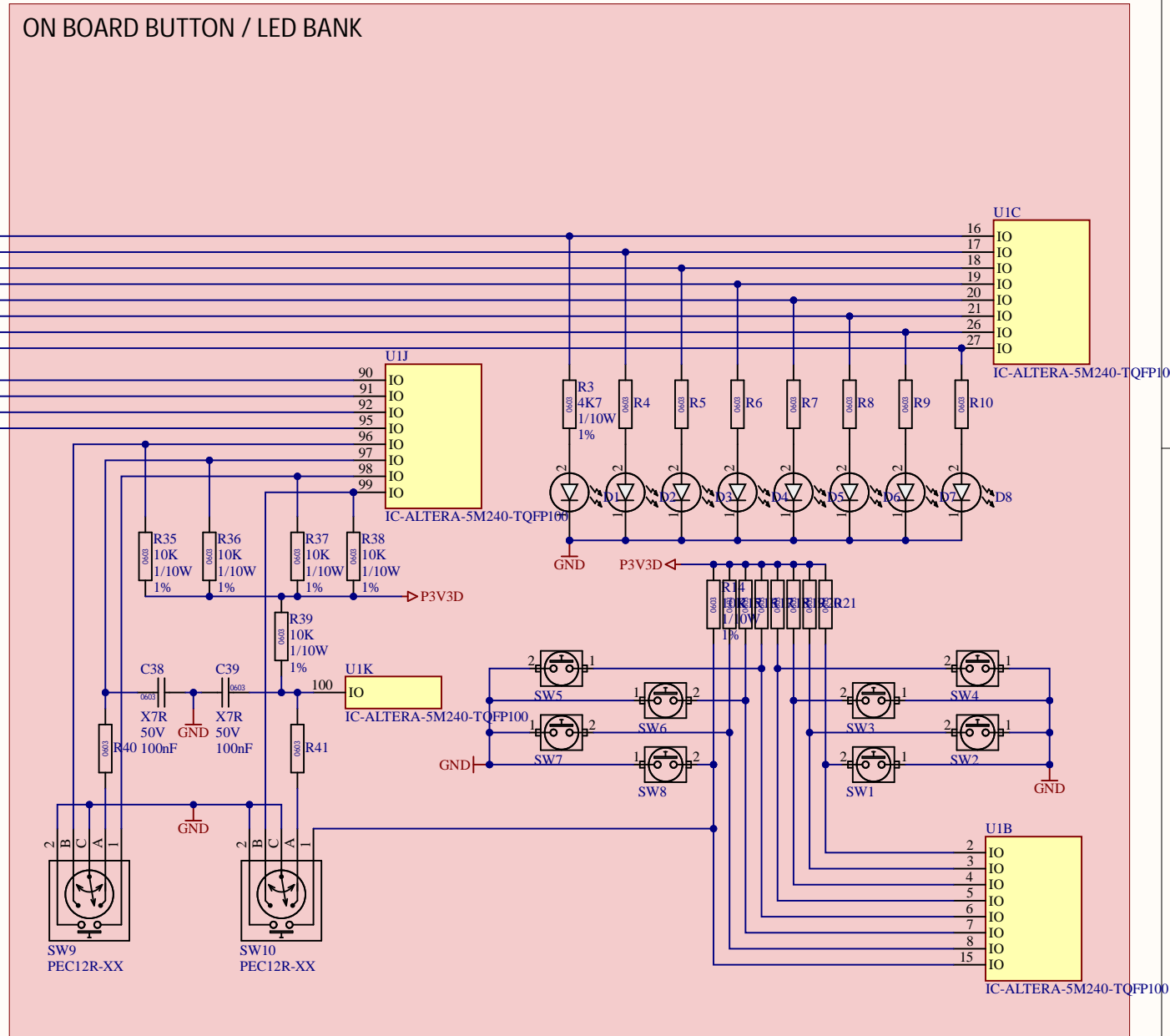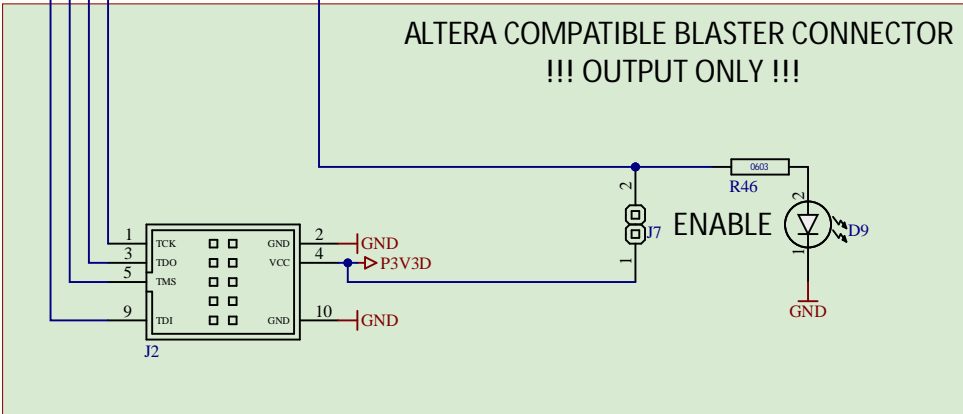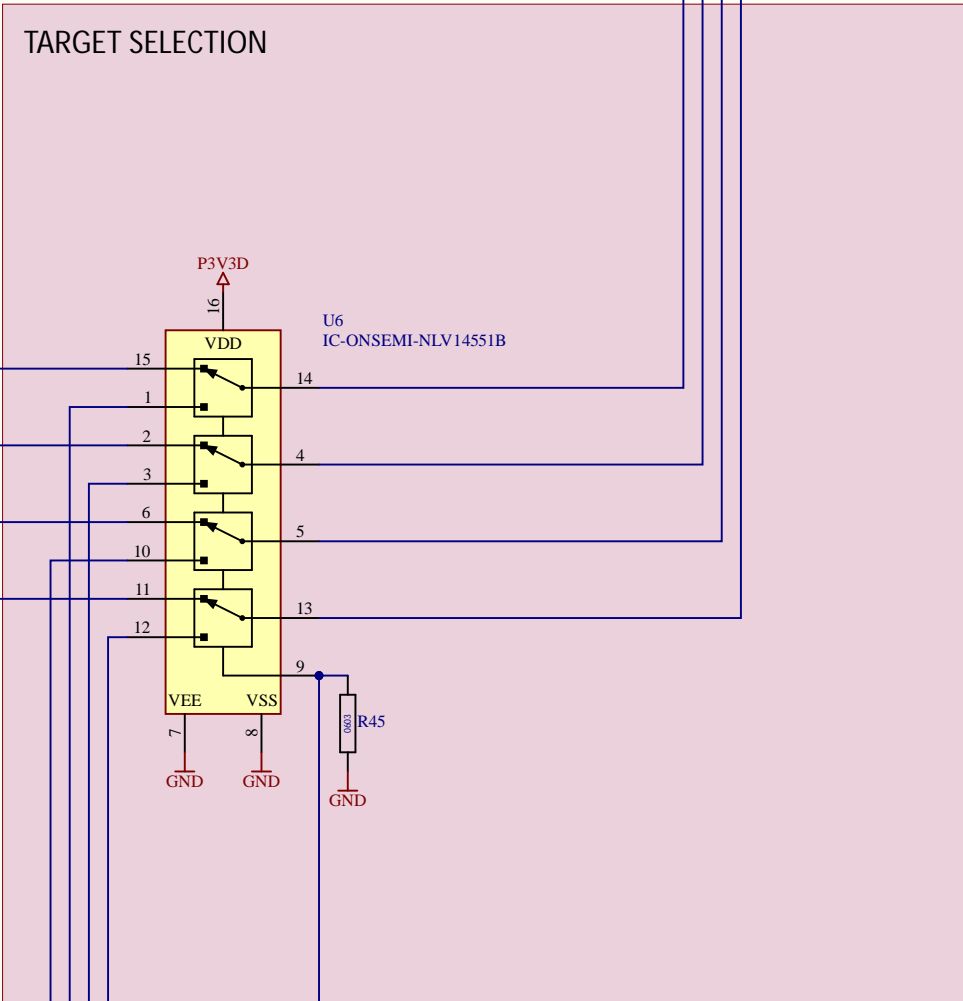Side channel in 245 Async mode for communication with PC application

48 GPIO pin on standard headers for breadboard / dupont style connectors.
Each I/O has extra pin for logic probe

CC O PUBLIC
DOMAIN

CIRCUITSONLINE.NET

SILICONVALLEYGARAGE
Instruments
CPLD-V
Breakout Board

CIRCUITSONLINE.NET

SILICONVALLEYGARAGE
Instruments
CPLD-V
Breakout Board

5V DC INPUT, CENTER POSITIVE

J8
PJ002B
C34 X5R 16V 4u7
C10 X7R 50V 100nF
GND

REGULATORS

U3 NCP1117-3V3
IN OUT P3V3D
GND
R47 4K7 1/10W 1%
D10
GND

C12 X5R 16V 4u7
C13 X5R 16V 4u7
C14 X7R 50V 100nF
C15 X5R 16V 4u7
C16 X5R 16V 4u7
C17 X7R 50V 100nF
GND

U5 NCP1117-1V8
IN OUT P1V8D
GND
C19 X5R 16V 4u7
C20 X5R 16V 4u7
C21 X7R 50V 100nF
C22 X5R 16V 4u7
C23 X5R 16V 4u7
C24 X7R 50V 100nF
GND

J3

CPLD POWER

P1V8D
C28 X5R 16V 4u7
C27 X7R 50V 100nF
C26 X5R 16V 4u7
C25 X7R 50V 100nF

U1A
13 VCCINT GND 1
63 VCCINT GND 10
9 VCCIO1 GND 11
31 VCCIO1 GND 32
45 VCCIO1 GND 46
59 VCCIO2 GND 60
80 VCCIO2 GND 65
94 VCCIO2 GND 79
GND 93
IC-ALTERA-5M240-TQFP100 GND

P3V3D
C37 X5R 16V 4u7
C36 X5R 16V 4u7
C35 X7R 50V 100nF
C33 X7R 50V 100nF
C32 X7R 50V 100nF
C31 X7R 50V 100nF
C30 X7R 50V 100nF
C29 X7R 50V 100nF
GND

PROGRAMMER / COMMUNICATION

P1V8D
C1 X7R 50V 100nF
C2 X7R 50V 100nF
C3 X7R 50V 100nF
C4 X7R 50V 100nF
C5 X7R 50V 100nF
C6 X7R 50V 100nF
C7 X7R 50V 100nF
GND

P3V3D
R1

C8 X5R 16V 4u7
C9 X7R 50V 100nF
GND

J4

D11 PESD2USB5
GND

R2 1K 1/10W 1%
GND

U2
VPHY VPLL RI RO VCORE VCCIO
ASYNC 245 MODE
DP
DM
RESET
ADBUS0 D0 R27
ADBUS1 D1 R28
ADBUS2 D2 R29
ADBUS3 D3 R30
ADBUS4 D4 R31
ADBUS5 D5 R32
ADBUS6 D6 R33
ADBUS7 D7 R34
ACBUS0 RXF
ACBUS1 TXE
ACBUS2 RD
ACBUS3 WR
ACBUS4
ACBUS5
ACBUS6
ACBUS7
MPSSE MODE
BDBUS0 TCK/SK
BDBUS1 TDI/DO
BDBUS2 TDO/DI
BDBUS3 TMCS/CS
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
EECS
EECLK
EEDATA
OSCI
OSCO
REF
TEST
PWREN
SUSPEND
AGND GND

J1

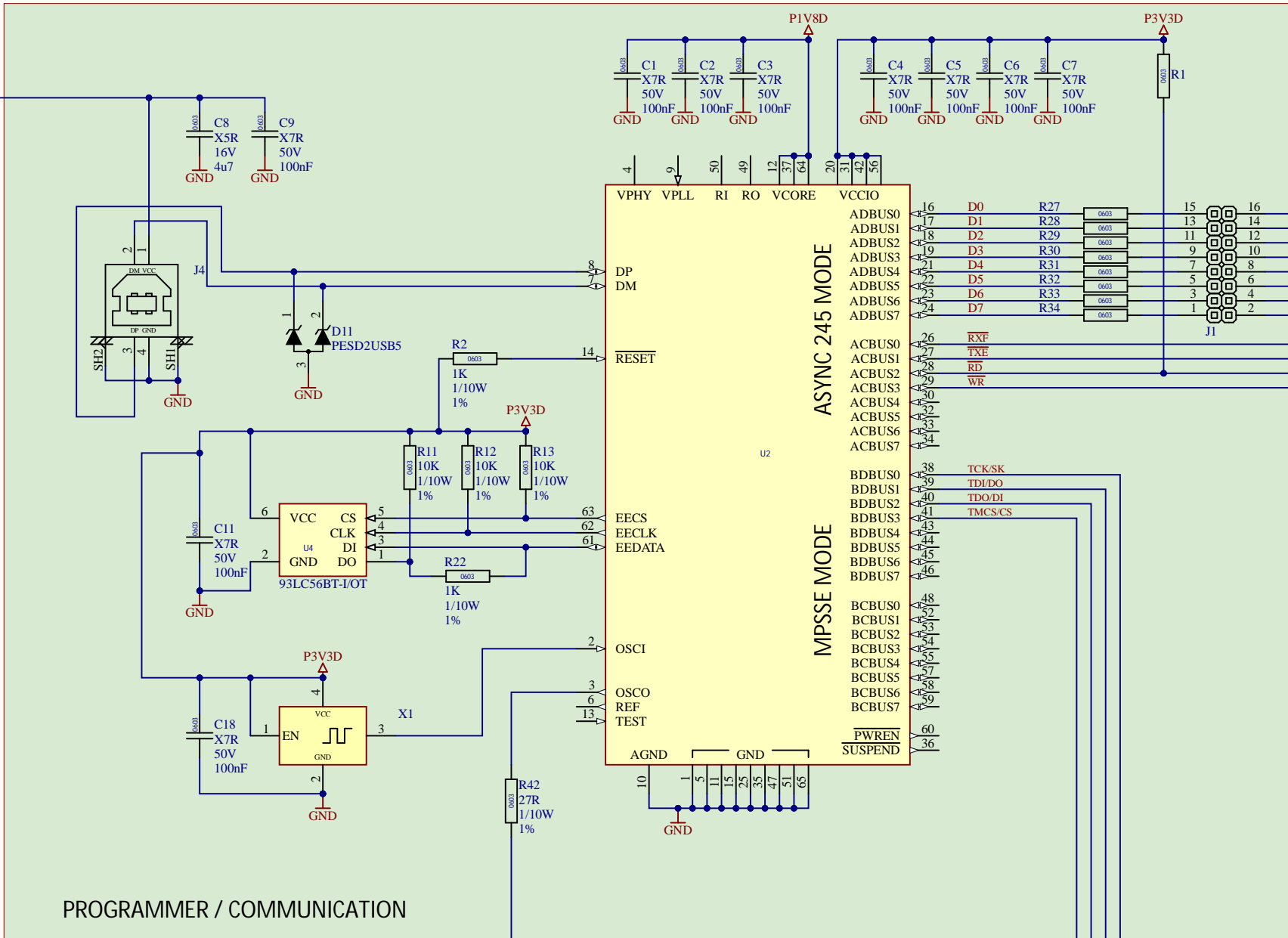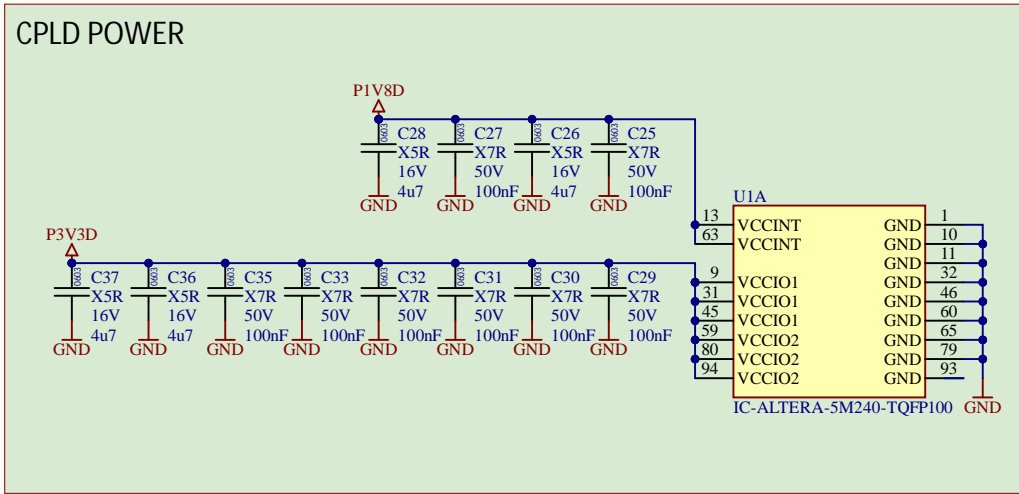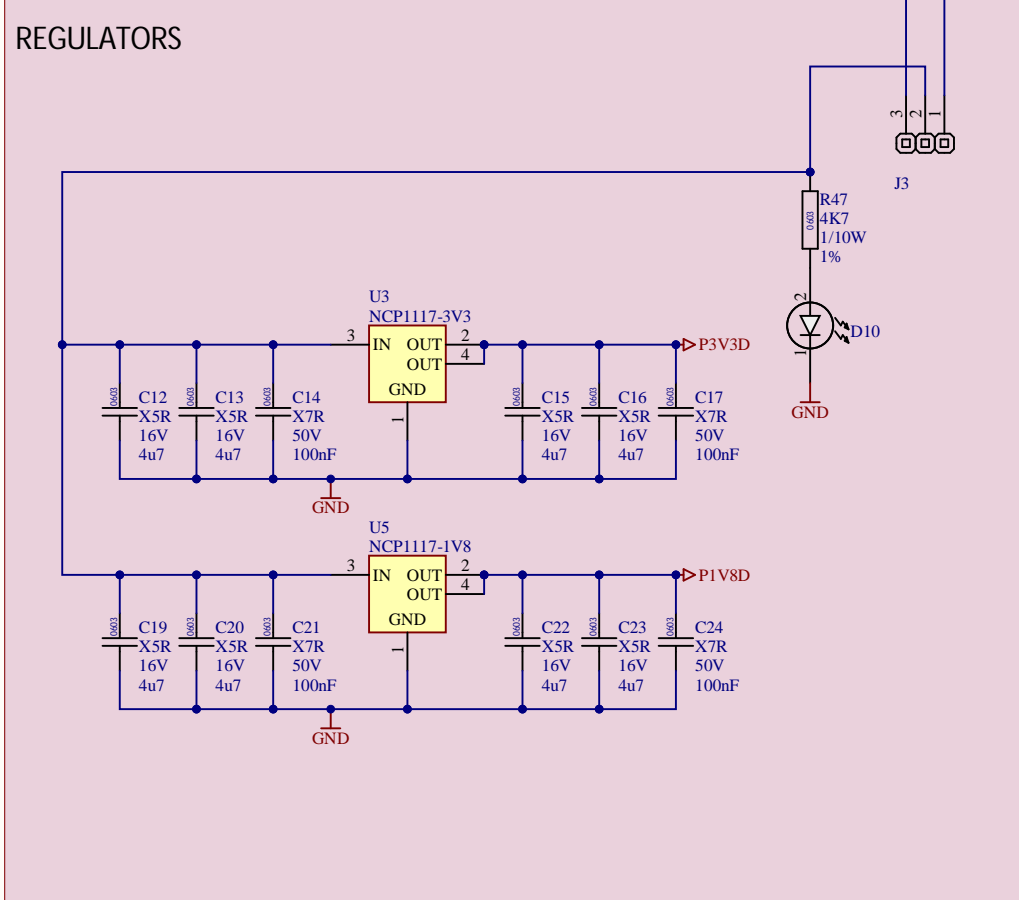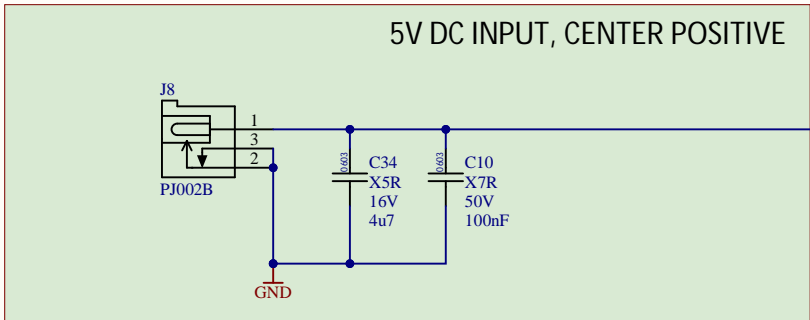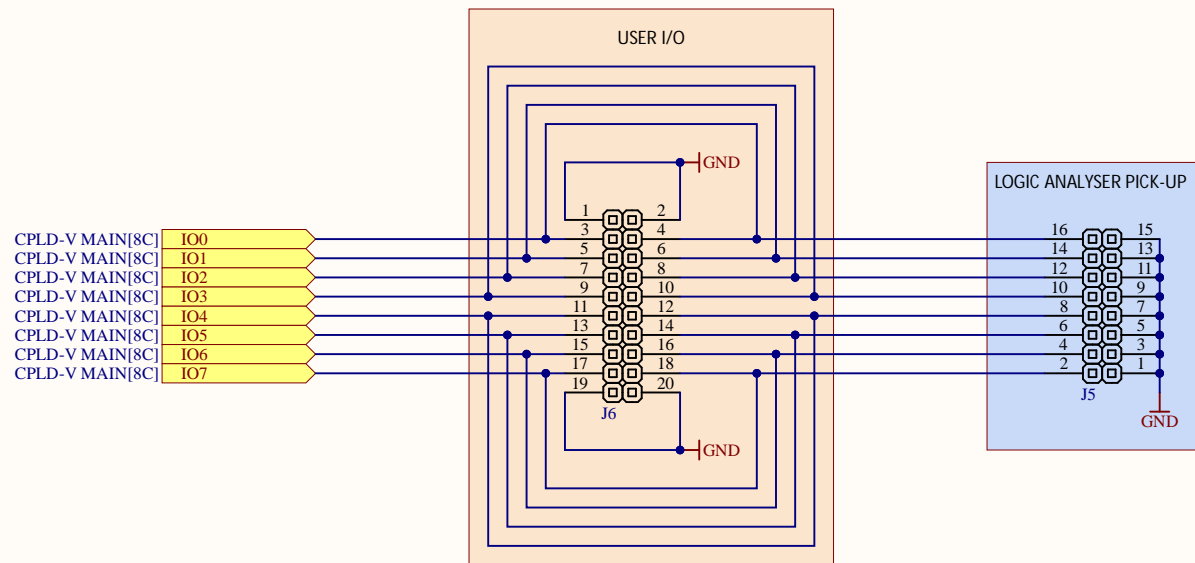R11 10K 1/10W 1%
R12 10K 1/10W 1%
R13 10K 1/10W 1%
P3V3D
GND

U4 93LC56BT-I/OT
VCC CS
CLK
GND DI
DO
R22 1K 1/10W 1%

C11 X7R 50V 100nF
GND

C18 X7R 50V 100nF
GND

X1
EN
VCC
GND

R42 27R 1/10W 1%
GND

JTAG/CLK

U1L
CLK1 DEV_OE
CLK0 DEV_CLR
CLK2
CLK3
TMS
TDO
TDI
TCK
IC-ALTERA-5M240-TQFP100

R43 10K 1/10W 1%
R44 10K 1/10W 1%
P3V3D
R23 10K 1/10W 1%
R24 10K 1/10W 1%
R25 10K 1/10W 1%
R26 10K 1/10W 1%

TARGET SELECTION

P3V3D
U6 IC-ONSEMI-NLV14551B
VDD
VEE VSS
R45
GND GND GND

ALTERA COMPATIBLE BLASTER CONNECTOR
!!! OUTPUT ONLY !!!

J2
TCK GND
TDO
TMS VCC
TDI GND
GND
P3V3D
GND

R46
ENABLE D9
GND

ON BOARD BUTTON / LED BANK

U1C
IO
IC-ALTERA-5M240-TQFP100

U1J
IO
IC-ALTERA-5M240-TQFP100

R3 4K7 1/10W 1%
R4 R5 R6 R7 R8 R9 R10
D8

R35 10K 1/10W 1%
R36 10K 1/10W 1%
R37 10K 1/10W 1%
R38 10K 1/10W 1%
P3V3D

R39 10K 1/10W 1%
U1K
IO 100
IC-ALTERA-5M240-TQFP100

C38 X7R 50V 100nF
C39 X7R 50V 100nF
R40 100nF
R41

SW5 SW4 SW3
SW6 SW7 SW8 SW1 SW2
GND

SW9 PEC12R-XX
SW10 PEC12R-XX
GND

U1B
IO
IC-ALTERA-5M240-TQFP100

USER I/O BANKS

U1D
28 IO IO0
29 IO IO1
30 IO IO2
33 IO IO3
34 IO IO4
35 IO IO5
36 IO IO6
37 IO IO7
IC-ALTERA-5M240-TQFP100
U_CPLD-V-HEADERBANK
CPLD-V-HEADERBANK.SchDoc

U1E
38 IO IO0
39 IO IO1
40 IO IO2
41 IO IO3
42 IO IO4
47 IO IO5
48 IO IO6
49 IO IO7
IC-ALTERA-5M240-TQFP100
U_CPLD-V-HEADERBANK
CPLD-V-HEADERBANK.SchDoc

U1F
50 IO IO0
51 IO IO1
52 IO IO2
53 IO IO3
54 IO IO4
55 IO IO5
56 IO IO6
57 IO IO7
IC-ALTERA-5M240-TQFP100
U_CPLD-V-HEADERBANK
CPLD-V-HEADERBANK.SchDoc

U1G
58 IO IO0
61 IO IO1
66 IO IO2
67 IO IO3
68 IO IO4
69 IO IO5
70 IO IO6
71 IO IO7
IC-ALTERA-5M240-TQFP100
U_CPLD-V-HEADERBANK
CPLD-V-HEADERBANK.SchDoc

U1H
72 IO IO0
73 IO IO1
74 IO IO2
75 IO IO3
76 IO IO4
77 IO IO5
78 IO IO6
81 IO IO7
IC-ALTERA-5M240-TQFP100
U_CPLD-V-HEADERBANK
CPLD-V-HEADERBANK.SchDoc

U1I
82 IO IO0
83 IO IO1
84 IO IO2
85 IO IO3
86 IO IO4
87 IO IO5
88 IO IO6
89 IO IO7
IC-ALTERA-5M240-TQFP100
U_CPLD-V-HEADERBANK
CPLD-V-HEADERBANK.SchDoc

	1	2	3	4

A

B

USER I/O

GND

LOGIC ANALYSER PICK-UP

CPLD-V MAIN[8C]	IO0
CPLD-V MAIN[8C]	IO1
CPLD-V MAIN[8C]	IO2
CPLD-V MAIN[8C]	IO3
CPLD-V MAIN[8C]	IO4
CPLD-V MAIN[8C]	IO5
CPLD-V MAIN[8C]	IO6
CPLD-V MAIN[8C]	IO7

1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20

J6

GND

16 15
14 13
12 11
10 9
8 7
6 5
4 3
2 1

J5

GND

C

SILICONVALLEYGARAGE

Instruments

CPLD-V
Breakout Board

D

	1	2	3	4