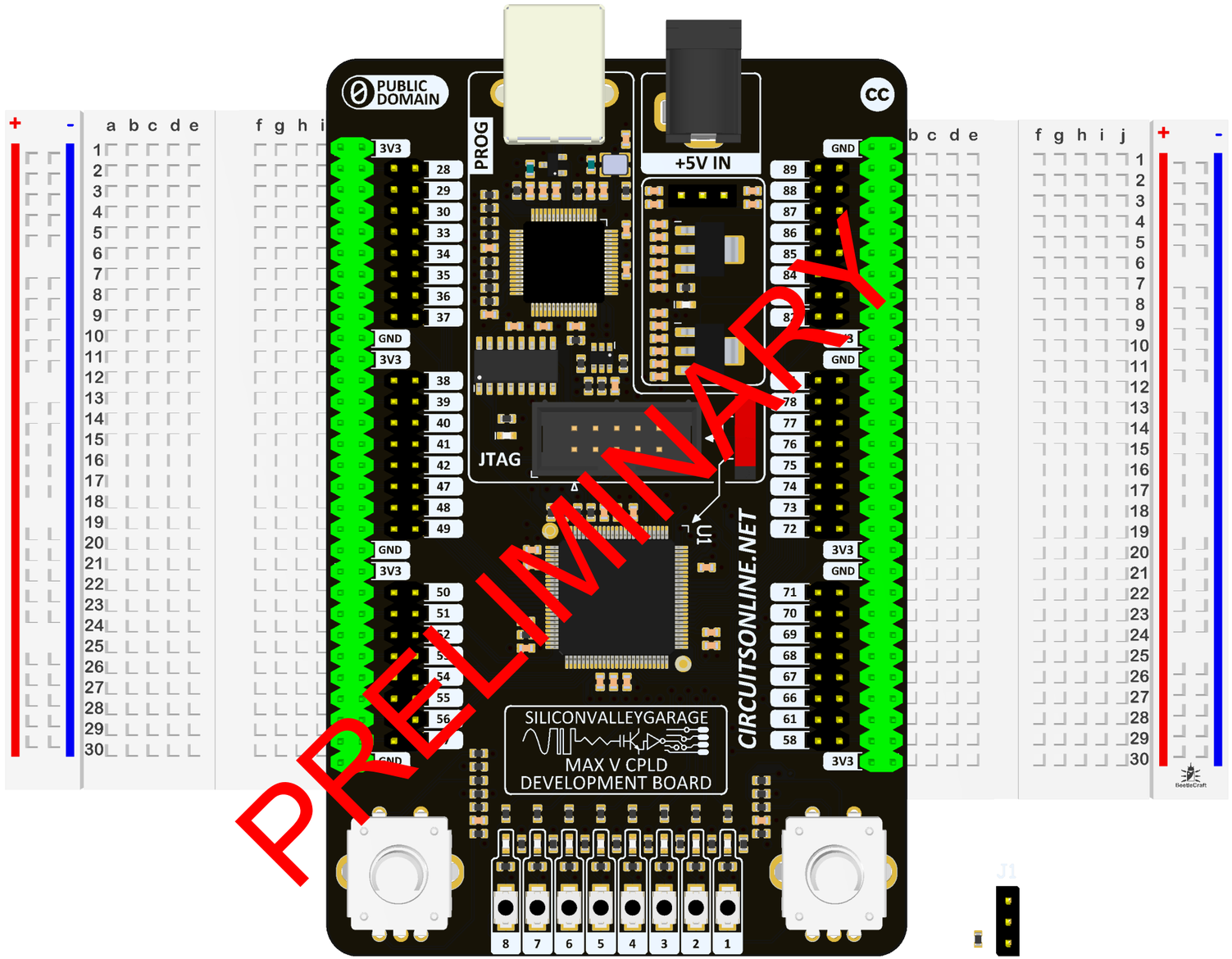
CPLD-V.PrjPcb

Realistic View



Document Creation Date: 11/12/2025

Design : Vincent Himpe

SILICONVALLEYGARAGE

Breakout Board for ALTERA 5MXXV in TQFP100 package.

Features :

On-board USB programmer with external target mode (usb blaster compatible pinning.

Programmer directly supported in Altera Quartus environment 32/64 bit

Side channel in 245 Async mode for communication with PC application

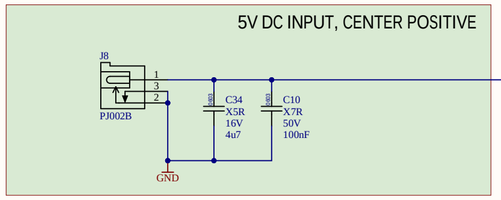
48 GPIO pin on standard headers for breadboard / dupont style connectors.
Each I/O has extra pin for logic probe

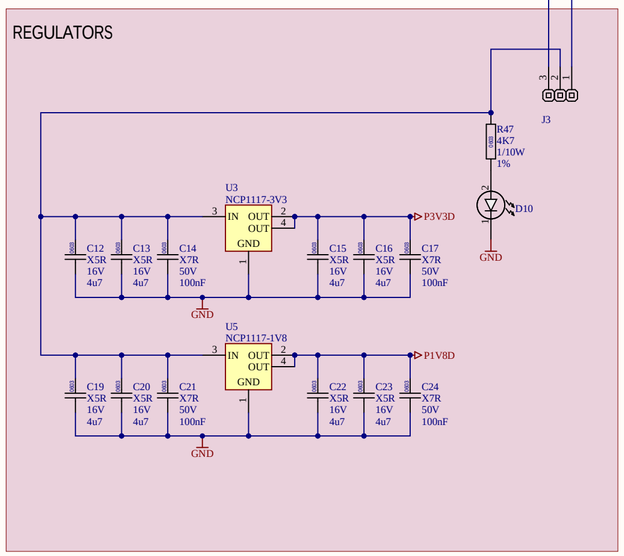
CIRCUITSONLINE.NET

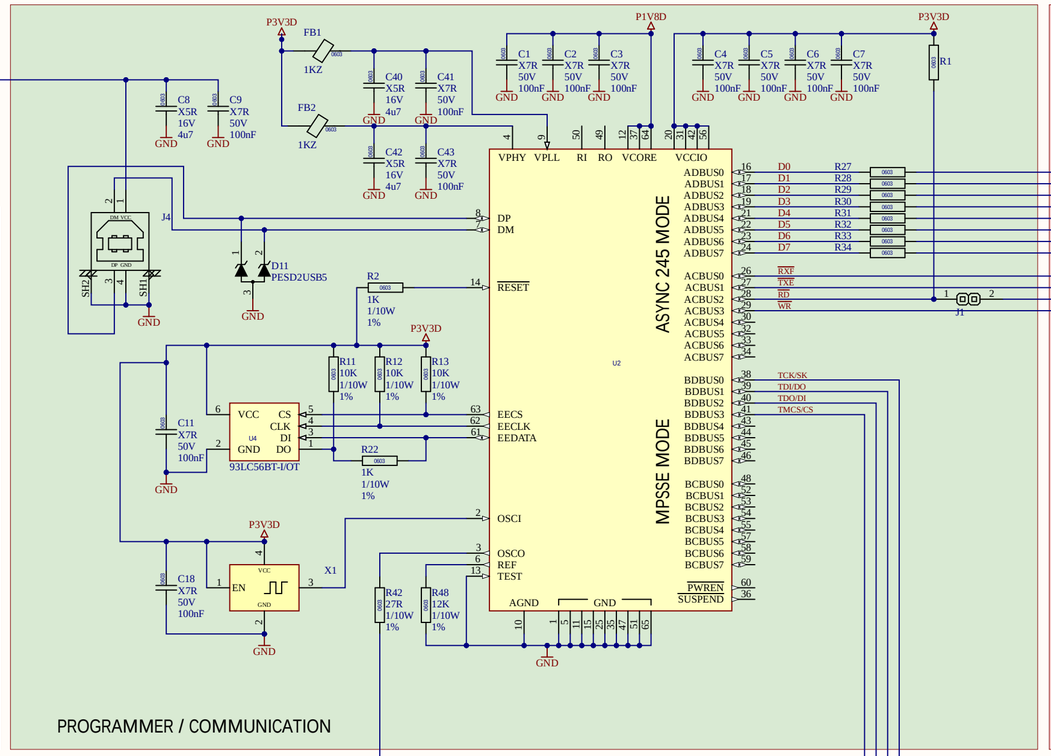
SILICONVALLEYGARAGE
Instruments

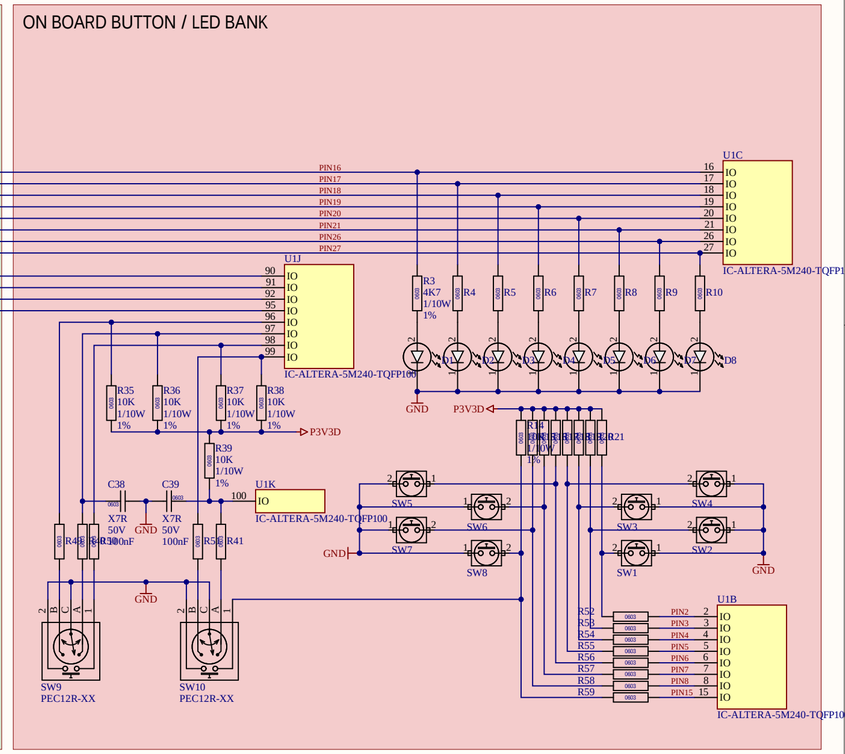
CPLD- V

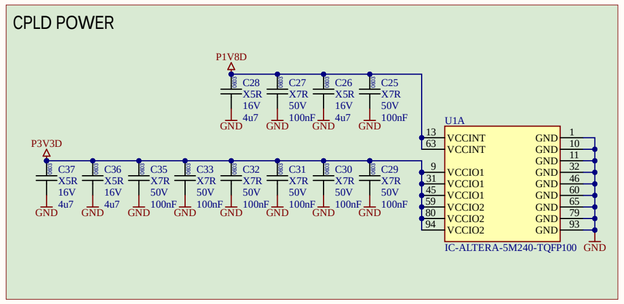
Breakout Board

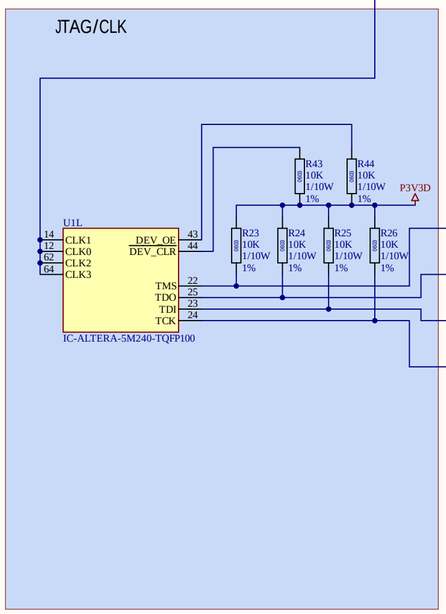


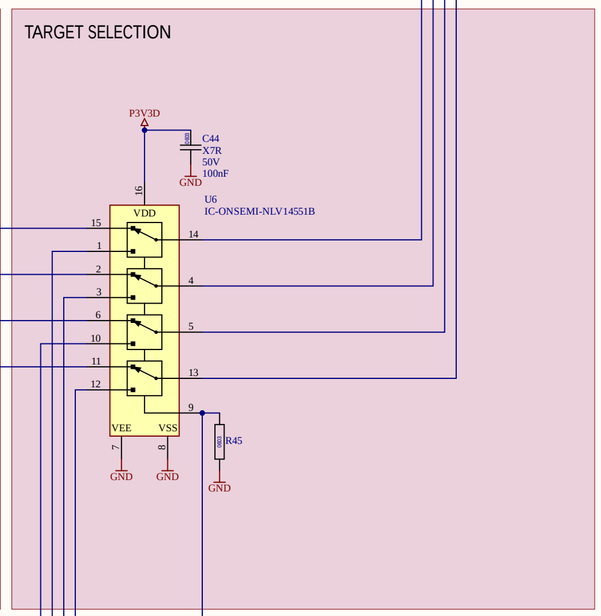


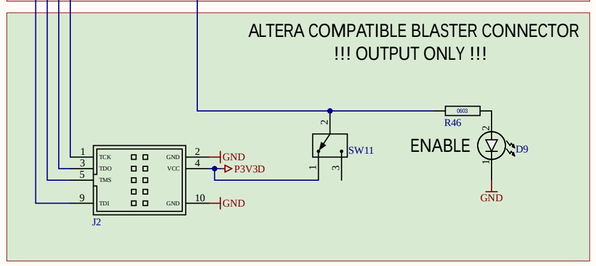


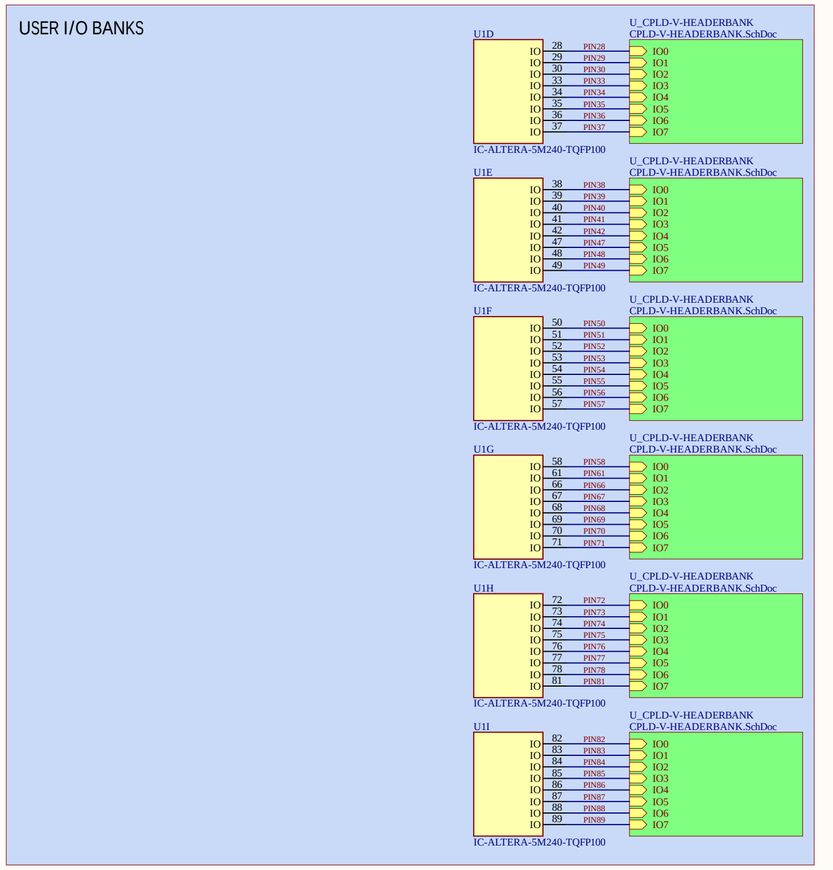










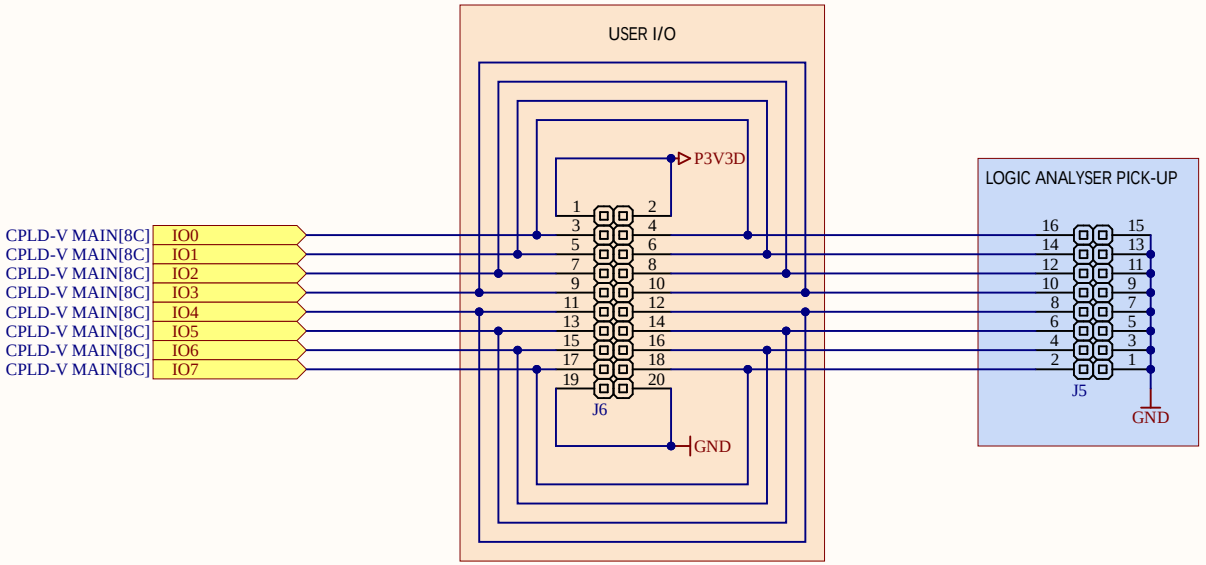


CIRCUITSONLINE.NET

SILICONVALLEYGARAGE Instruments

CPLD-V

Breakout Board



SILICONVALLEYGARAGE

Instruments

CPLD-V

Breakout Board

GENERAL

GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.
3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER
4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2
5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

MATERIALS

7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY

SILICONVALLEYGARAGE

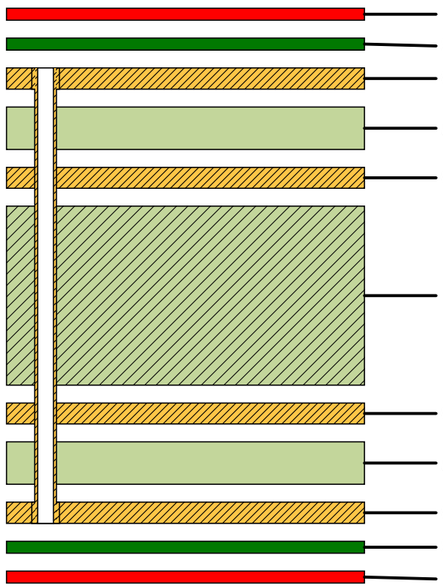
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER STACK

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber	Dk	Weight	Constructions	Df	Resin
	Top Overlay			Legend	GTO					
Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5				
Copper	**Top Layer**	**0.036mm(1.400mil)**		**Signal**	**GTL**		**1oz**			
Prepreg		*0.071mm(2.800mil)*	*PP-006*	*Dielectric*		*4.1*		*1080*	*0.02*	*62%*
CF-004	**Layer 1**	**0.035mm(1.378mil)**		**Signal**	**G1**		**1oz**			
		1.520mm(59.843mil)	*FR-4*	*Dielectric*		*4.8*				
CF-004	**Layer 2**	**0.035mm(1.378mil)**		**Signal**	**G2**		**1oz**			
Prepreg		*0.071mm(2.800mil)*	*PP-006*	*Dielectric*		*4.1*		*1080*	*0.02*	*62%*
Copper	**Bottom Layer**	**0.036mm(1.400mil)**		**Signal**	**GBL**		**1oz**			
Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5				
	Bottom Overlay			Legend	GBO					

Total thickness: 1.824mm(71.799mil)

SILICONVALLEYGARAGE

Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
◇	180	0.500mm(19.685mil)	Plated	Round	Top Layer - Bottom Layer	Via				(Mixed)	(Mixed)
⊠	3	0.800mm(31.496mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✡	4	0.920mm(36.221mil)	Plated	Round	Top Layer - Bottom Layer	Pad	(Mixed)				
□	245	1.000mm(39.370mil)	Plated	(Mixed)	Top Layer - Bottom Layer	Pad	(Mixed)				
○	2	2.300mm(90.551mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
⊠	4	2.600mm(102.362mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
	438 Total										

SILICONVALLEYGARAGE

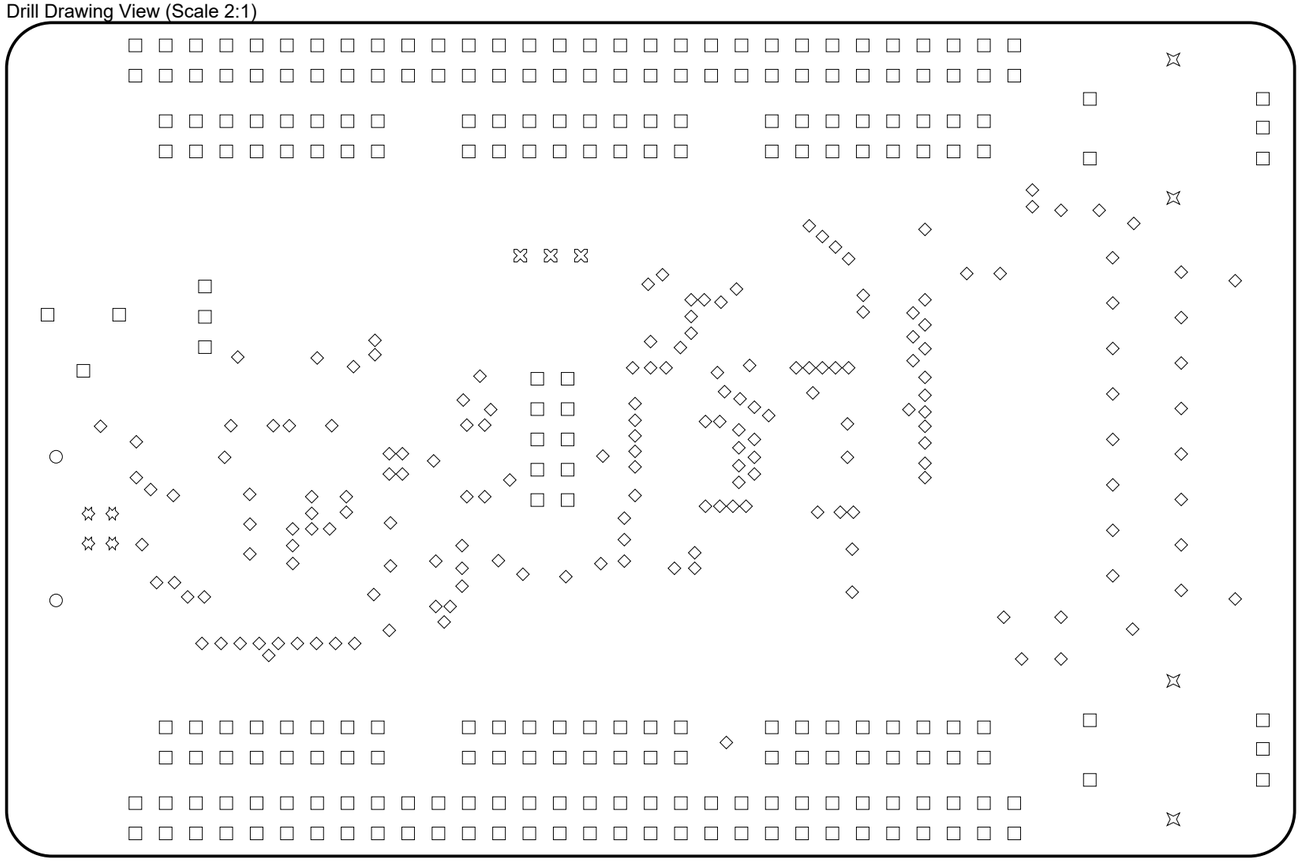
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL DRAWING

Drill Drawing View (Scale 2:1)



SILICONVALLEYGARAGE

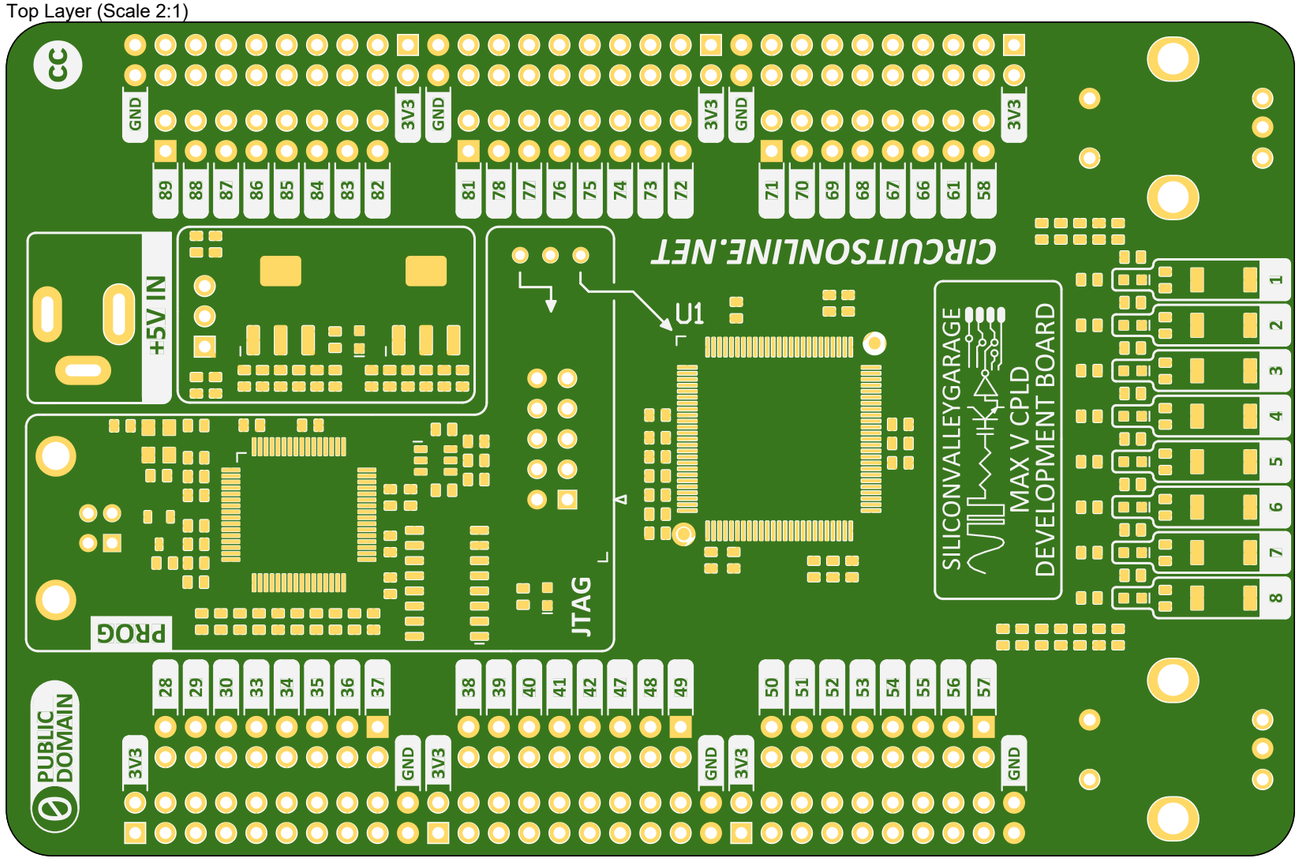
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

COMPOSITE VIEW FRONT

Top Layer (Scale 2:1)



SILICONVALLEYGARAGE

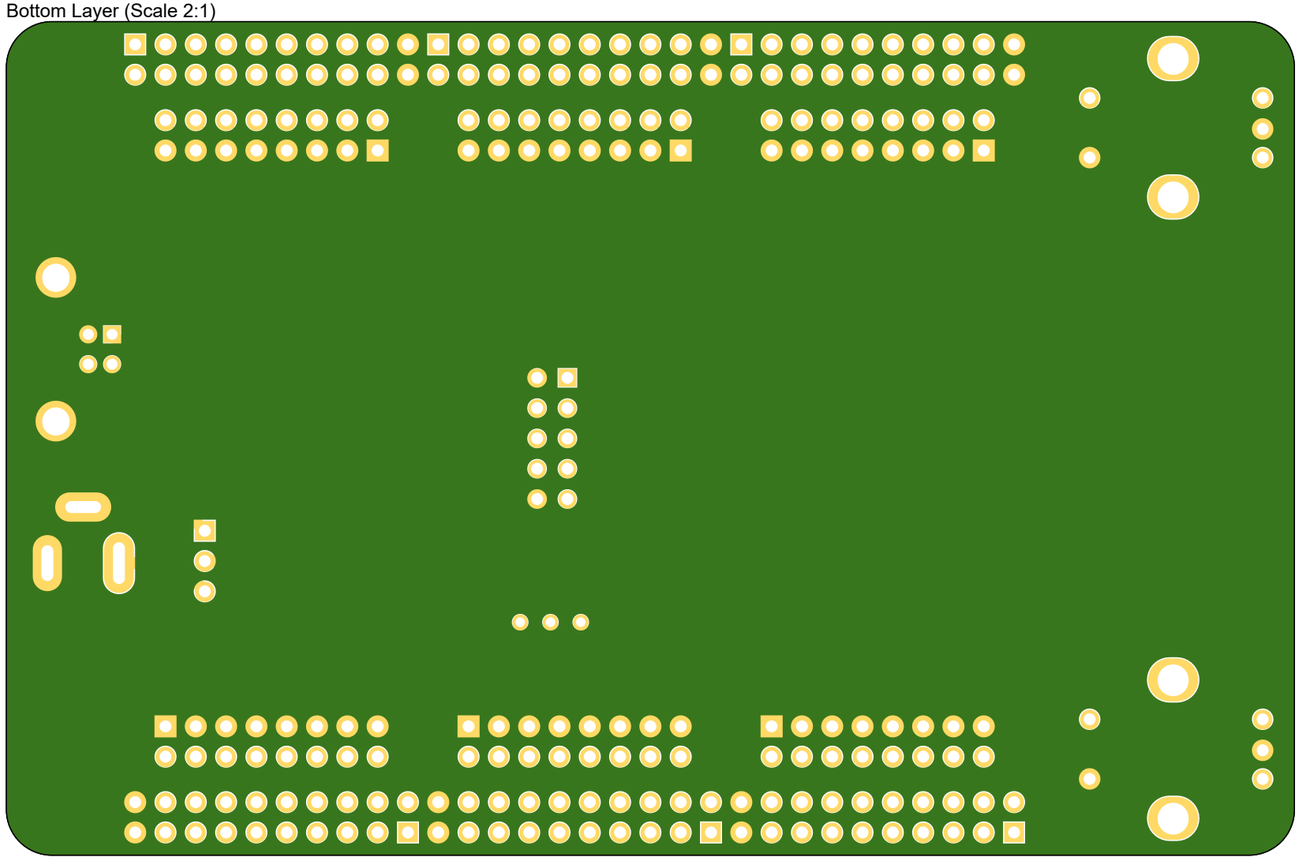
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

COMPOSITE VIEW BACK

Bottom Layer (Scale 2:1)



SILICONVALLEYGARAGE

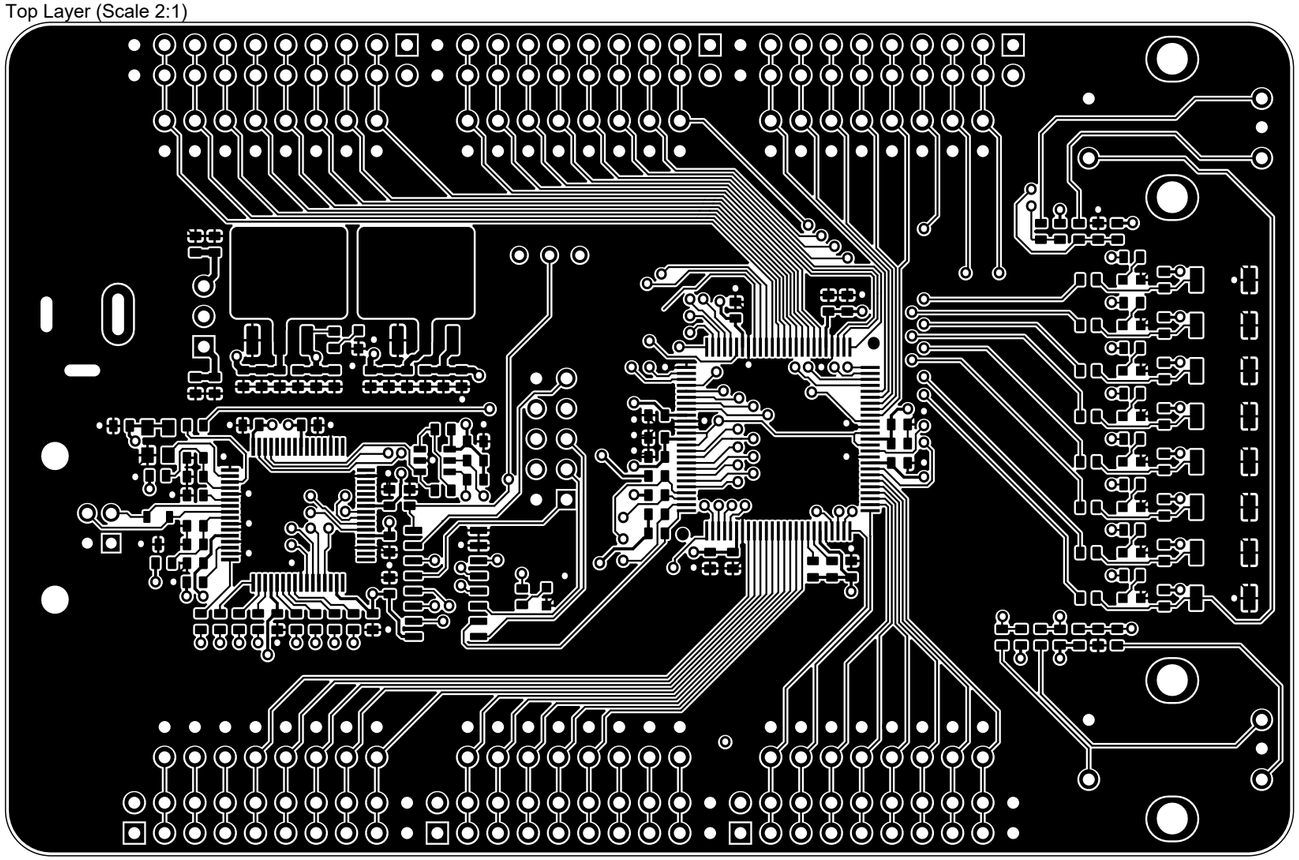
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP LAYER

Top Layer (Scale 2:1)



SILICONVALLEYGARAGE

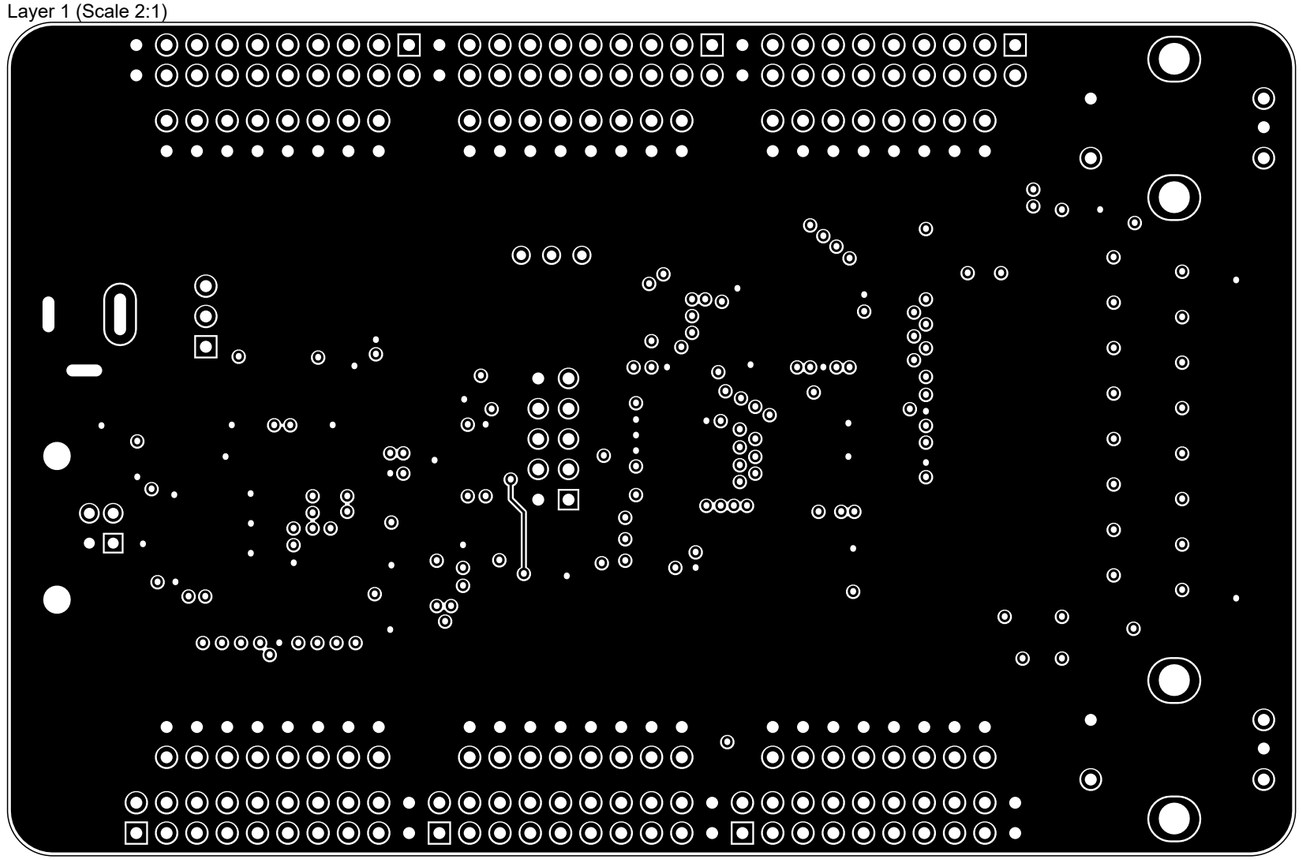
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : MID 1 (GND)

Layer 1 (Scale 2:1)



SILICONVALLEYGARAGE

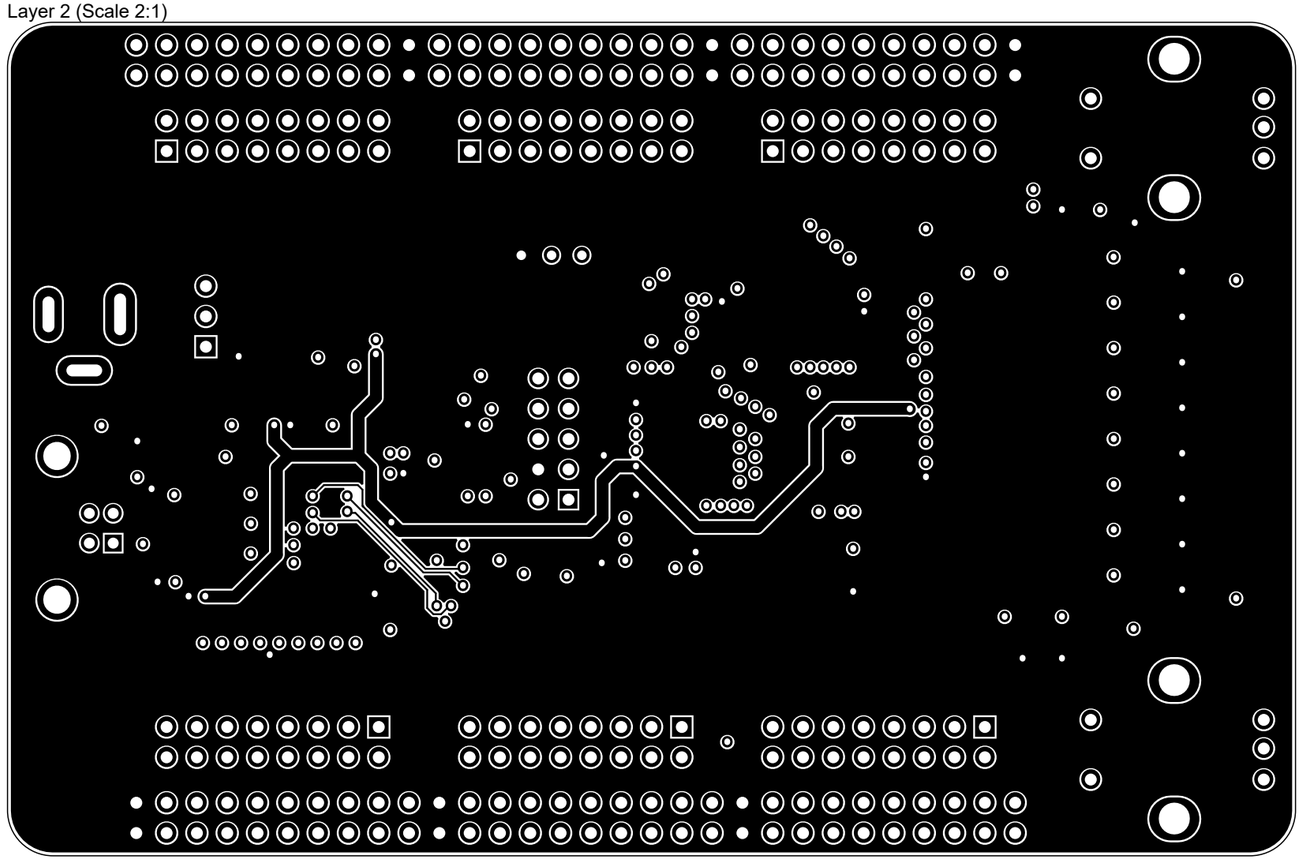
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : MID 2 (POWER)

Layer 2 (Scale 2:1)



SILICONVALLEYGARAGE

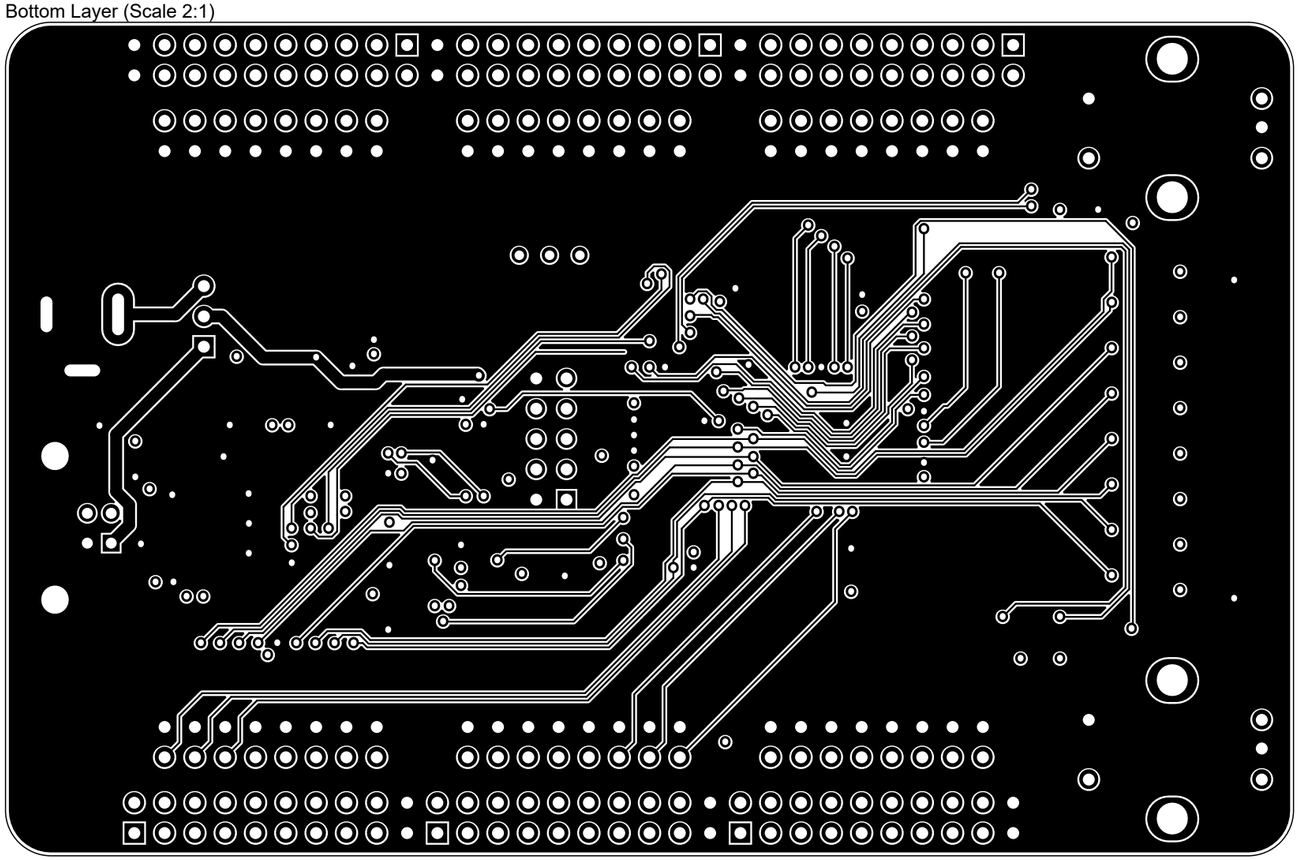
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM LAYER

Bottom Layer (Scale 2:1)



SILICONVALLEYGARAGE

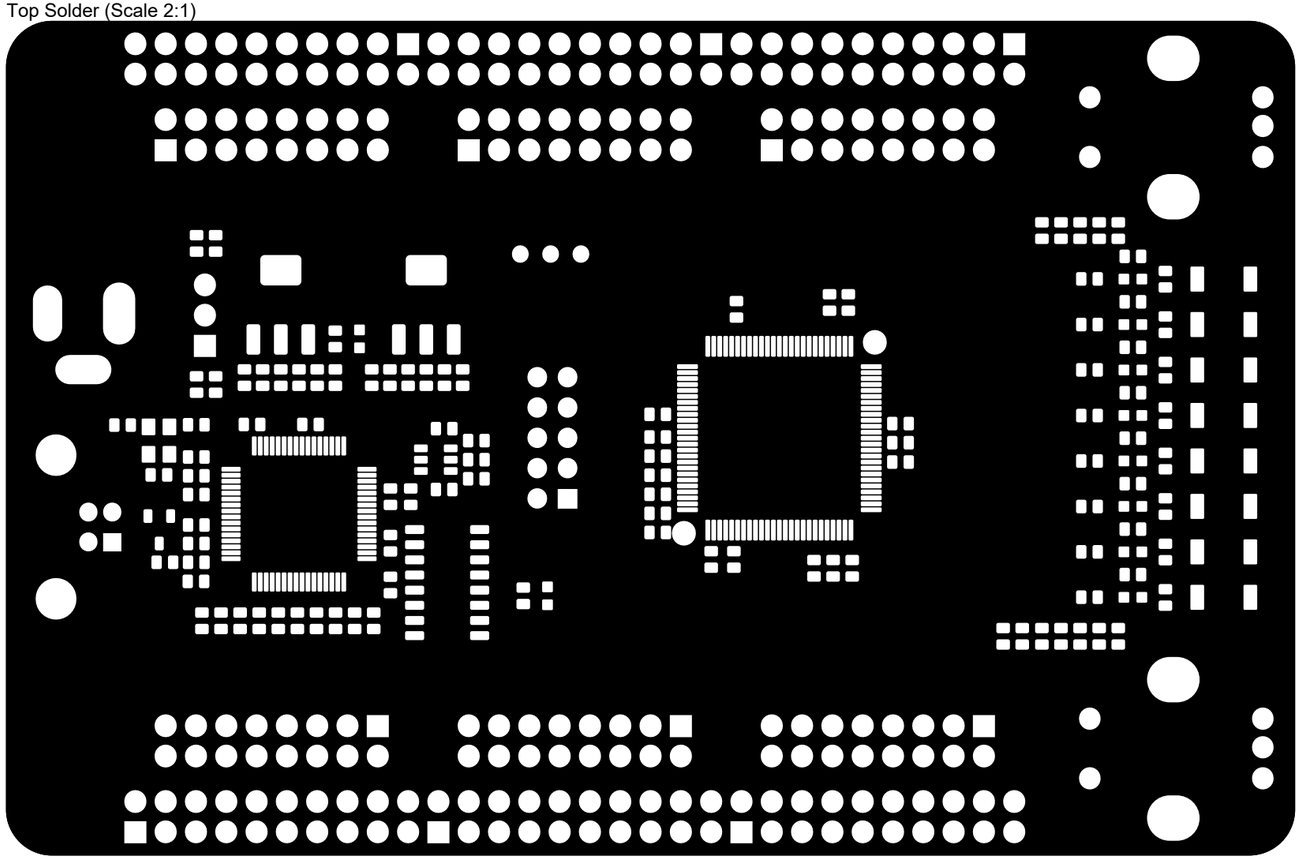
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP SOLDER MASK

Top Solder (Scale 2:1)



SILICONVALLEYGARAGE

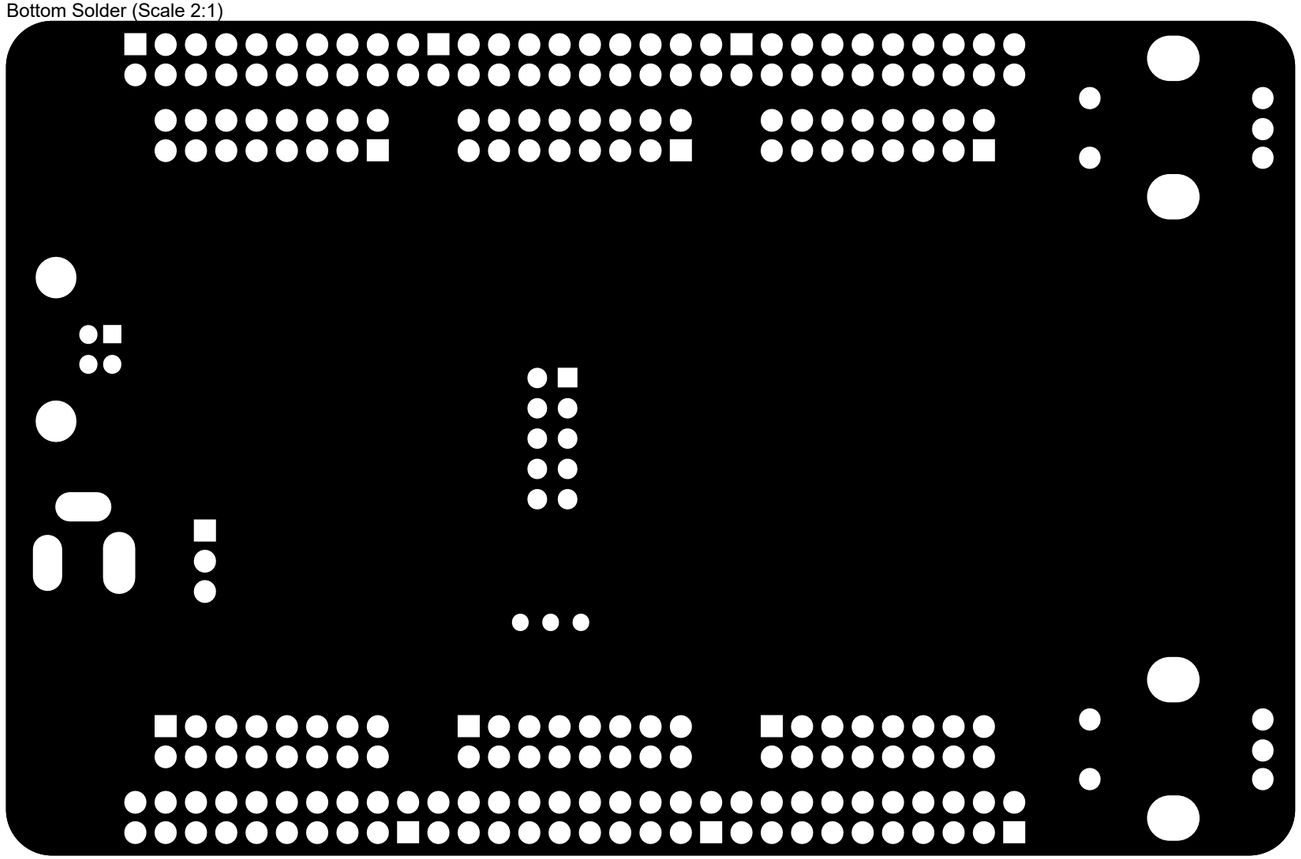
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SOLDER MASK

Bottom Solder (Scale 2:1)



SILICONVALLEYGARAGE

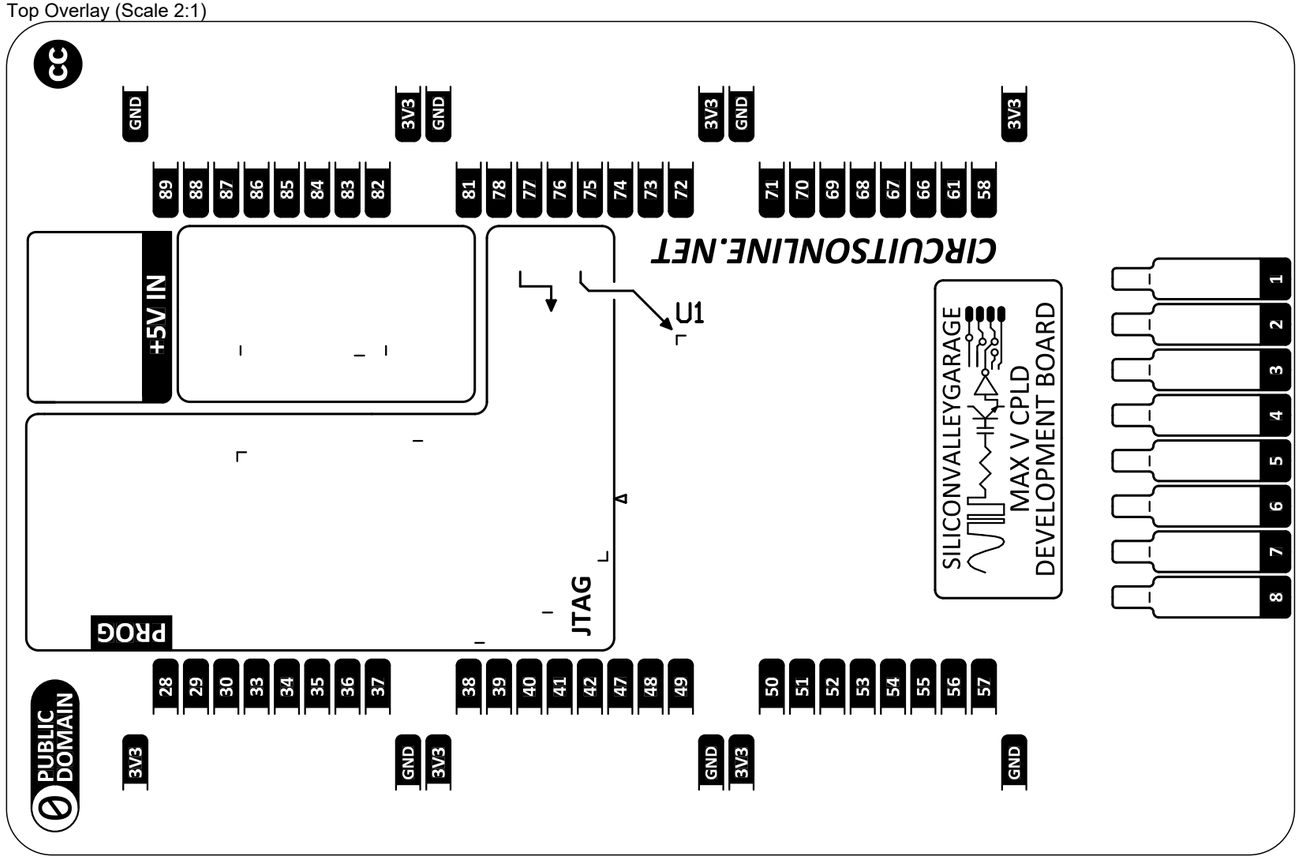
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP SILKSCREEN (LEGEND)

Top Overlay (Scale 2:1)



SILICONVALLEYGARAGE

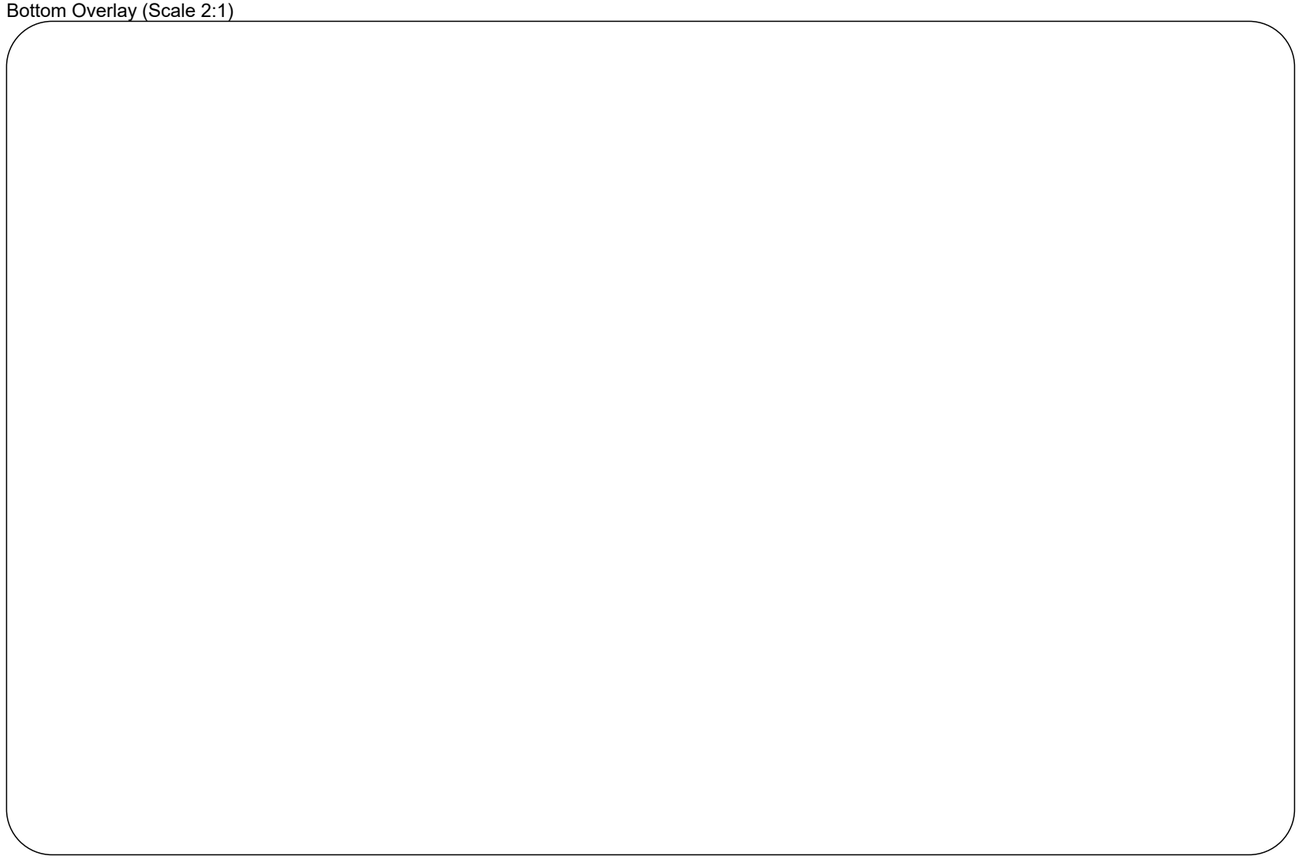
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

Bottom Overlay (Scale 2:1)



SILICONVALLEYGARAGE

Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

GENERAL

Unless otherwise specified the following rules apply:

1. DO NOT DEVIATE FROM ARTWORK OR BOM WITHOUT PRIOR AUTHORIZATION.
2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

Bill of Materials and Material Handling

3. THE BOM CONTAINED IN THIS DOCUMENT IS AS-BUILT. NON-INSTALLED PARTS HAVE BEEN REMOVED. ADDITIONAL BOM FORMATS ARE AVAILABLE IN THE PROJECT FILES
4. ANY PART SUBSTITUTIONS MUST BE APPROVED IN WRITING BEFORE ASSEMBLY
5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
7. ESD CONTROL PER IPC RULES

Soldering

8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
10. SOLDERING PREFERRABLY TO BE DONE USING NITROGEN ATMOSPHERE
11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

SILICONVALLEYGARAGE

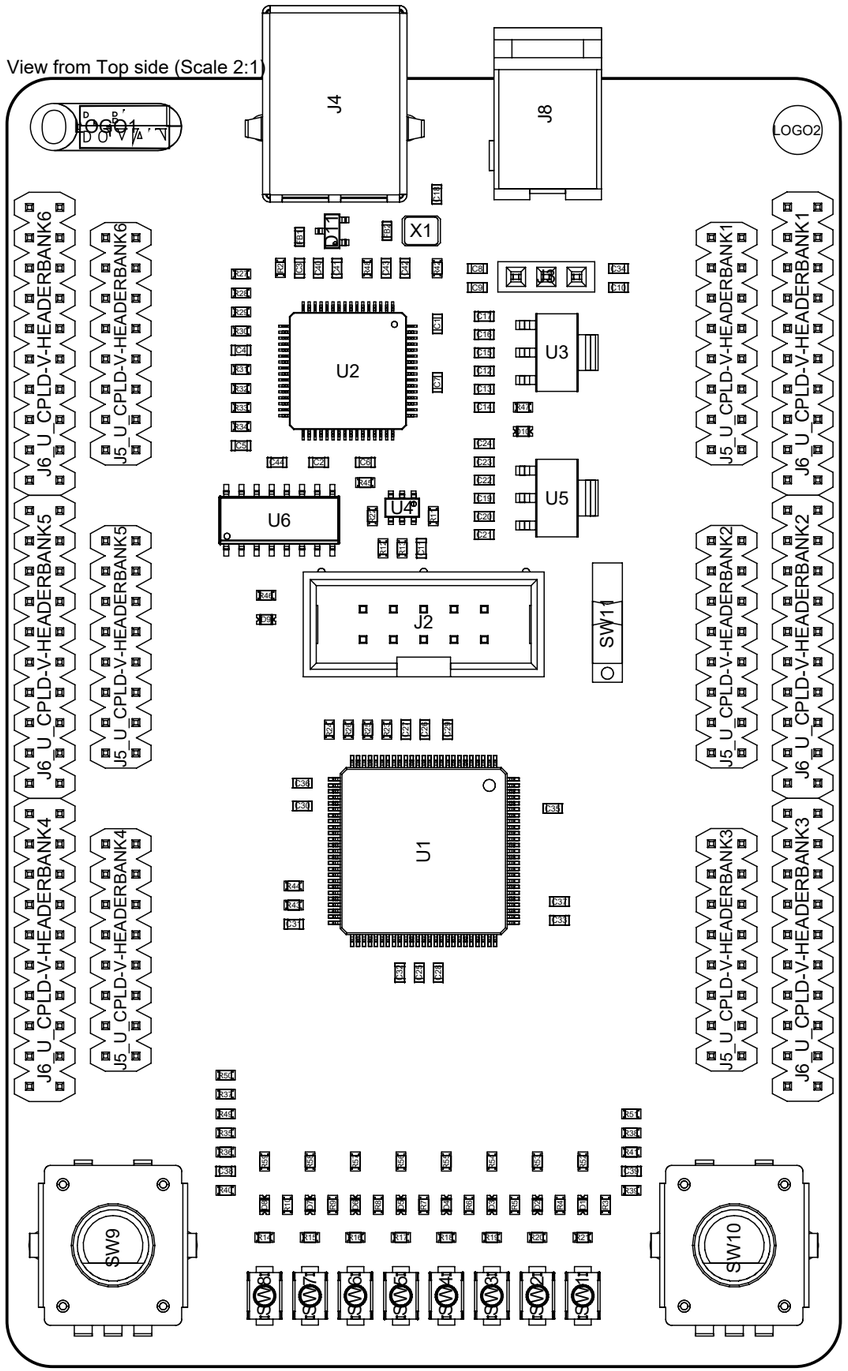
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

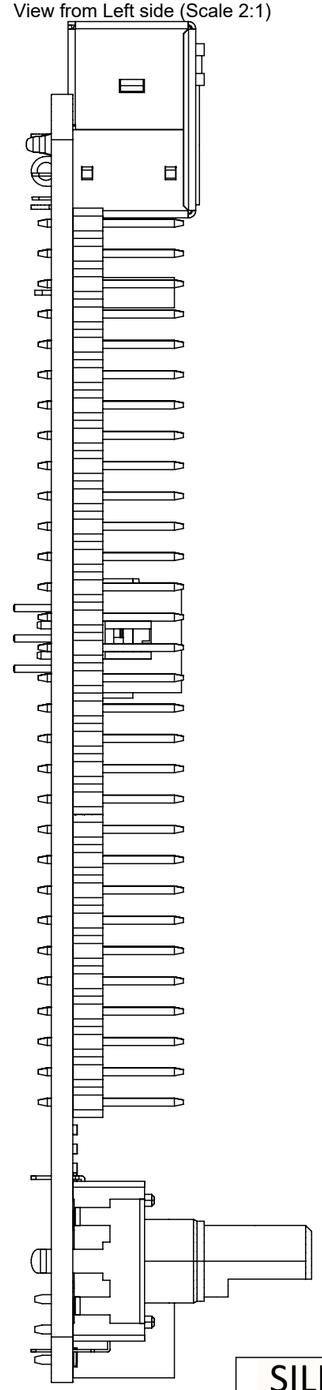
ASSEMBLY DRAWING

2D VIEW

View from Top side (Scale 2:1)



View from Left side (Scale 2:1)



SILICONVALLEYGARAGE

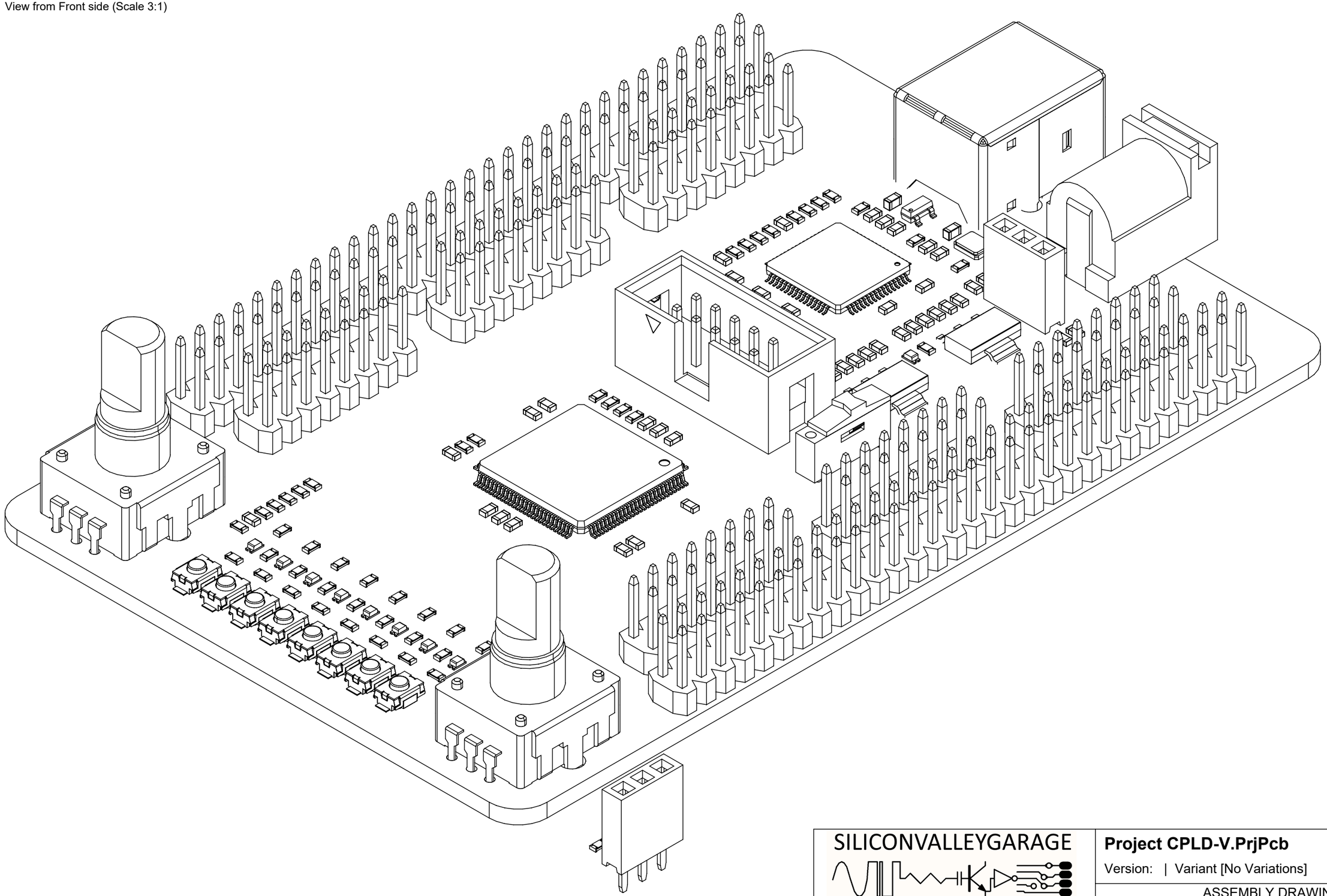
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

3D VIEW

View from Front side (Scale 3:1)



SILICONVALLEYGARAGE

Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

Bill Of Materials

Quantity	Designator	Description	LCSC
28	C1, C2, C3, C4, C5, C6, C7, C9, C10, C11, C14, C17, C18, C21, C24, C25, C27, C29, C30, C31, C32, C33, C35, C38, C39, C41, C43, C44	CAPACITOR,CERAMIC,100nF,50V,X7R,0603	C14663
16	C8, C12, C13, C15, C16, C19, C20, C22, C23, C26, C28, C34, C36, C37, C40, C42	CAPACITOR,CERAMIC,4u7,16V,X5R,0603	C19666
10	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10	LED,SMD,WHITE,42mCd,0603	C2290
1	D11	DIODE,TVS,DUAL,NIDIRETIONAL,USB,PESD2USB5UX-TR,SOT23	C3709087
2	FB1, FB2	FERRITE,1KZ@100MHz,0R2DC,0603	C160982
1	J1	CONN,HEADER,1x2,2.54mm	C429954
1	J2	CONN,BOXHEADER,2X5,ALTERA JTAG PINOUT	
1	J3	CONN,HEADER,1x3,2.54mm	C429954
1	J4	CONN,USB2.0,B,RA,BLUE	C720549
6	J5_U_CPLD-V-HEADERBANK1, J5_U_CPLD-V-HEADERBANK2, J5_U_CPLD-V-HEADERBANK3, J5_U_CPLD-V-HEADERBANK4, J5_U_CPLD-V-HEADERBANK5, J5_U_CPLD-V-HEADERBANK6	CONN,HEADER,2X8,2.54mm	C42431826
6	J6_U_CPLD-V-HEADERBANK1, J6_U_CPLD-V-HEADERBANK2, J6_U_CPLD-V-HEADERBANK3, J6_U_CPLD-V-HEADERBANK4, J6_U_CPLD-V-HEADERBANK5, J6_U_CPLD-V-HEADERBANK6	CONN,HEADER,2X10,2.54mm	C5383109
1	J8	CONN,DCPOWER,BARREL,CUI,PJ002B	
24	R1, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R23, R24, R25, R26, R35, R36, R37, R38, R39, R43, R44, R45	RESISTOR,10K,1%,100mW,0603 (1608)	C25804
2	R2, R22	RESISTOR,1K,1%,100mW,0603 (1608)	C21190
10	R3, R4, R5, R6, R7, R8, R9, R10, R46, R47	RESISTOR,4K7,1%,100mW,0603 (1608)	C23162
21	R27, R28, R29, R30, R31, R32, R33, R34, R40, R41, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59	RESISTOR,470R,1%,100mW,0603 (1608)	C23179
1	R42	RESISTOR,27R,1%,100mW,0603 (1608)	
1	R48	RESISTOR,12K,1%,100mW,0603 (1608)	
8	SW1, SW2, SW3, SW4, SW5, SW6, SW7, SW8	SWITCH,TACT,SMD,2PIN,SMT,TOP ACTUATOR	C720477
2	SW9, SW10	SWITCH,ENCODER+CLICK,BOURNS,PEC12R-4120F-S0012	
1	SW11	SWITCH-WURTH-450301014042	
1	U1	IC,LOGIC,CPLD,ALTERA,5M240-TQFP100	
1	U2	IC,XCVR.USB USART.DUAL,FTDI,FT2232H,QFP64	C193662
1	U3	IC,VOLTAGE REG,LIN,POSITIVE,3V3,SOT223	
1	U4	IC,EEPROM,2KBIT,MICROWIRE	C190271
1	U5	IC,VOLTAGE REG,LIN,POSITIVE,1V8,SOT223	
1	U6	IC,ANALOG,4PDT ANALOG SWITCH,ONSEMI,NLV14551	
1	X1	XOSC,12MHz,3225	C49207924

SILICONVALLEYGARAGE

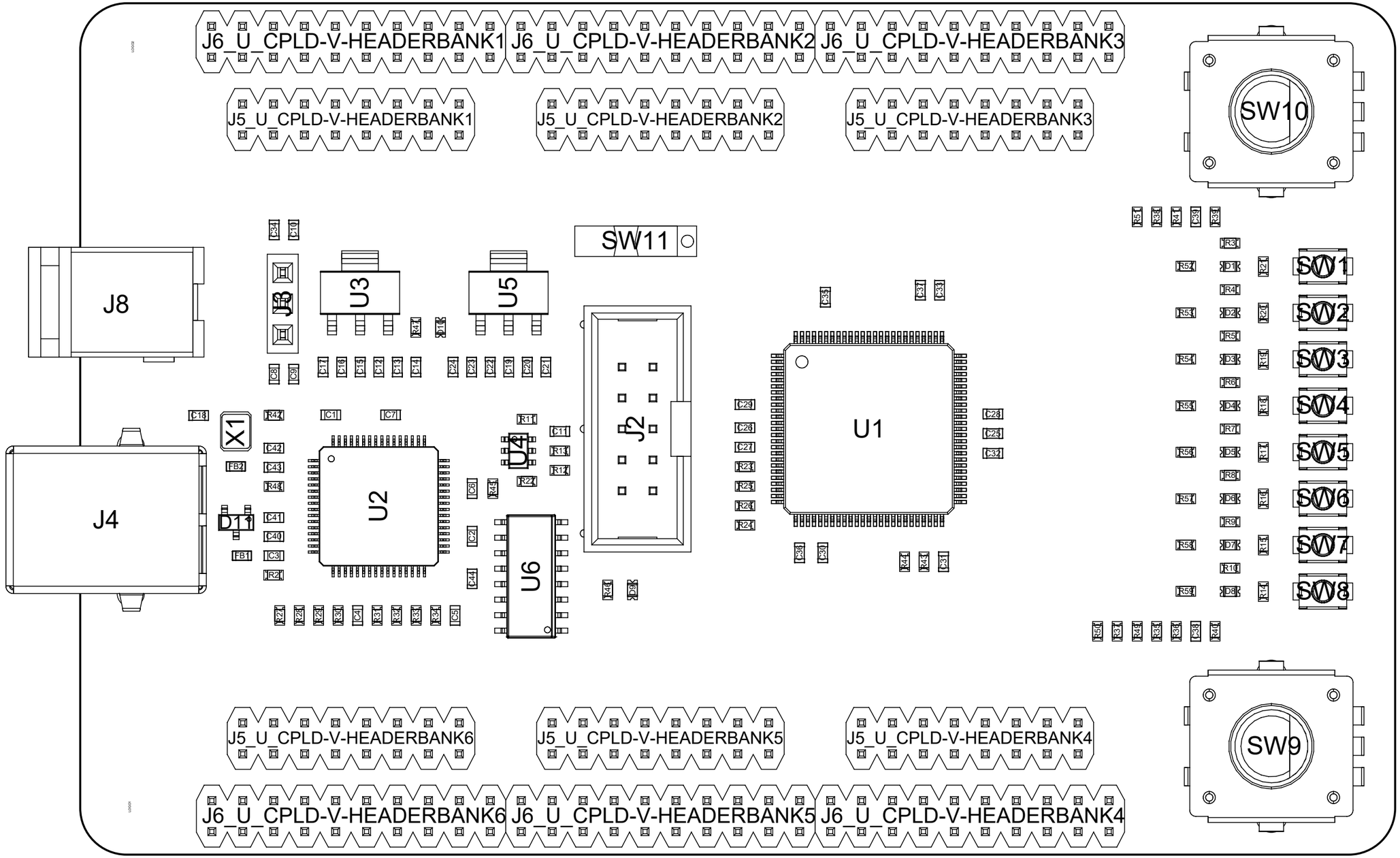
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

DESIGNATORS FRONT

View from Top side (Scale 3:1)



SILICONVALLEYGARAGE

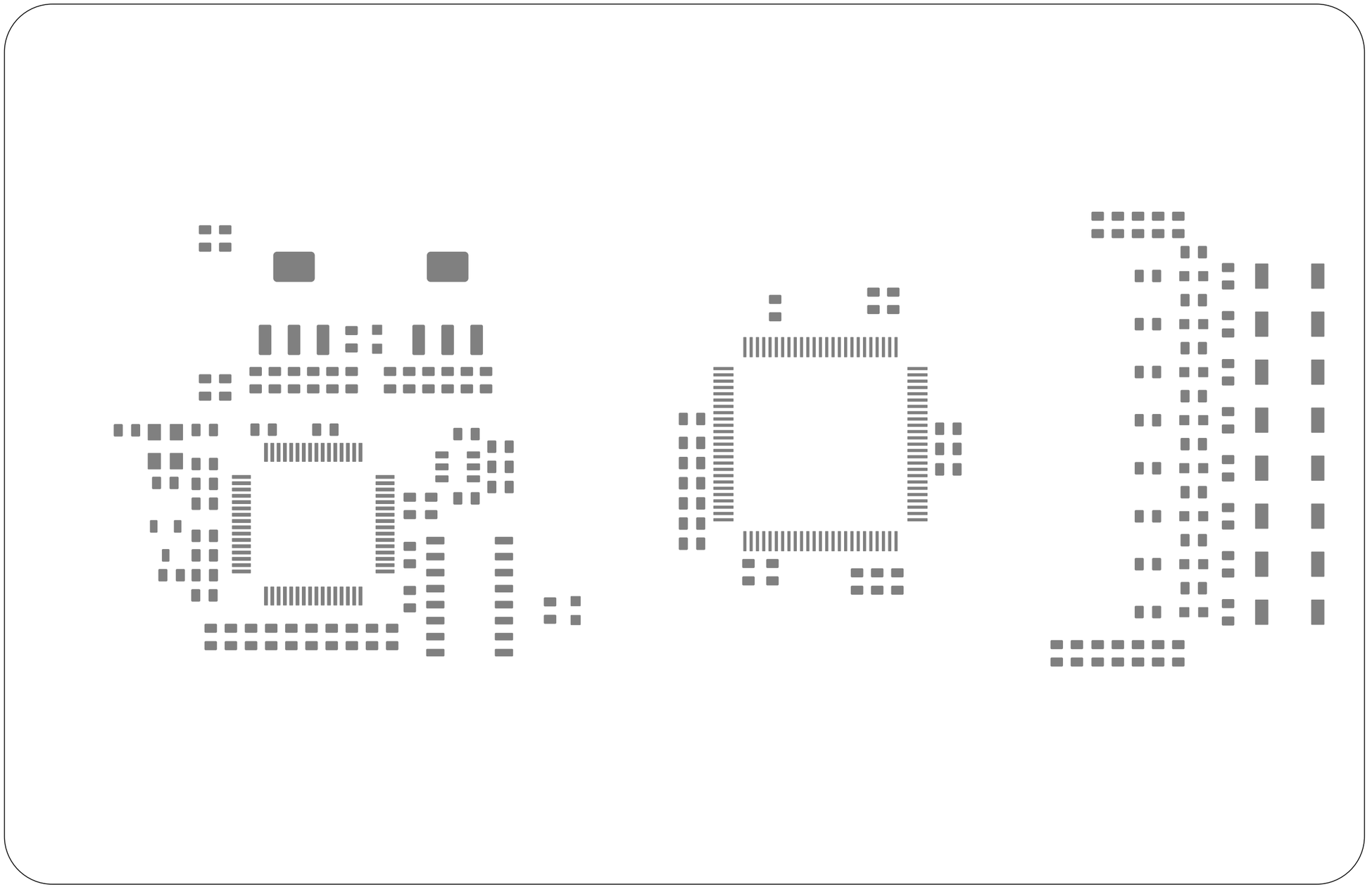
Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

PASTE MASK TOP

Top Paste (Scale 3:1)



SILICONVALLEYGARAGE

Project CPLD-V.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING