

1

2

3

4

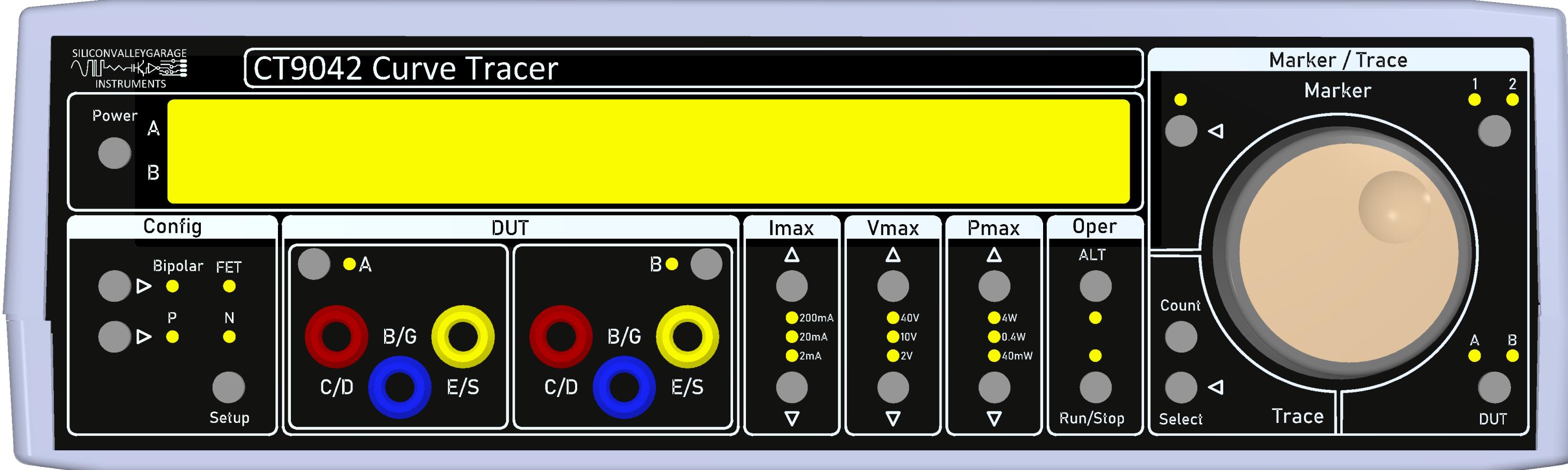
5

6

# CT9042.PrjPcb

A

Realistic View



A

B

B

C

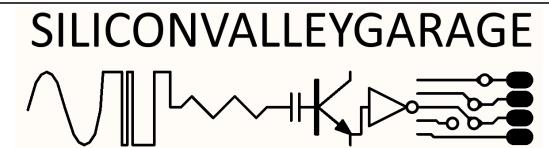
C

D

D

Document Creation Date: 8/27/2025

Design : free\_electron



1

2

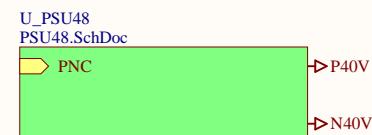
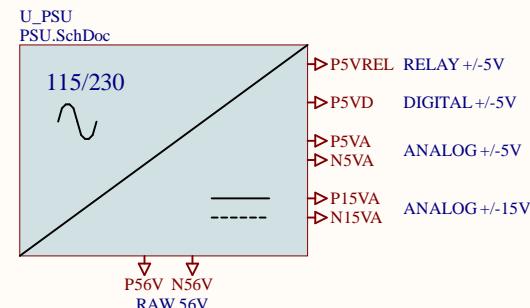
3

4

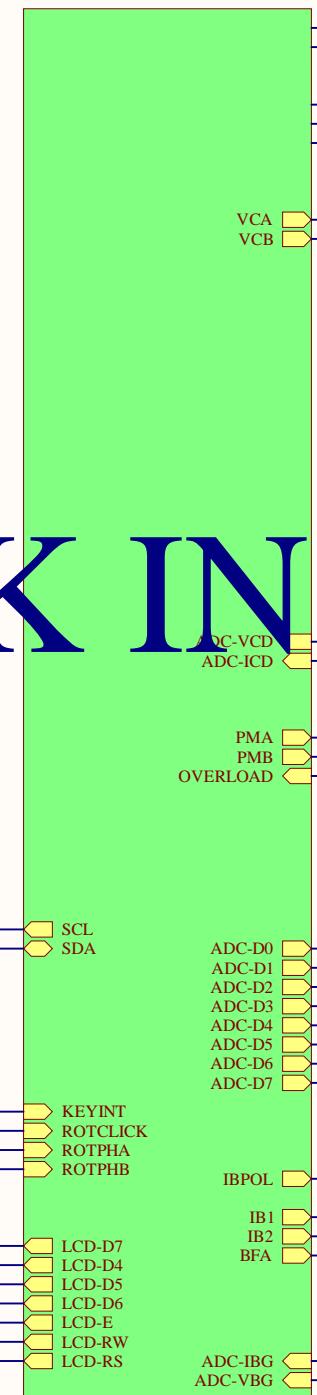
5

6

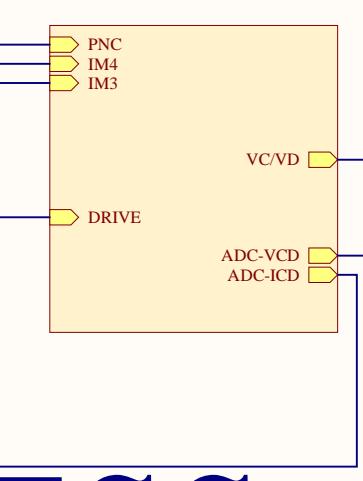
1 2 3 4 5 6



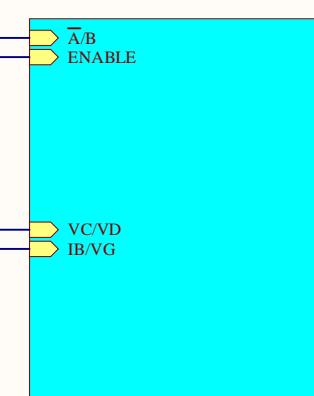
**U\_PROCESSOR**  
PROCESSOR.SchDoc



**U\_POWERAMP**  
POWERAMP.SchDoc

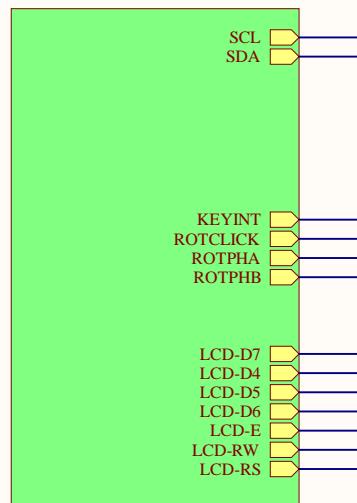


**U\_POWERMUX**  
POWERMUX.SchDoc



**WORK IN PROGRESS**

**U\_FrontPanel**  
FrontPanel.SchDoc



SDA

SCL

KEYINT

ROTCLOCK

ROTPHA

ROTPHB

LCD-D7

LCD-D4

LCD-D5

LCD-D6

LCD-E

LCD-RW

LCD-RS

ADC-D0

ADC-D1

ADC-D2

ADC-D3

ADC-D4

ADC-D5

ADC-D6

ADC-D7

IBPOL

IB1

IB2

BFA

ADC-IBG

ADC-VBG

ADC-D0

ADC-D1

ADC-D2

ADC-D3

ADC-D4

ADC-D5

ADC-D6

ADC-D7

IBPOL

IB1

IB2

BFA

ADC-IBG

ADC-VBG

**U\_MUX-PLAYER**  
MULTIPLAYER.SchDoc

YOUT

MARKER

PMA

PMB

OVERLOAD

**U\_IBVG-DRIVER**  
IBVG-DRIVER.SchDoc

IB/VG

IBPOL

IB1

IB2

BFA

ADC-D0

ADC-D1

ADC-D2

ADC-D3

ADC-D4

ADC-D5

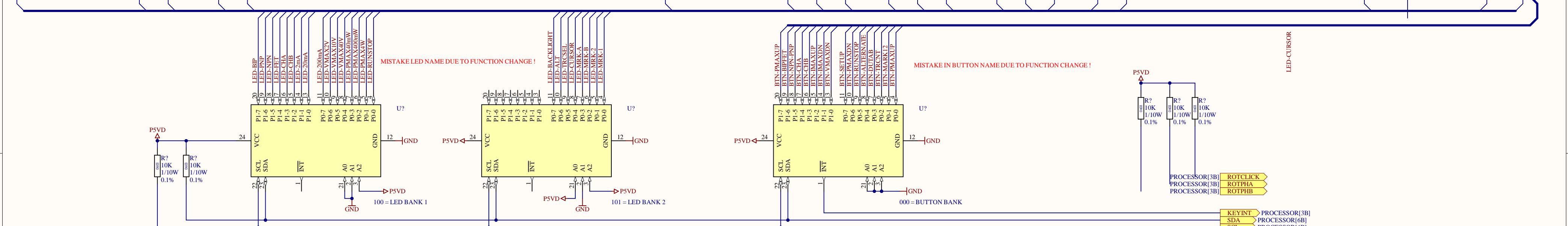
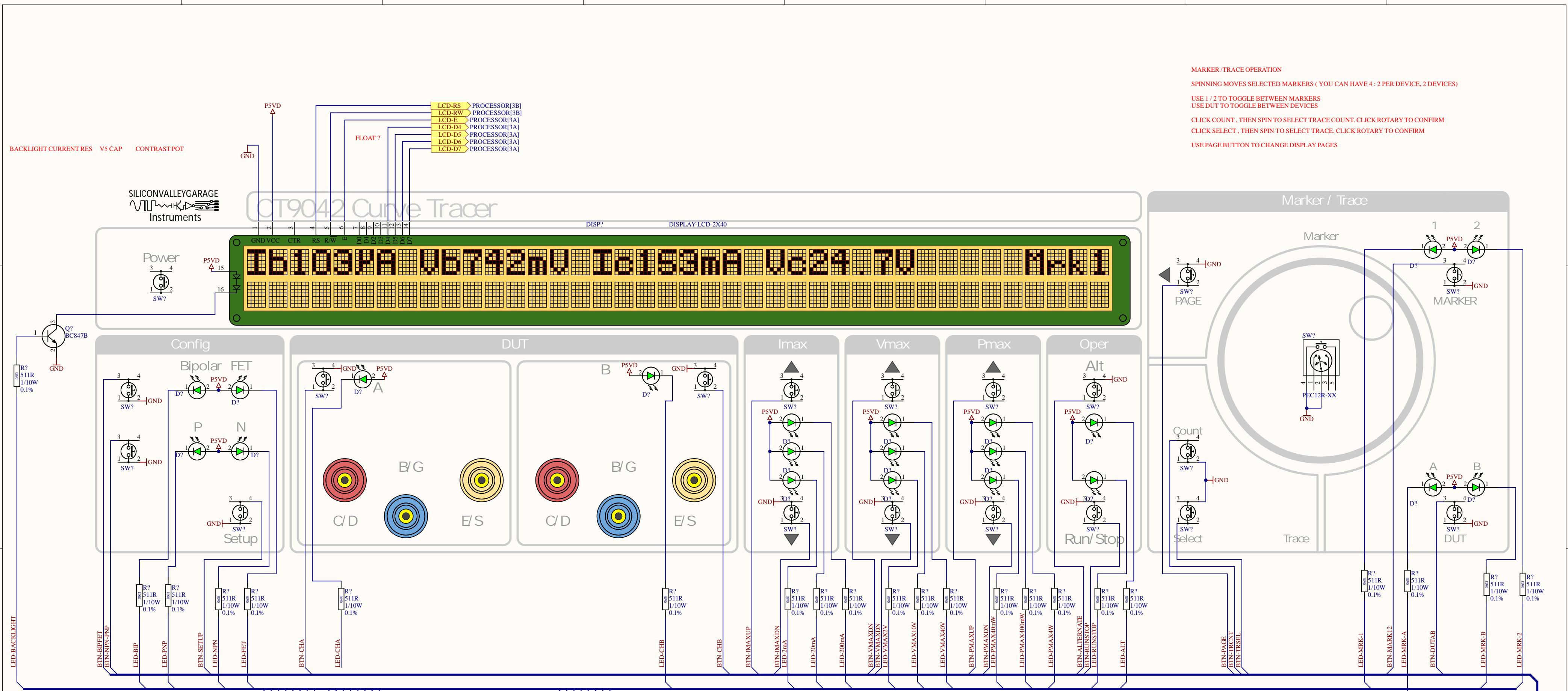
ADC-D6

ADC-D7

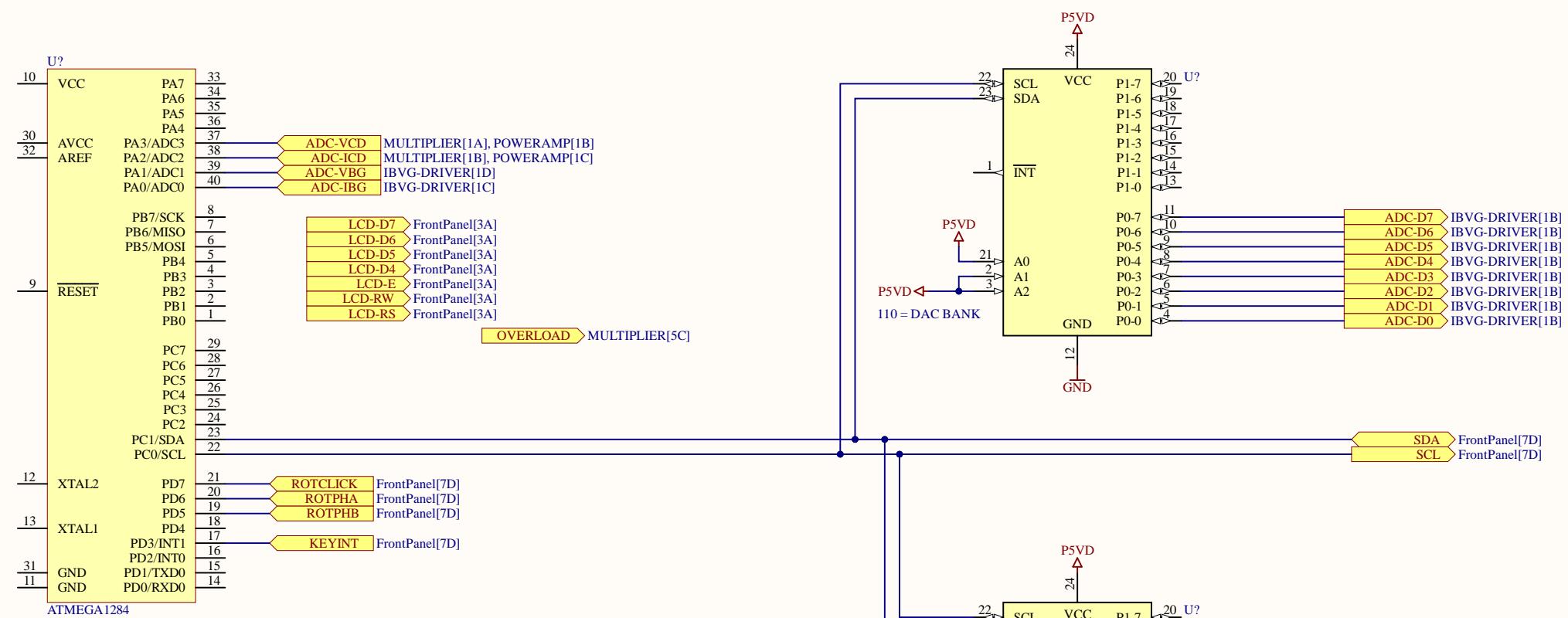
ADC-IBG

ADC-VBG

SILICONVALLEYGARAGE  
Instruments  
**CT9042**  
Curve Tracer

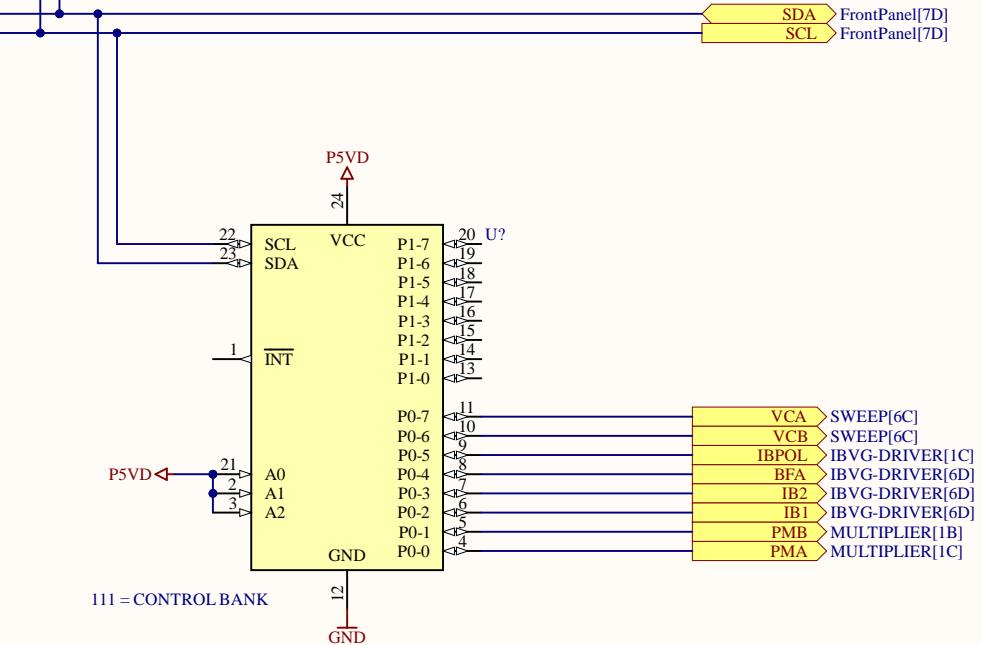


A



B

A

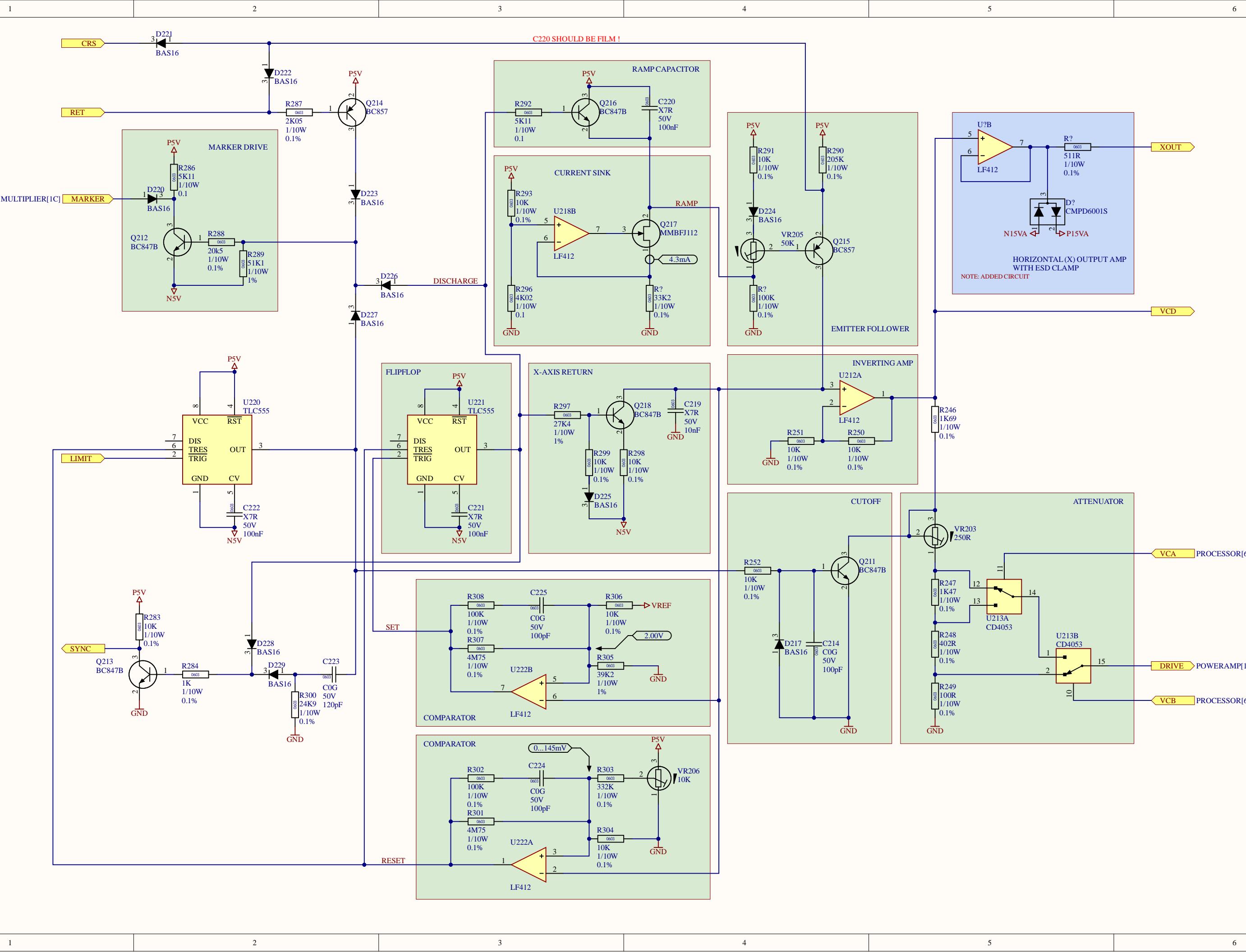


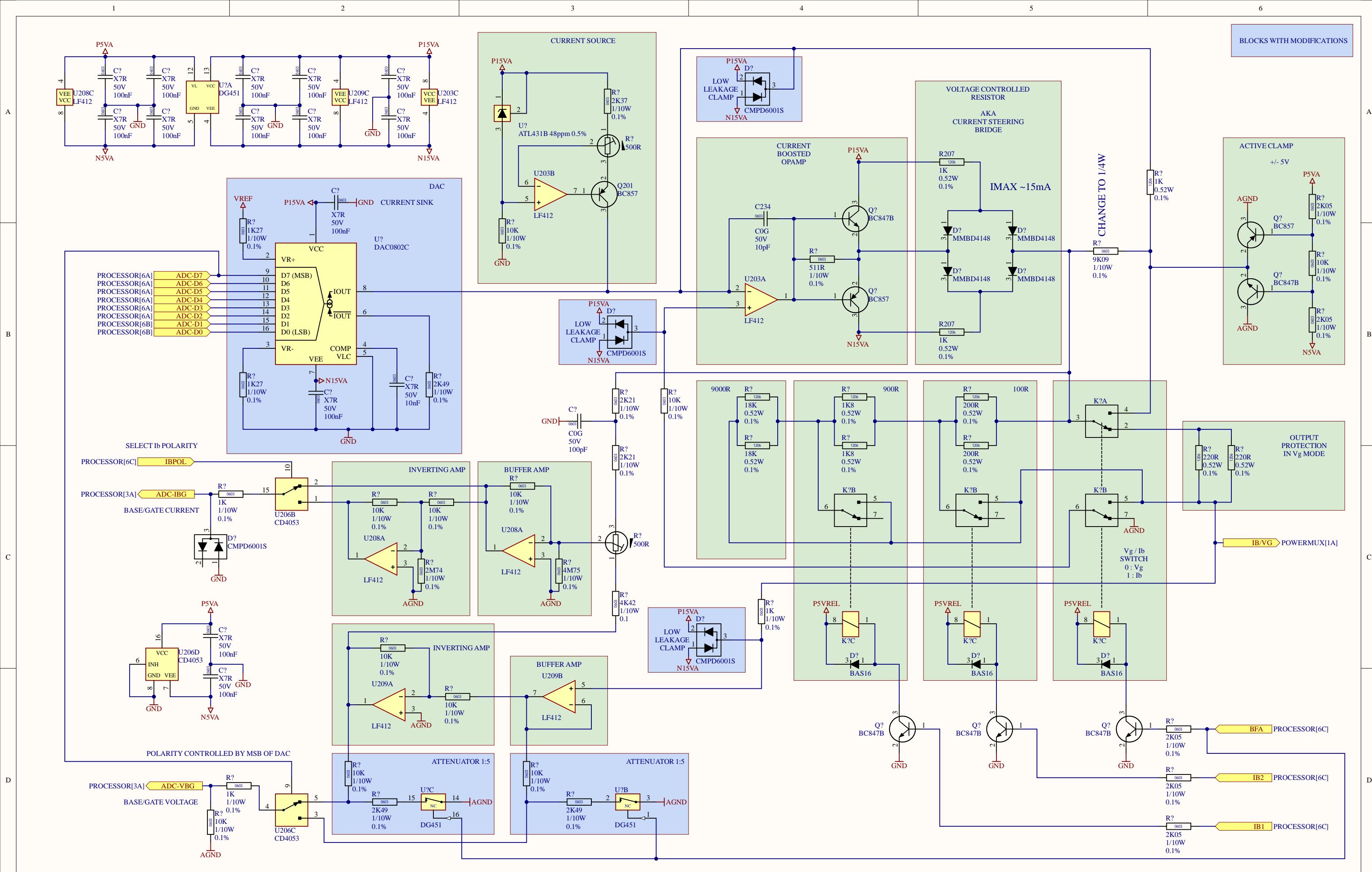
C

B

D

C

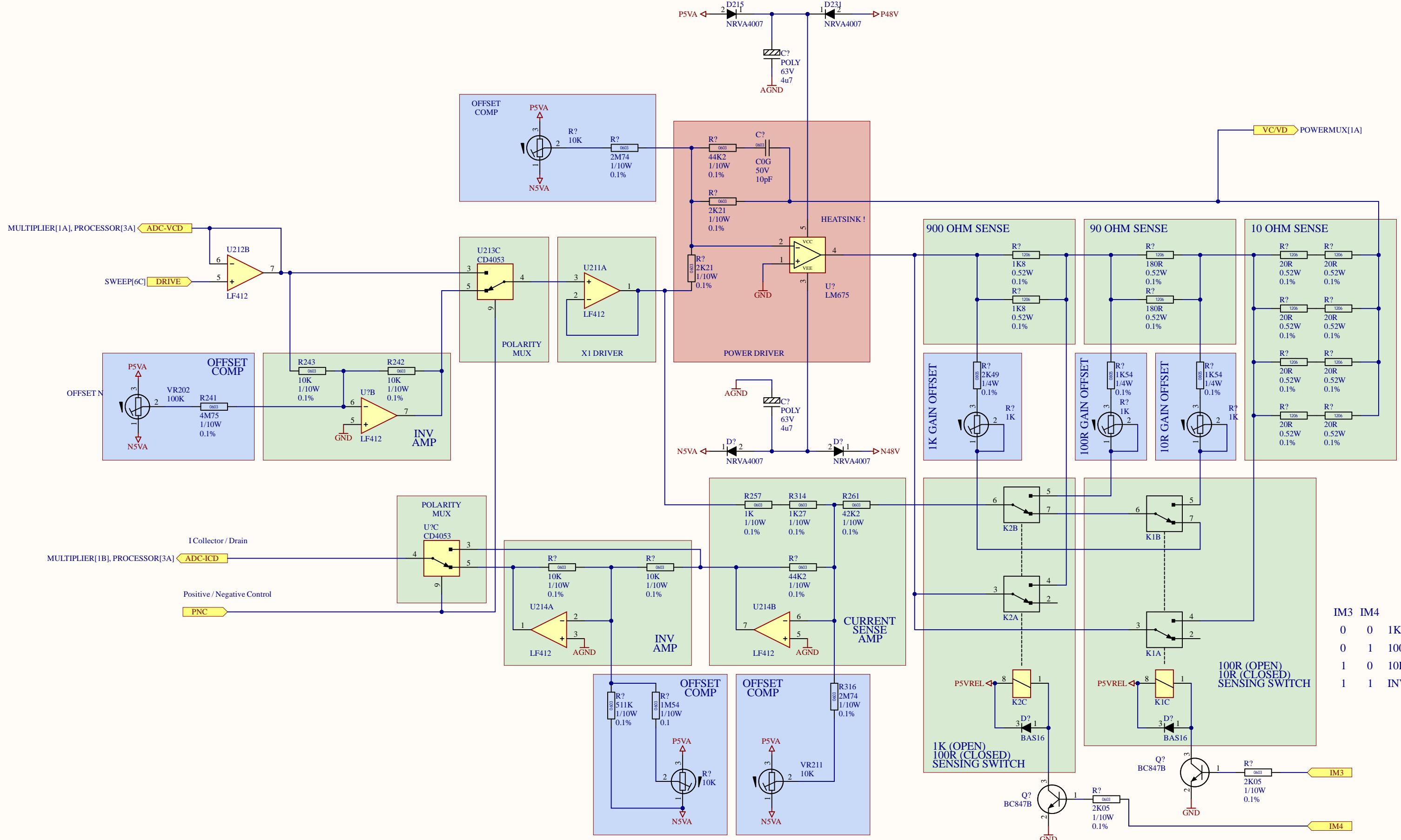




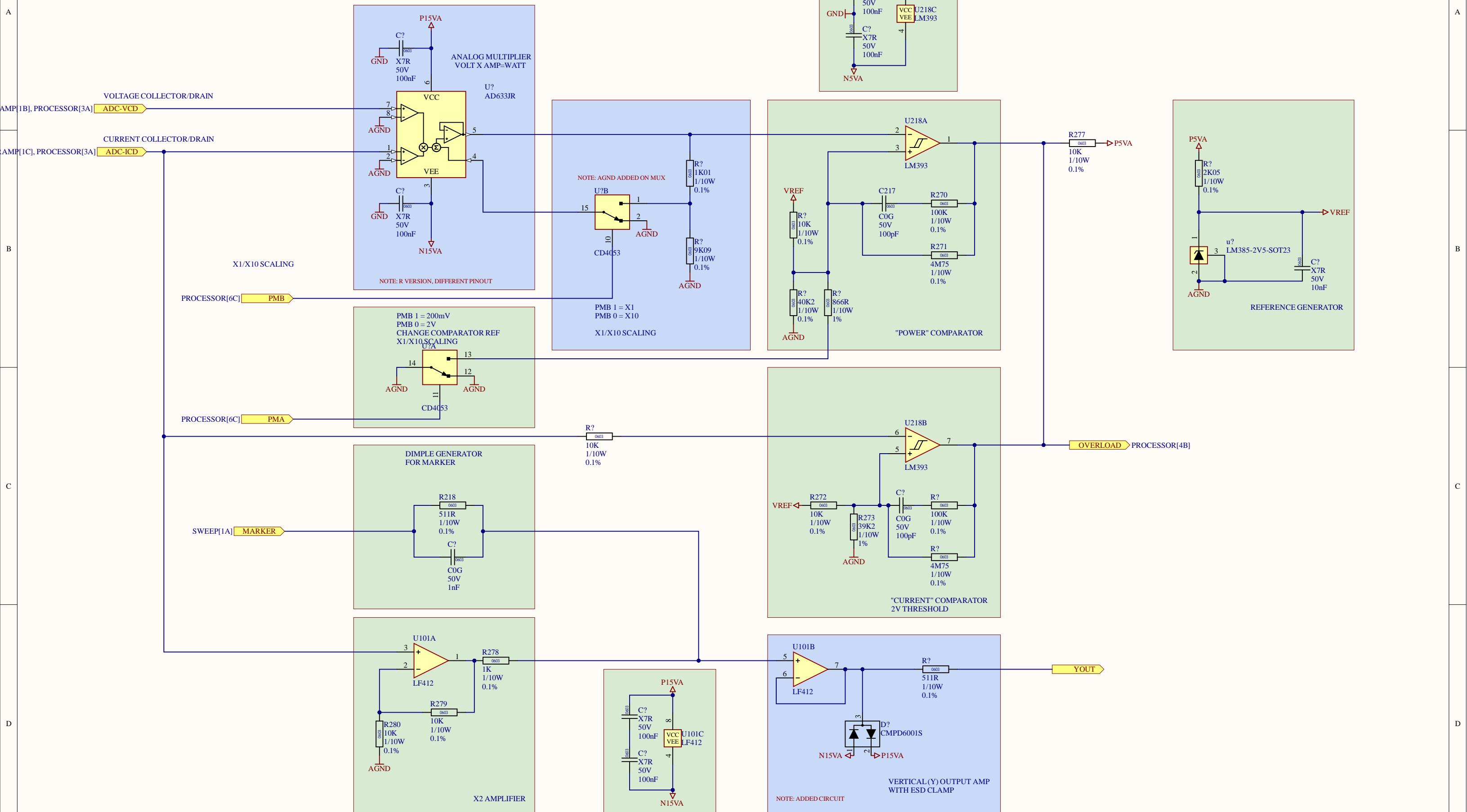
BLOCKS WITH MODIFICATIONS

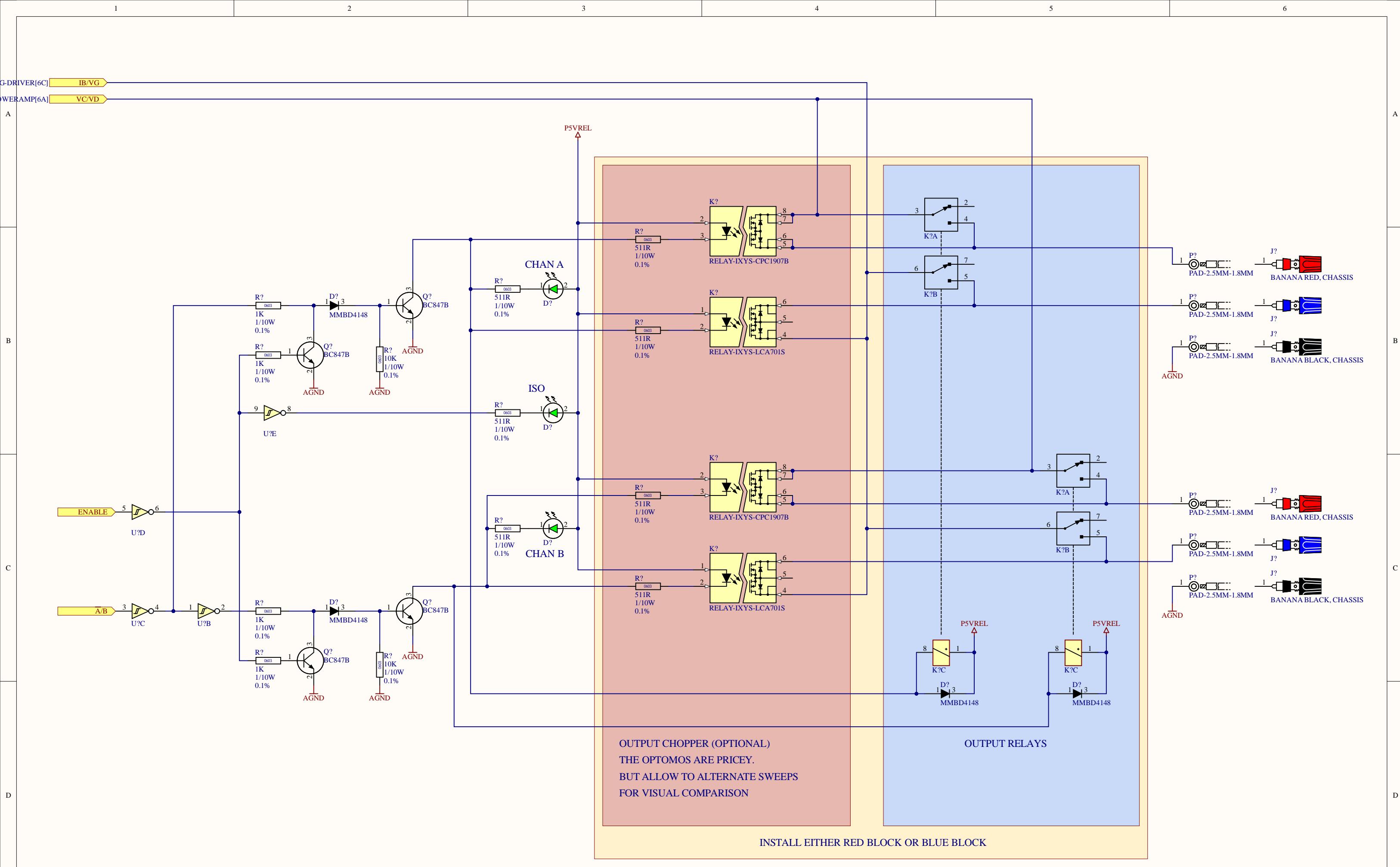
A

A

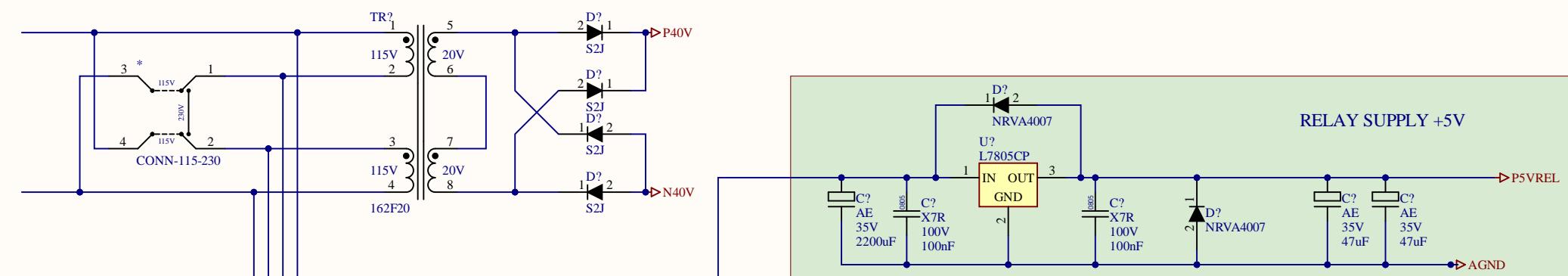


BLOCKS WITH MODIFICATIONS

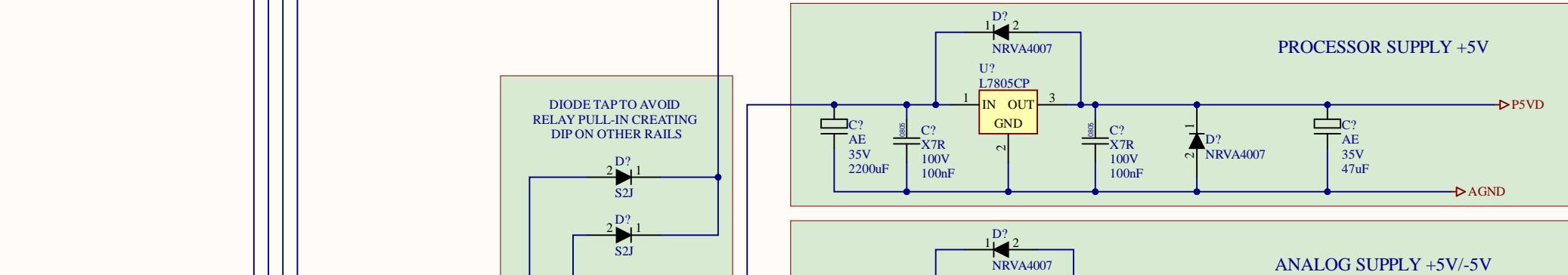




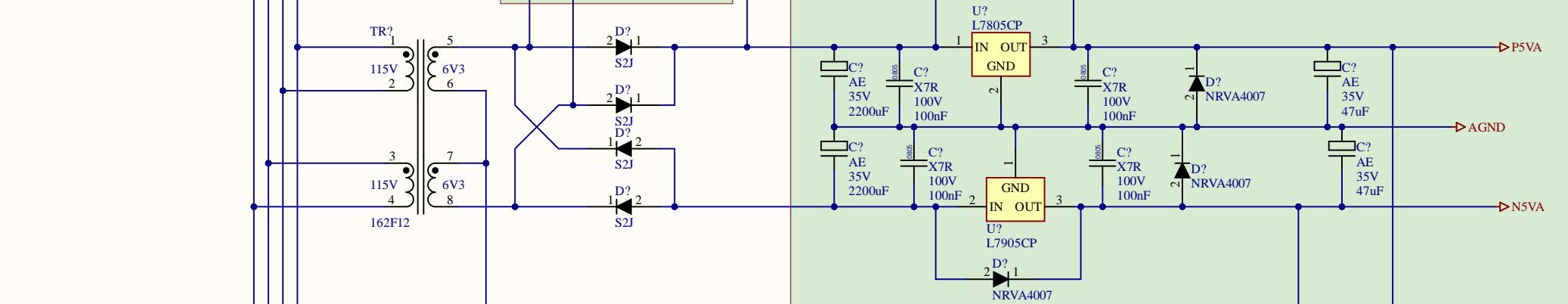
A



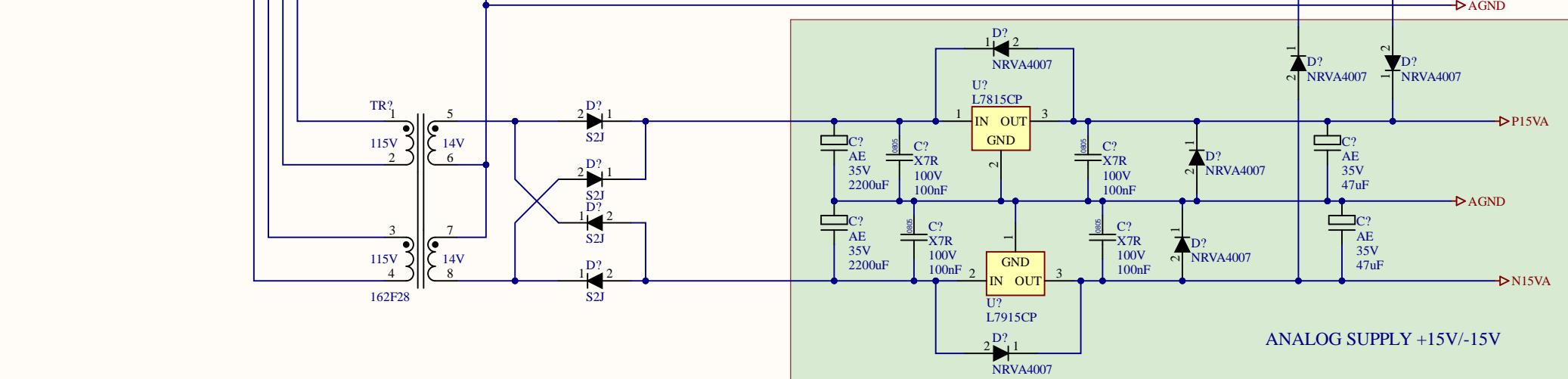
B



C



D



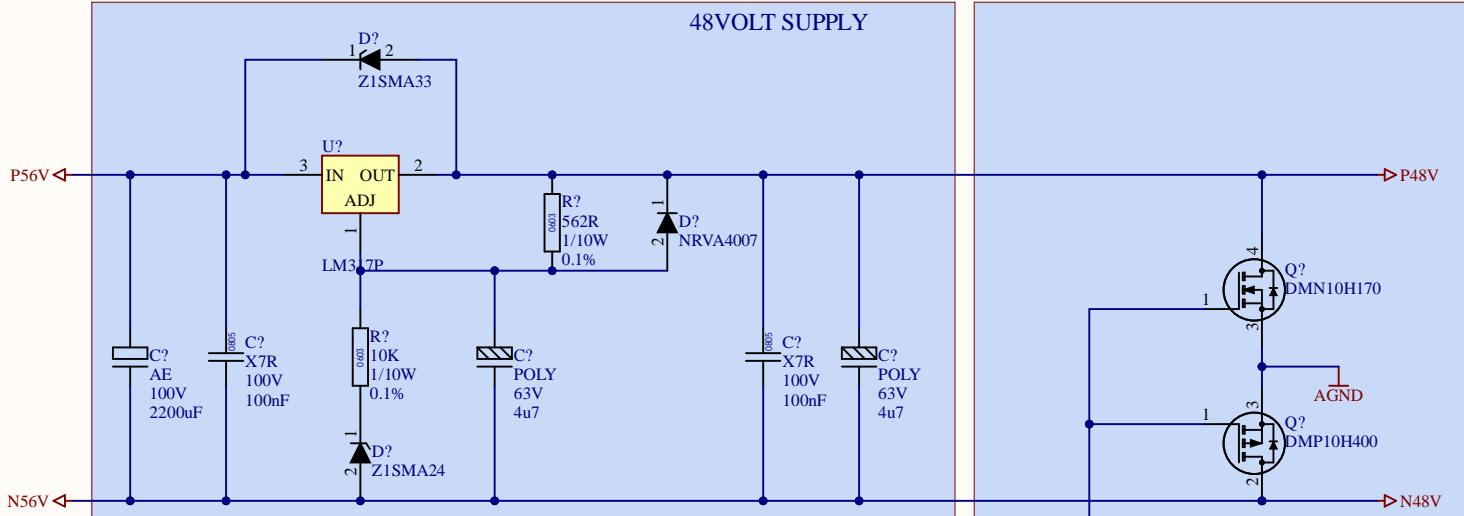
A

B

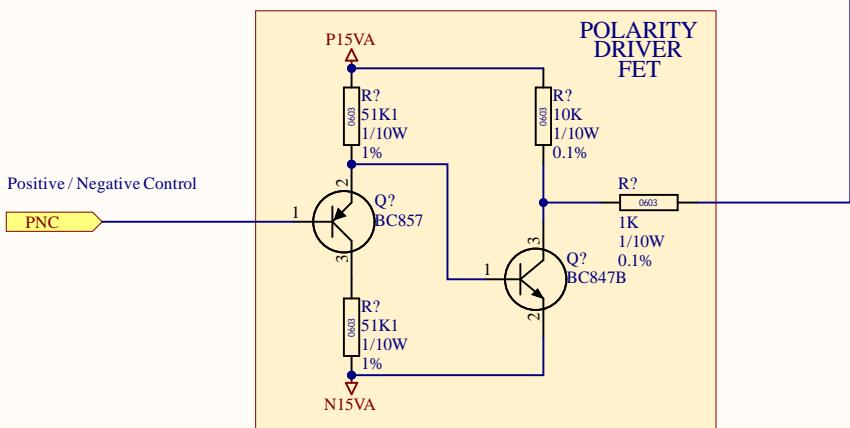
C

D

BLOCKS WITH MODIFICATIONS



THIS MECHANISM PUSHES EITHER THE POSITIVE RAIL TO 40 VOLTS OR THE NEGATIVE RAIL TO -40 VOLTS. THE POWER AMP EITHER RUNS FROM +5 TO -40 VOLTS, OR FROM -5 TO +40 VOLTS



# GENERAL

## GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.
3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER
4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2
5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

## MATERIALS

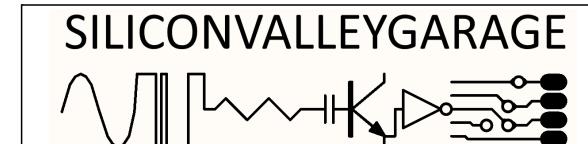
7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

## STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

## QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY



Project CT9042.PrjPcb

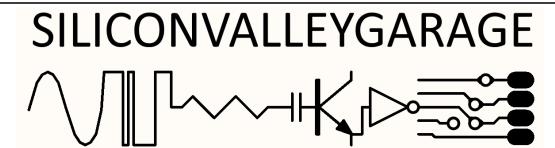
Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER STACK

## Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material Type	Gerber Dk	Weight	Constructions	Df	Resin
A		Top Overlay		Legend GTO					
B	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask GTS	3.5			
C	<b>Copper</b>	<b>Top Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal GTL</b>	<b>1oz</b>			
D		Prepreg	0.102mm(4.000mil)	Core-009	Dielectric	4.5	1-2116	0.02	47%
			1.450mm(57.087mil)	FR-4	Dielectric	4.8			
		Prepreg	0.102mm(4.000mil)	Core-009	Dielectric	4.5	1-2116	0.02	47%
	<b>Copper</b>	<b>Bottom Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal GBL</b>	<b>1oz</b>			
	Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask GBS	3.5			
		Bottom Overlay		Legend GBO					
	Total thickness: 1.745mm(68.687mil)								



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
▽	21	2.100mm(82.677mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
□	19	5.500mm(216.535mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
☆	1	8.000mm(314.961mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
○	6	8.600mm(338.583mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
47 Total											

A

A

B

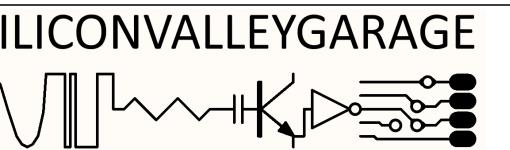
B

C

C

D

D



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

19

20

21

22

23

24

# DRILL DRAWING

A

A

Drill Drawing View (Scale 1.5:1)



B

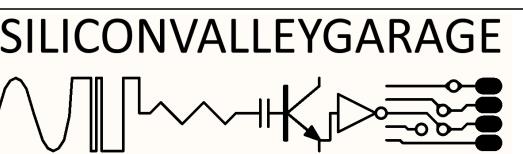
B

C

C

D

D



**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

19

20

21

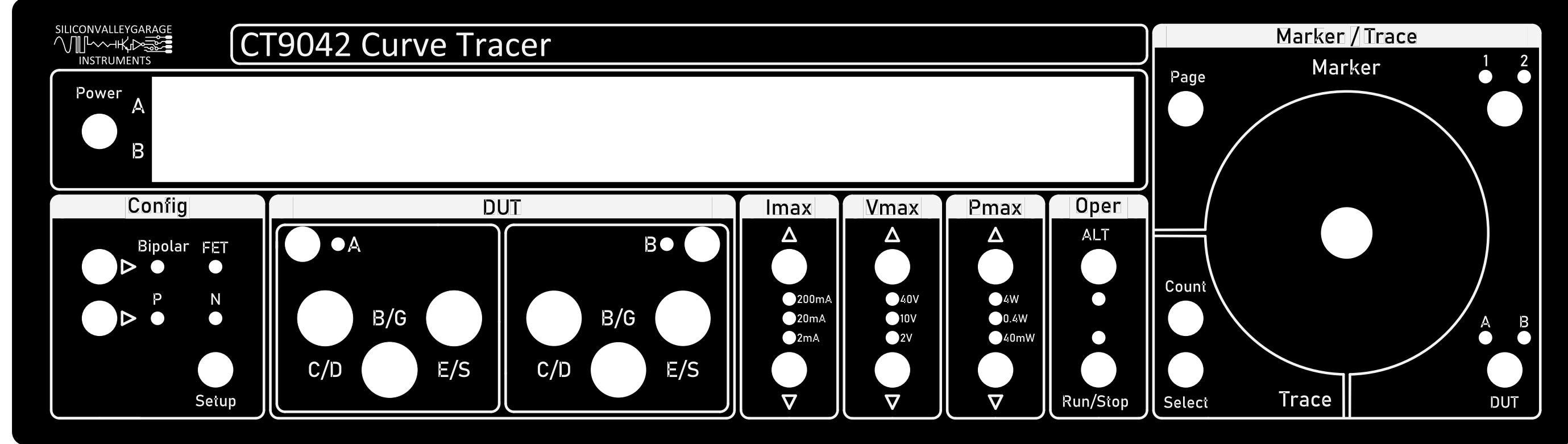
22

23

24

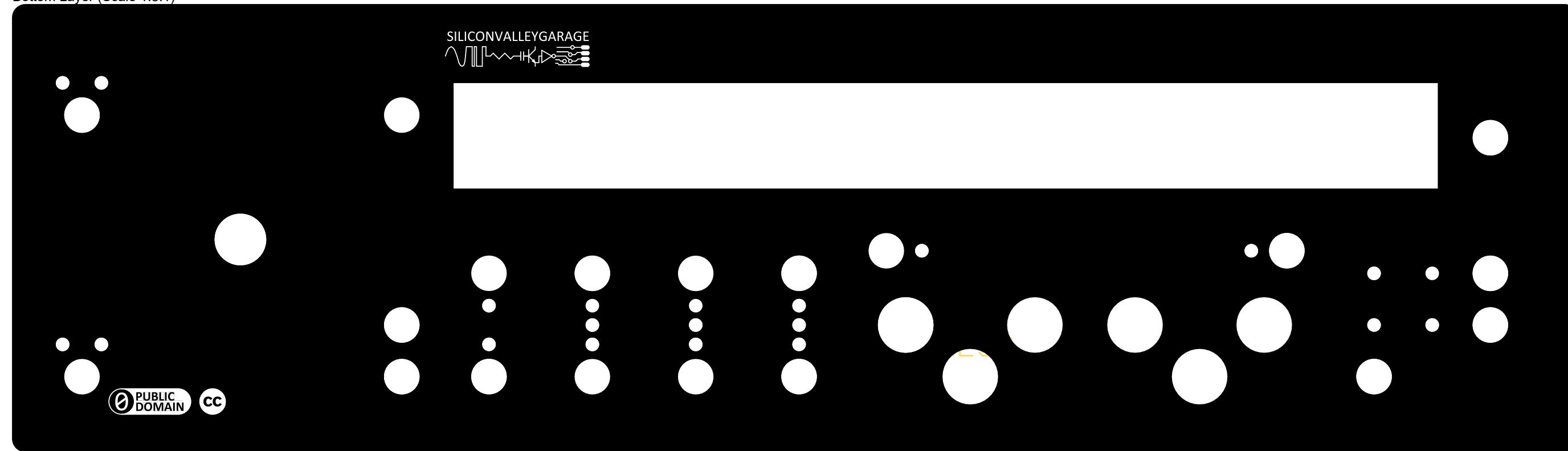
# COMPOSITE VIEW FRONT

Top Layer (Scale 1.5:1)



## COMPOSITE VIEW BACK

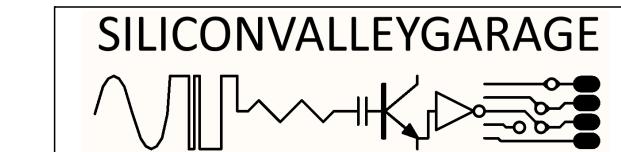
Bottom Layer (Scale 1.5:1)



# LAYER VIEW : TOP LAYER

Top Layer (Scale 1.5:1)

WORK IN PROGRESS



**Project CT9042.PrjPcb**

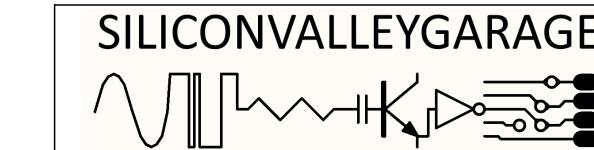
Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER VIEW : BOTTOM LAYER

Bottom Layer (Scale 1.5:1)

MORK IN PROGRESS



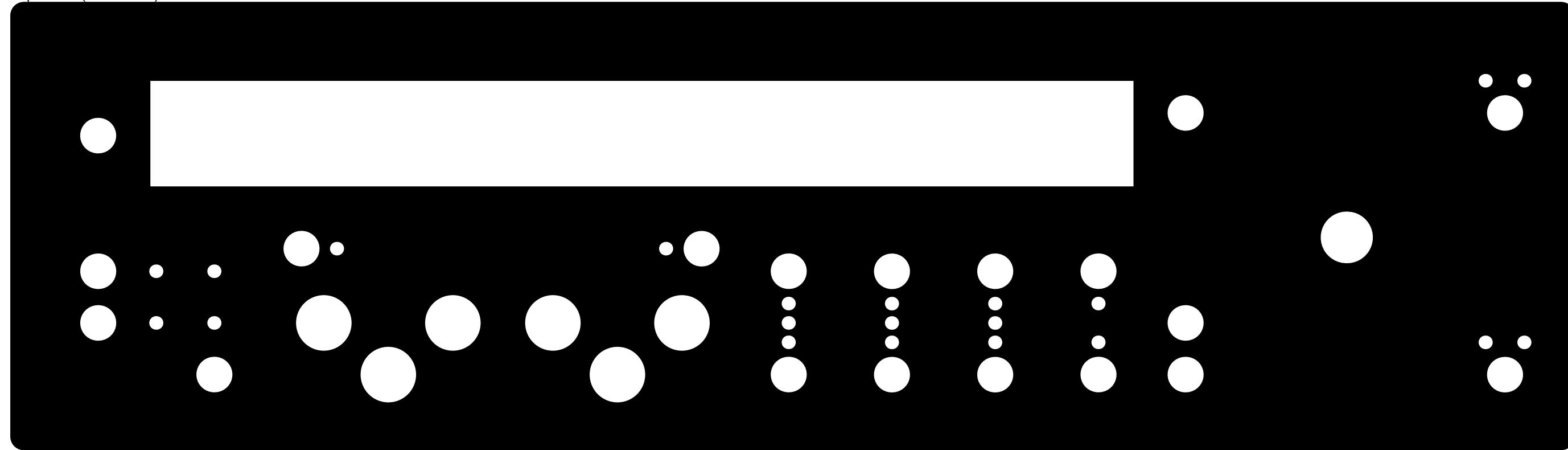
**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

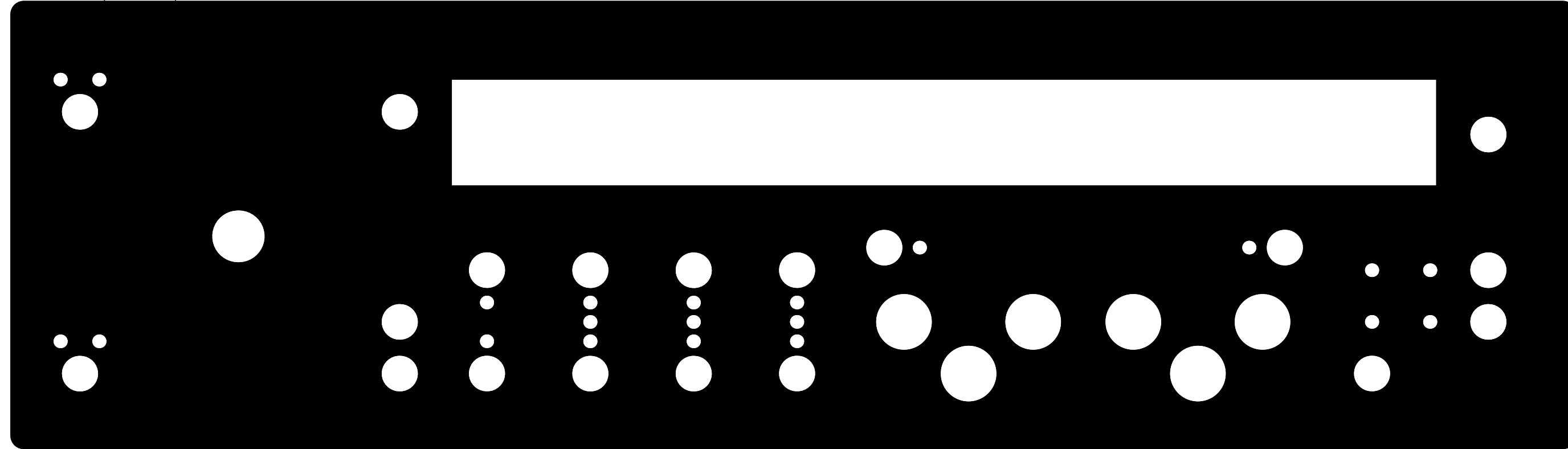
# LAYER VIEW : TOP SOLDER MASK

Top Solder (Scale 1.5:1)



# LAYER VIEW : BOTTOM SOLDER MASK

Bottom Solder (Scale 1.5:1)



A

A

B

B

C

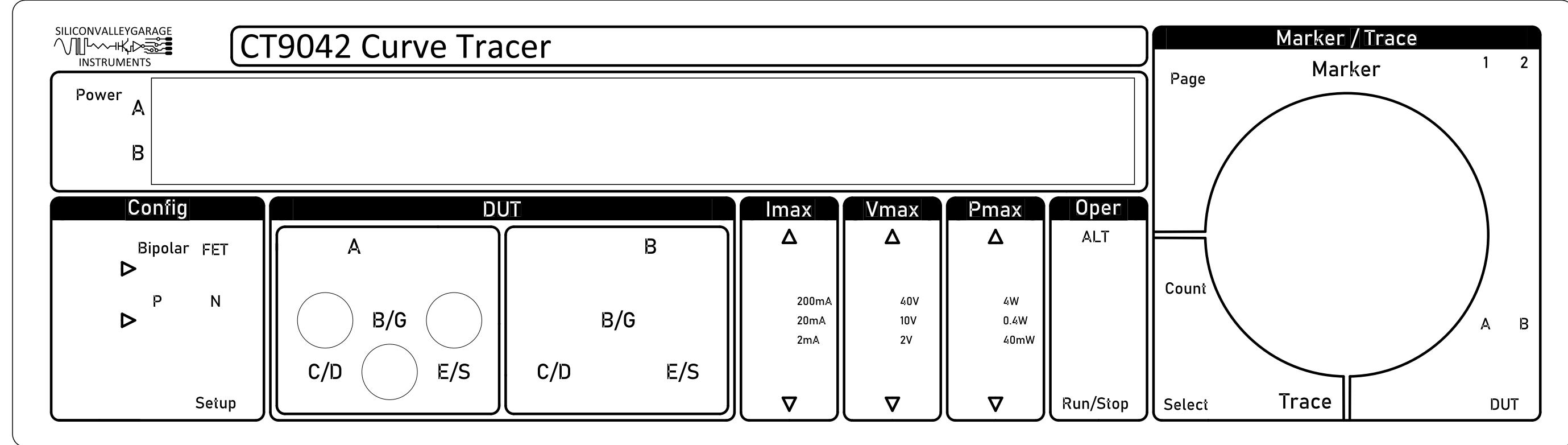
C

D

D

# LAYER VIEW : TOP SILKSCREEN (LEGEND)

Top Overlay (Scale 1.5:1)



# LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

Bottom Overlay (Scale 1.5:1)



# GENERAL

## GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.
3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER
4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2
5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

## MATERIALS

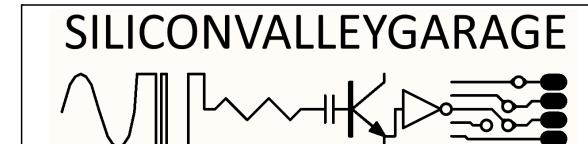
7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

## STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

## QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY



Project CT9042.PrjPcb

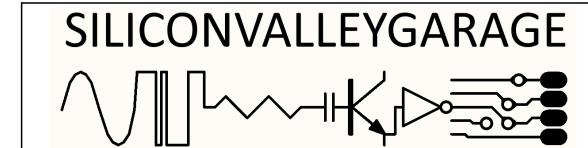
Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER STACK

## Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material Type	Gerber Dk	Weight	Constructions	Df	Resin
A	Top Overlay			Legend	GTO				
B	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5		
C	<b>Copper</b>	<b>Top Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal</b>	<b>GTL</b>	<b>1oz</b>		
D	Prepreg		0.102mm(4.000mil)	Core-009	Dielectric		4.5	1-2116	0.02 47%
	CF-004	Layer 1	0.035mm(1.378mil)		Signal	G1	1oz		
			1.450mm(57.087mil)	FR-4	Dielectric		4.8		
	CF-004	Layer 2	0.035mm(1.378mil)		Signal	G2	1oz		
	Prepreg		0.102mm(4.000mil)	Core-009	Dielectric		4.5	1-2116	0.02 47%
	<b>Copper</b>	<b>Bottom Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal</b>	<b>GBL</b>	<b>1oz</b>		
	Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5		
	Bottom Overlay			Legend	GBO				
	Total thickness: 1.815mm(71.443mil)								



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# DRILL LEGEND

**Drill Table**

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
□	125	1.000mm(39.370mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
▽	2	2.600mm(102.362mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✖	2	3.200mm(125.984mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✖	6	10.000mm(393.701mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
135 Total											

A

A

B

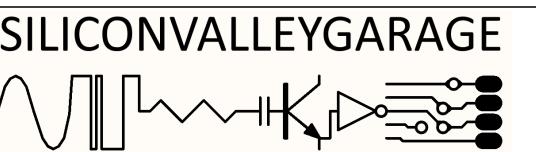
B

C

C

D

D



**Project CT9042.PjPcb**

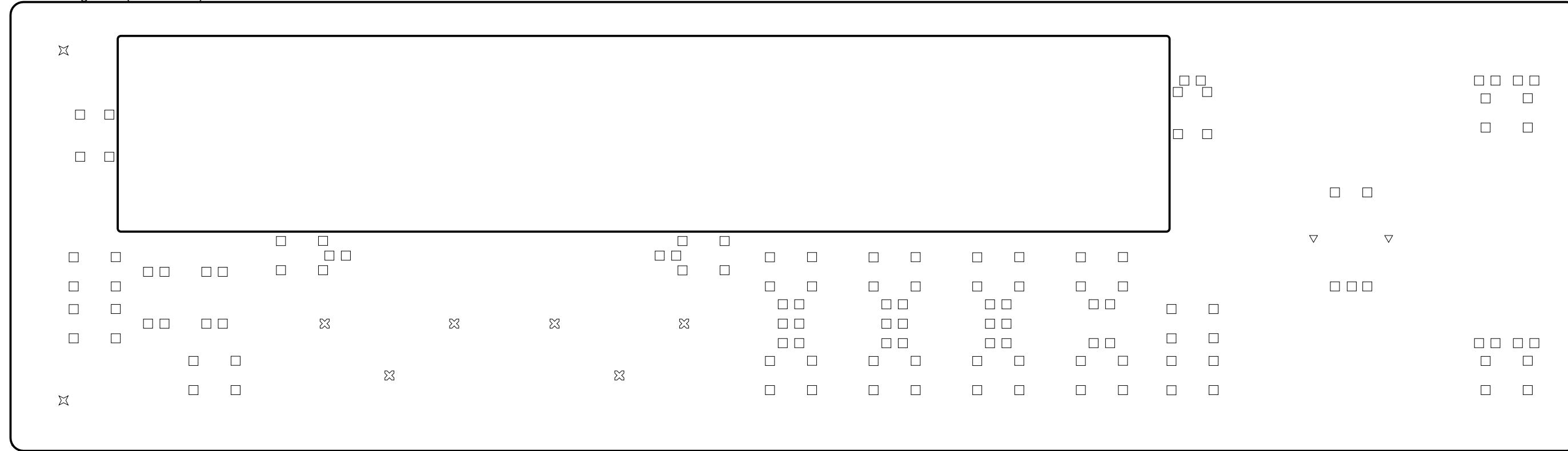
Version: | Variant [No Variations]

FABRICATION DRAWING

# DRILL DRAWING

A

Drill Drawing View (Scale 1.5:1)



A

B

B

C

C

D

D

25

26

27

28

29

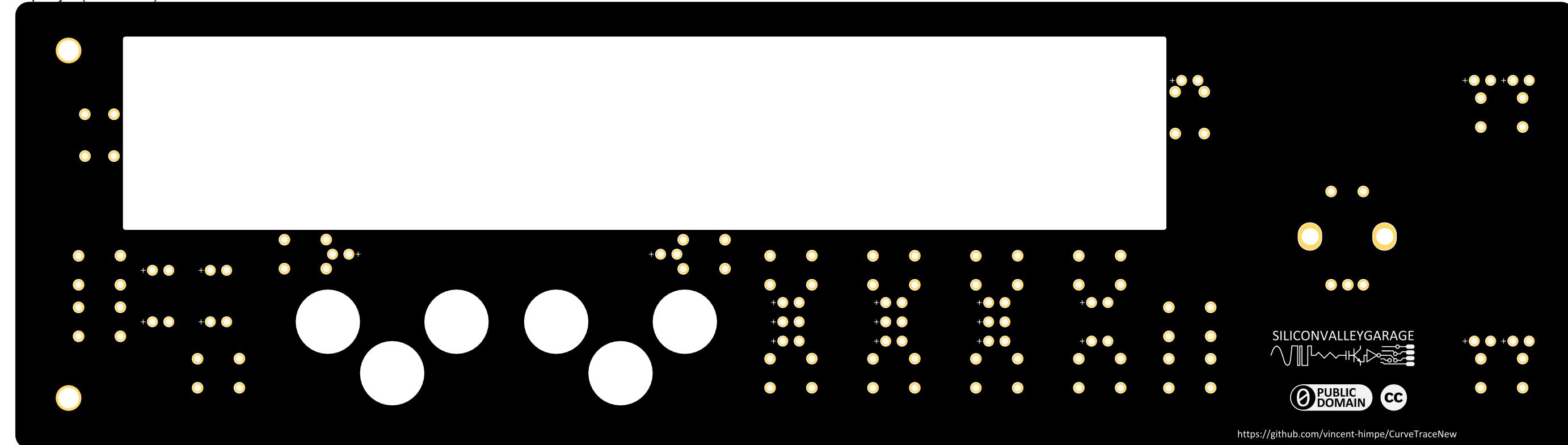
30

# COMPOSITE VIEW FRONT

A

A

Top Layer (Scale 1.5:1)



B

B

C

C

D

D

31

32

33

34

35

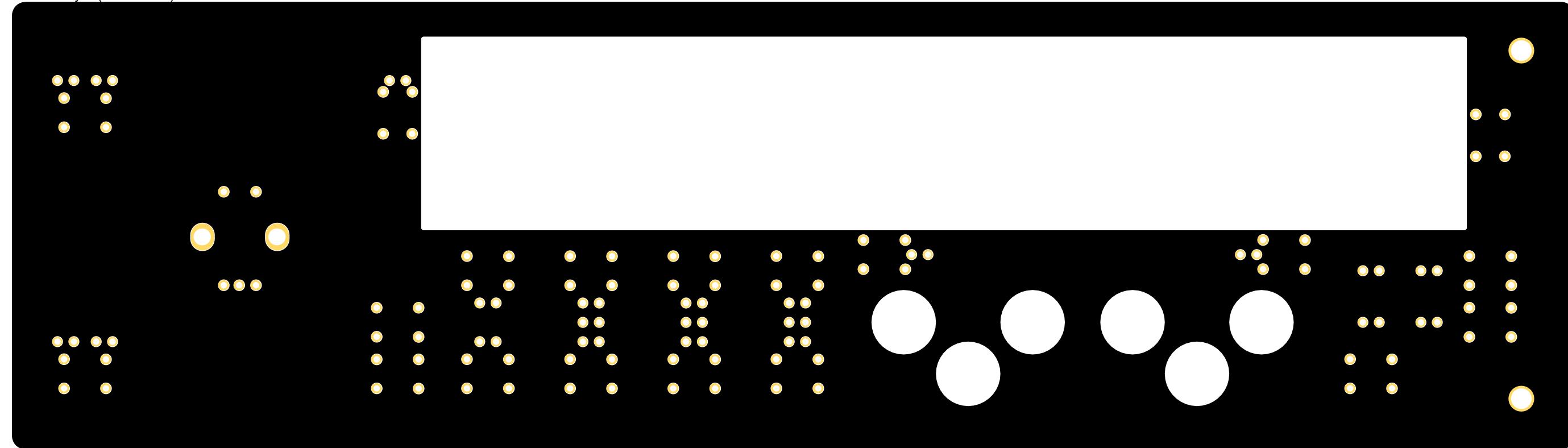
36

# COMPOSITE VIEW BACK

A

A

Bottom Layer (Scale 1.5:1)



B

B

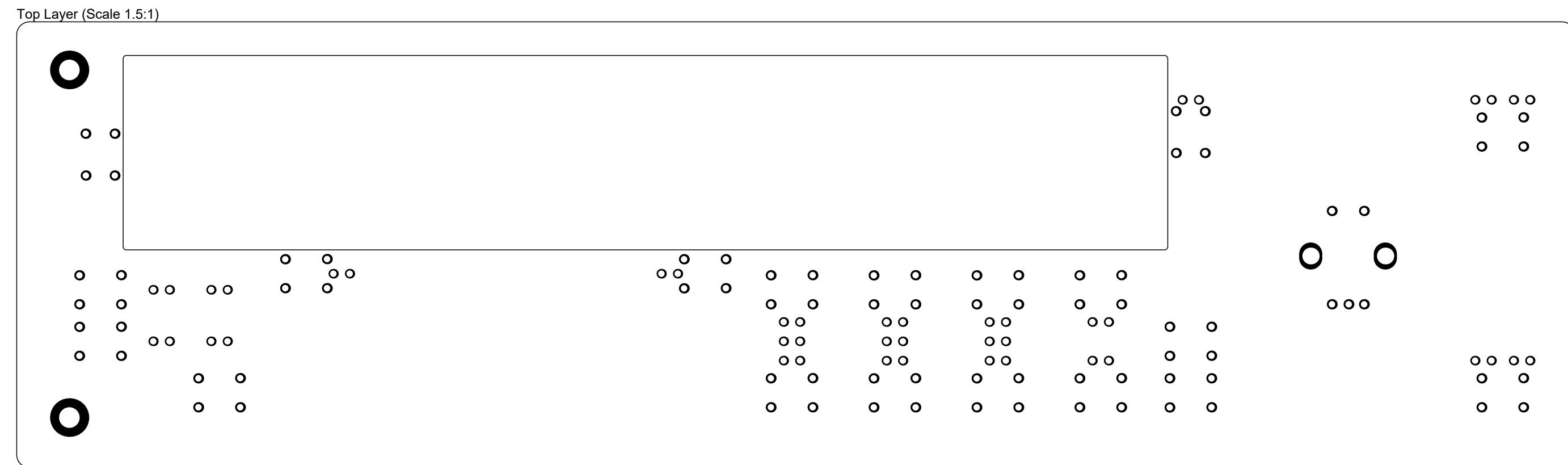
C

C

D

D

# LAYER VIEW : TOP LAYER

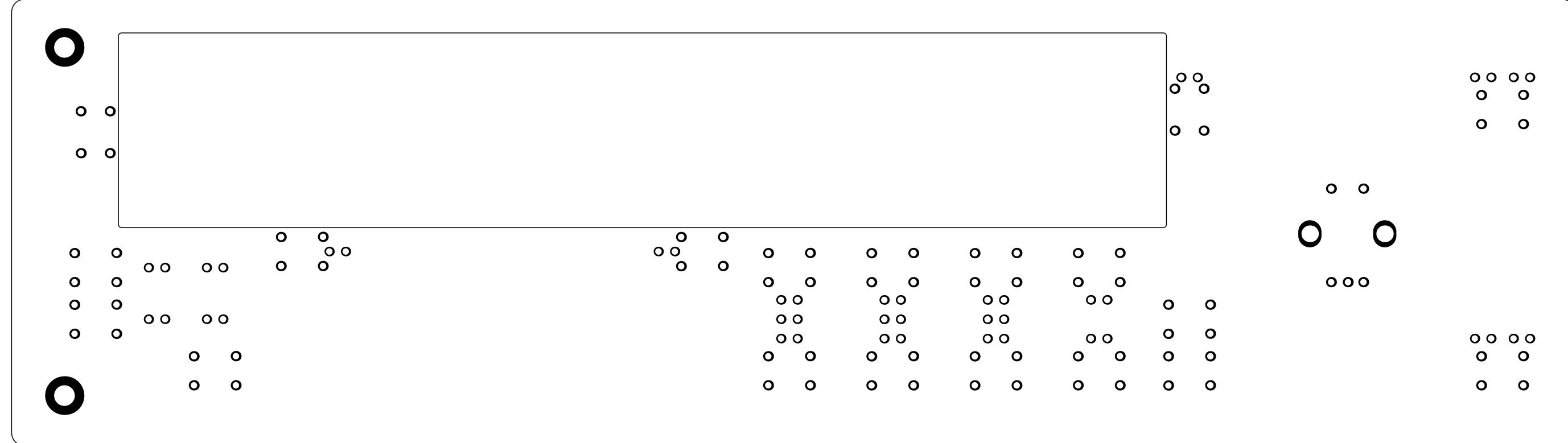


## LAYER VIEW : MID LAYER 1

A

A

Layer 1 (Scale 1.5:1)



B

B

C

C

D

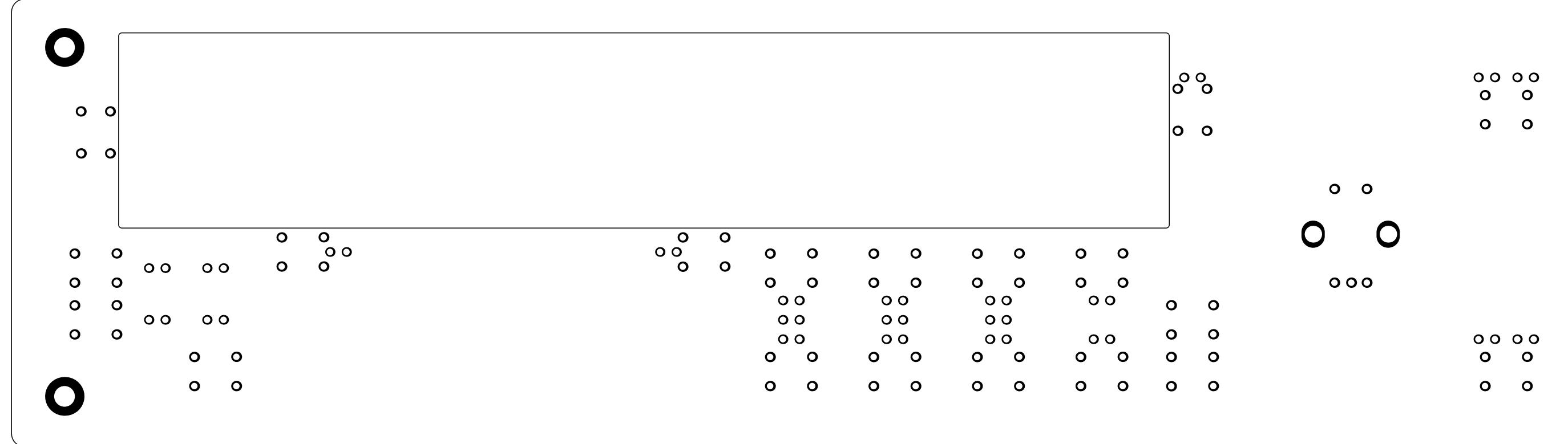
D

## LAYER VIEW : MID LAYER 2

A

A

Layer 2 (Scale 1.5:1)



B

B

C

C

D

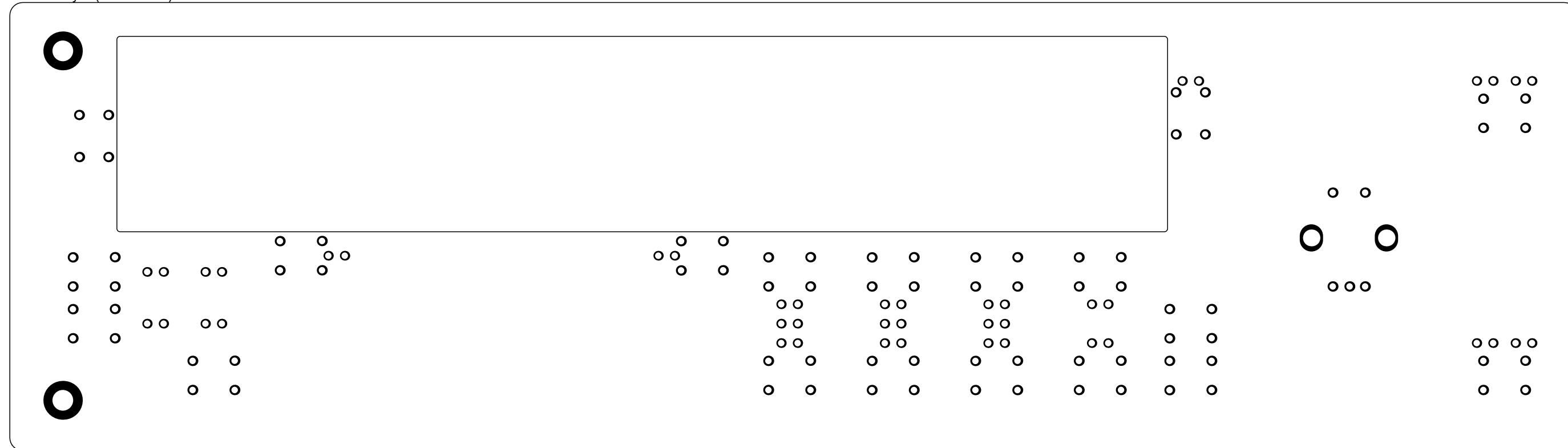
D

## LAYER VIEW : BOTTOM LAYER

A

A

Bottom Layer (Scale 1.5:1)



B

B

C

C

D

D

61

62

63

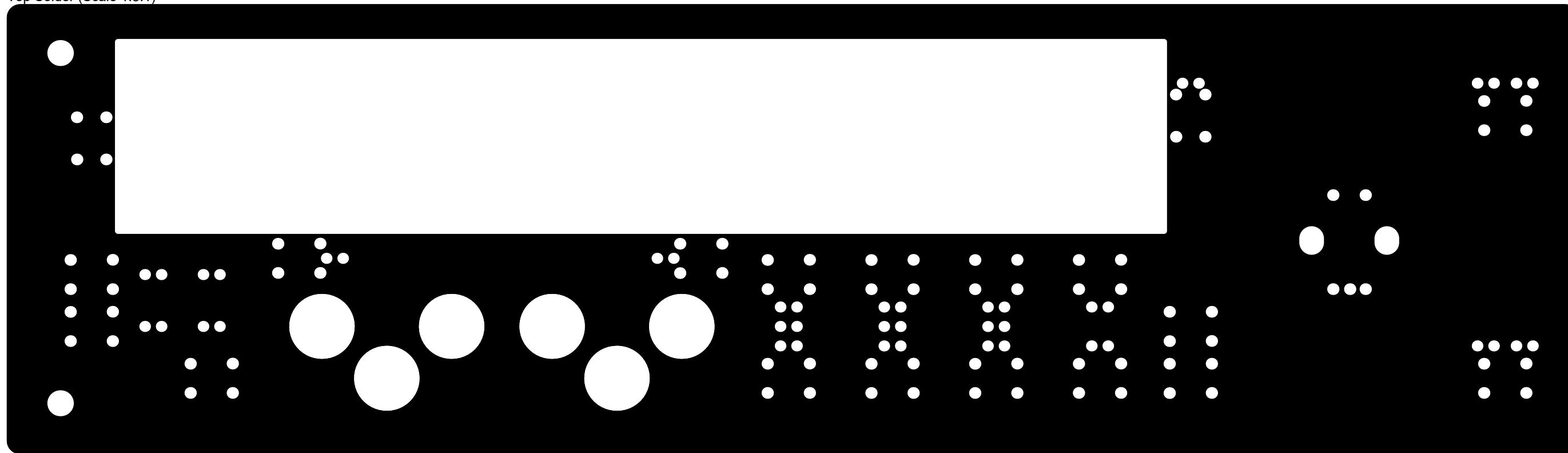
64

65

66

# LAYER VIEW : TOP SOLDER MASK

Top Solder (Scale 1.5:1)



A

A

B

B

C

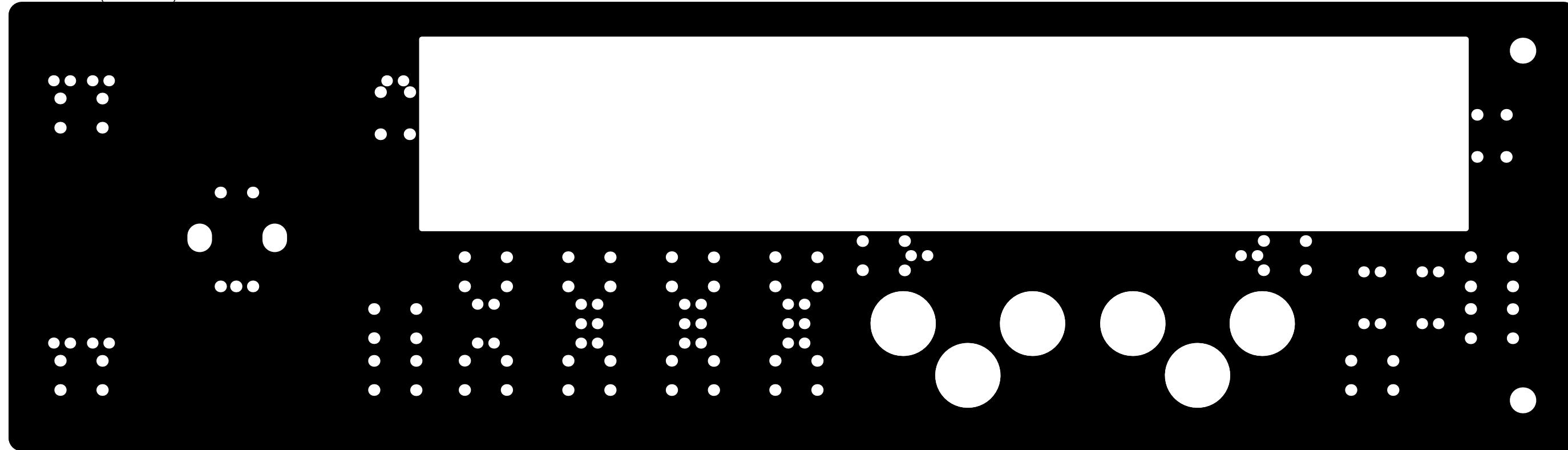
C

D

D

# LAYER VIEW : BOTTOM SOLDER MASK

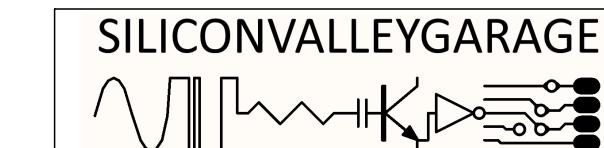
Bottom Solder (Scale 1.5:1)



# LAYER VIEW : TOP SILKSCREEN (LEGEND)

## Top Overlay (Scale 1.5:1)

<https://github.com/vincent-himpe/CurveTraceNew>



Project CT9042.PrjPcb

Version: | Variant [No Variations]

## FABRICATION DRAWING

# LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

A

Bottom Overlay (Scale 1.5:1)



A

B

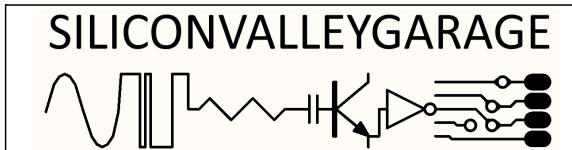
B

C

C

D

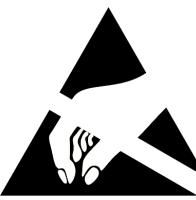
D

**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

# GENERAL



## A Unless otherwise specified the following rules apply:

1. DO NOT DEVIATE FROM ARTWORK OR BOM WITHOUT PRIOR AUTHORIZATION.
2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

## B Bill of Materials and Material Handling

3. THE BOM CONTAINED IN THIS DOCUMENT IS AS-BUILT. NON-INSTALLED PARTS HAVE BEEN REMOVED. ADDITIONAL BOM FORMATS ARE AVAILABLE IN THE PROJECT FILES
4. ANY PART SUBSTITUTIONS MUST BE APPROVED IN WRITING BEFORE ASSEMBLY
5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
7. ESD CONTROL PER IPC RULES

## B Soldering

8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
10. SOLDERING PREFERABLY TO BE DONE USING NITROGEN ATMOSPHERE
11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

1

2

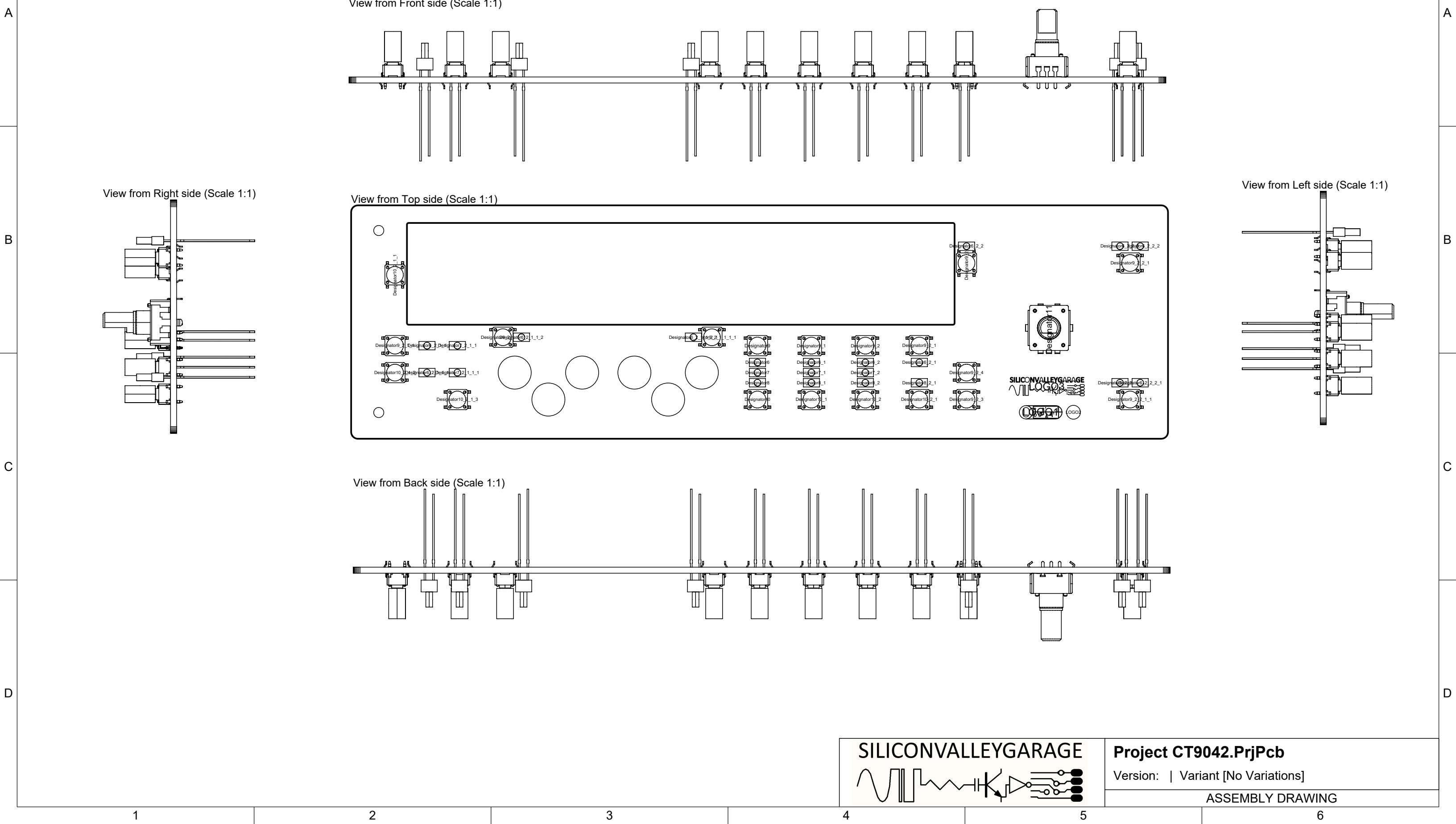
3

4

5

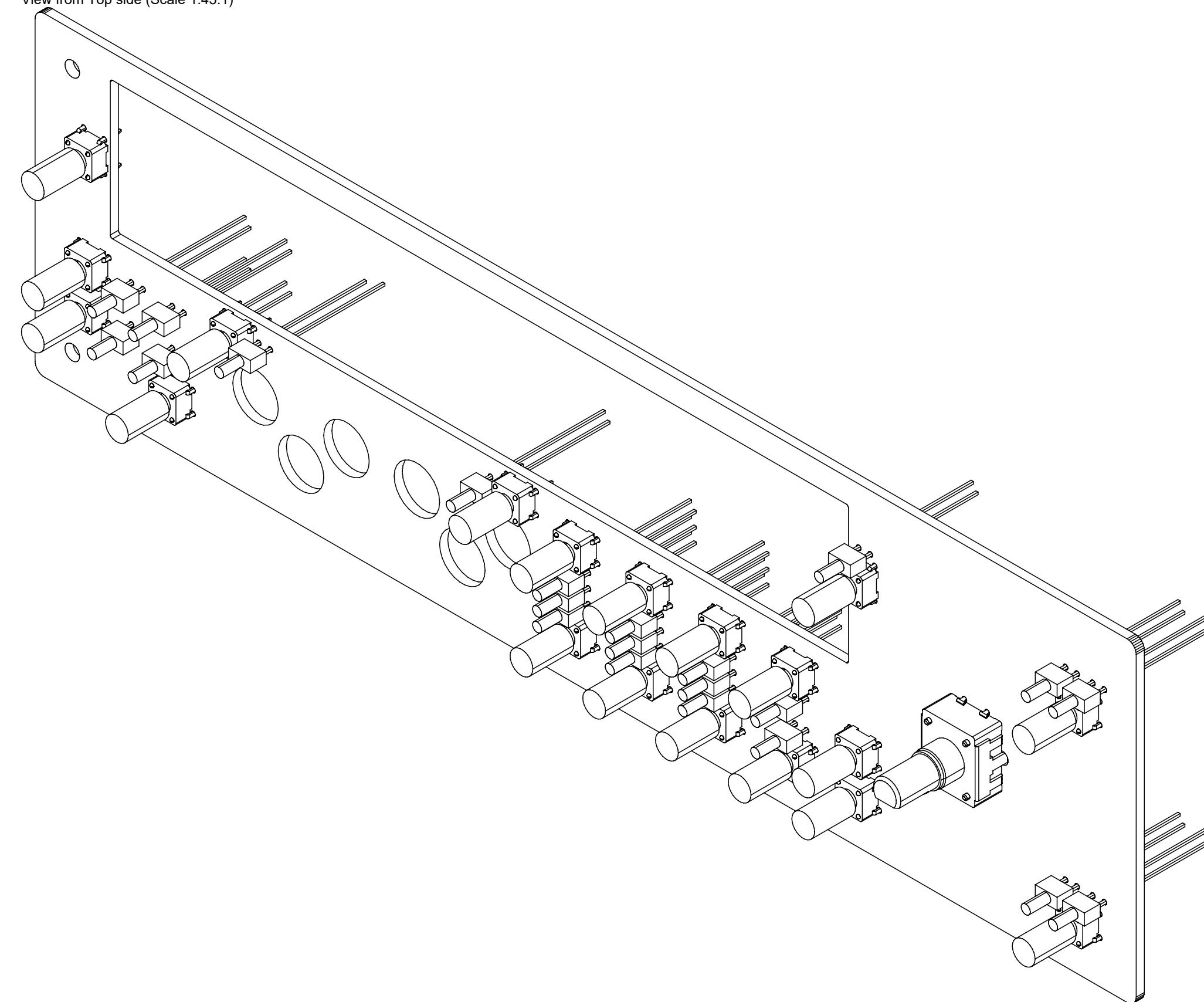
6

# 2D VIEW



## 3D VIEW

View from Top side (Scale 1.45:1)



# Bill Of Materials

A

Quantity	Designator	Description	LCSC	MOUSER
1				
6	C214, C217, C224, C225, C?	CAPACITOR,CERAMIC,100pF,50V,C0G,0603		
3	C219, C?	CAPACITOR,CERAMIC,10nF,50V,X7R,0603		
23	C220, C221, C222, C?	CAPACITOR,CERAMIC,100nF,50V,X7R,0603	C127833	80-C0603C104K5R
1	C223	CAPACITOR,CERAMIC,120pF,50V,C0G,0603		
2	C234, C?	CAPACITOR,CERAMIC,10pF,50V,C0G,0603		80-C0603C100J5GAC
1	C?	CAPACITOR,CERAMIC,1nF,50V,C0G,0603		
7	C?	CAPACITOR,ALU,47uF,35V,TH,P0.25mm,D6.3mm,H12.5mm		
6	C?	CAPACITOR,ALU,2200uF,35V,TH,P7.5mm,D16mm,H27mm		
1	C?	CAPACITOR,ALU,2200uF,100V,TH,P10mm,D35mm,H32mm,SNAP		
14	C?	CAPACITOR,CERAMIC,100nF,100V,X7R,0805		
4	C?	CAPACITOR,POLYMER,4u7,63V	C161937	
19	D215, D231, D?	DIODE,RECTIFIER,1000V,1A,ONSEMI,NRVA4007,SMA		
16	D217, D220, D221, D222, D223, D224, D225, D226, D227, D228, D229, D?	DIODE,RECTIFIER,75V,0.3A,BAS16,SOT23		
6	D?	DIODE,75V,250mA,SOT23,500pA ULTRA LOW LEAKAGE		
23	D?	LED,TH,GREEN,42mCd,3MM		78-VLMPG33N1P2
3	D?	LED,GREEN,TH,3MM		
8	D?	DIODE,RECTIFIER,75V,0.3A,MMBD4148,SOT23		
14	D?	DIODE,RECTIFIER,600V,2A,S2J,DO214AA(SMB)		637-SK115
1	D?	DIODE,ZENER,24V,1W,Z1SMA24,DO214AC(SMA)		
1	D?	DIODE,ZENER,33V,1W,Z1SMA33,DO214AC(SMA)		
1	DISP?	DISPLAY,LCD,ALPHA,2X40CHAR,HD44780,YELLOW BL		
2	J?			
2	J?			
2	J?	CONNECTOR,BANANA,BLUE,CHASSIS,CLIFF		
9	K1, K2, K?			
2	K?	RELAY,OPTOMOS,6A,60V,AC,IXYS,CPC1907B,SMD		
2	K?	RELAY,OPTOMOS,1.5A,100V,AC,IXYS,LCA701S,SMD		
6	K?	RELAY,DPDT,1A,250VAC,220VDC,5V COIL,KEMET,UA2-5NJ		
6	Q201, Q214, Q215, Q?	XSTR,PNP,SOT23,BC857,SOT23		
18	Q211, Q212, Q213, Q216, Q218, Q?	XSTR,NPN,45V,0.1A,,BC847B,SOT23		
1	Q217	XSTR,JFET,NCHAN,ONSEMI,MMBFJ112,SOT23		
1	Q?	XSTR,NMOS,100V,12A,DMN10H170SK3-13,DPAK		
1	Q?	XSTR,PMOS,100V,5.6A,DMP10H400SK3-13,DPAK		
3	R207, R?	RESISTOR,1K,1206,0.1%,520mW,1206		
3	R218, R?	RESISTOR,511R,0.1%,100mW,0603 (1608)		
6	R241, R271, R301, R307, R?	RESISTOR,4M75,0.1%,100mW,0603 (1608)		
40	R242, R243, R250, R251, R252, R272, R277, R279, R280, R283, R291, R293, R298, R299, R304, R306, R?	RESISTOR,10K,0.1%,100mW,0603 (1608)		
1	R246	RESISTOR,1K69,0.1%,100mW,0603 (1608)		
1	R247	RESISTOR,1K47,0.1%,100mW,0603 (1608)		
1	R248	RESISTOR,402R,0.1%,100mW,0603 (1608)		
1	R249	RESISTOR,100R,0.1%,100mW,0603 (1608)		
11	R257, R278, R284, R?	RESISTOR,1K,0.1%,100mW,0603 (1608)		
1	R261	RESISTOR,42K2,0.1%,100mW,0603 (1608)		
5	R270, R302, R308, R?	RESISTOR,100K,0.1%,100mW,0603 (1608)		
2	R273, R305	RESISTOR,39K2,0.1%,100mW,0603 (1608)		
2	R286, R292	RESISTOR,5K11,0.1%,100mW,0603 (1608)		
9	R287, R?	RESISTOR,2K05,0.11%,100mW,0603 (1608)		

D

1

2

3

4

5

6

# DESIGNATORS FRONT

A

A

B

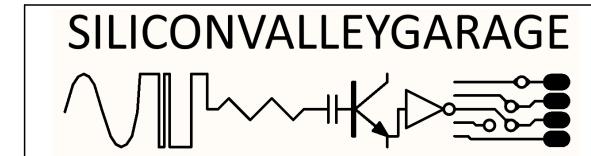
B

C

C

D

D

**SILICONVALLEYGARAGE****Project CT9042.PrjPcb**

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6

1

2

3

4

5

6

# DESIGNATORS BACK

A

A

B

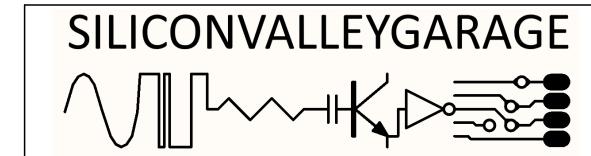
B

C

C

D

D

**SILICONVALLEYGARAGE****Project CT9042.PrjPcb**

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6

1

2

3

4

5

6

# PASTE MASK TOP

A

A

B

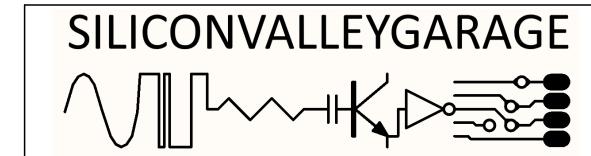
B

C

C

D

D



**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6

1

2

3

4

5

6

# PASTE MASK BACK

A

A

B

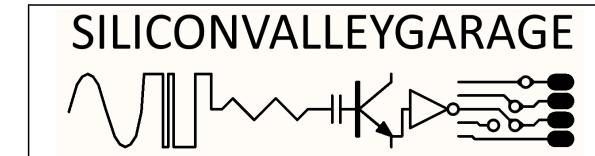
B

C

C

D

D



**Project CT9042.PrjPcb**  
Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6