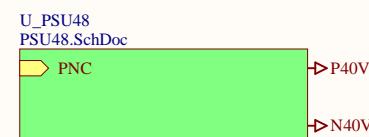
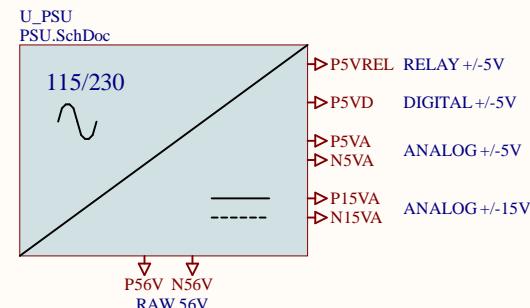


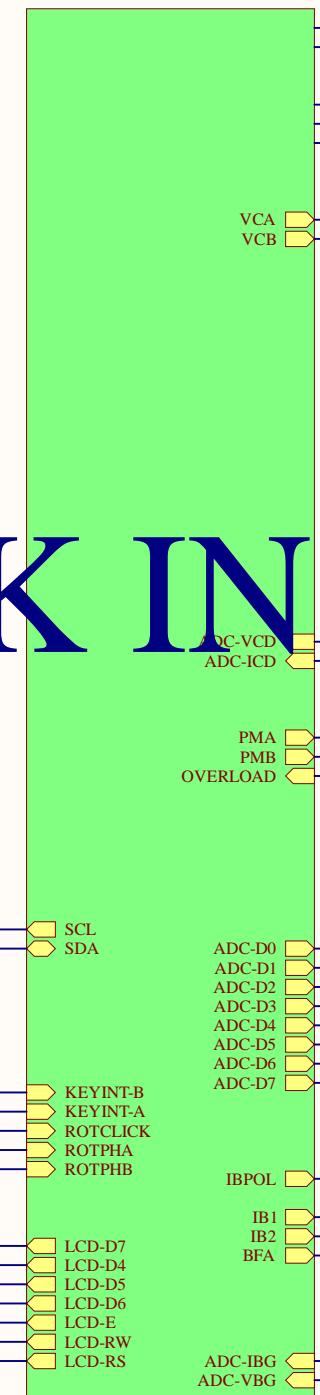
## CT9042.PrjPcb

A  
Realistic ViewD  
Document Creation Date: 8/28/2025D  
Design : free\_electron

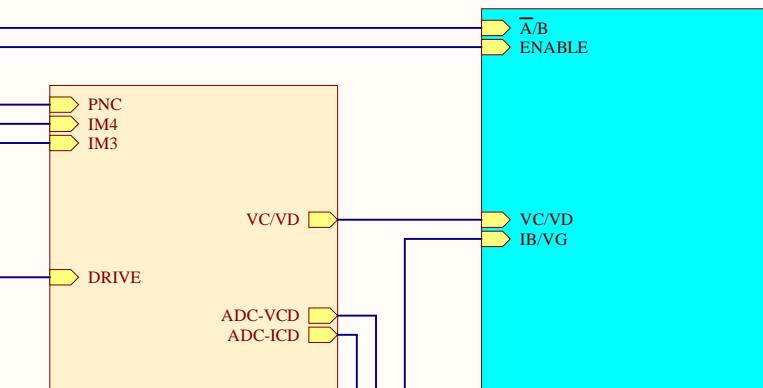
1 2 3 4 5 6



**U\_PROCESSOR**  
PROCESSOR.SchDoc



**U\_POWERAMP**  
POWERAMP.SchDoc

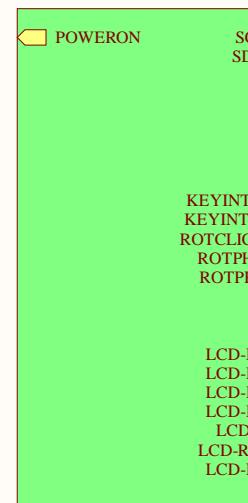


**U\_POWERMUX**  
POWERMUX.SchDoc

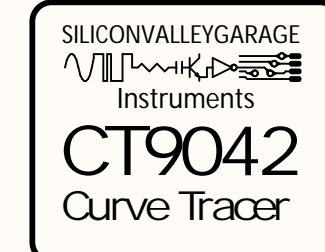
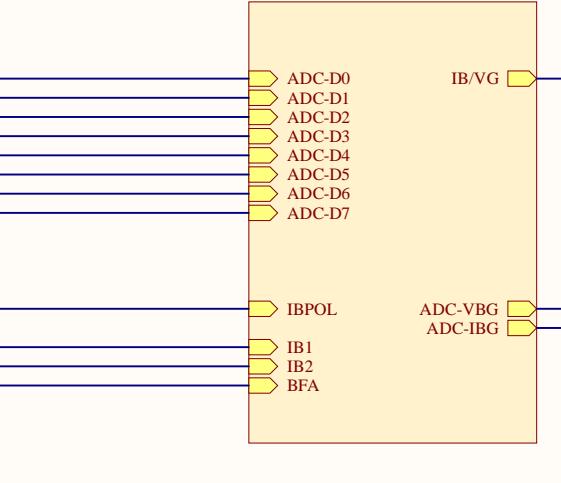
SILICONVALLEYGARAGE  
Instruments  
**CT9042**  
Curve Tracer

# WORK IN PROGRESS

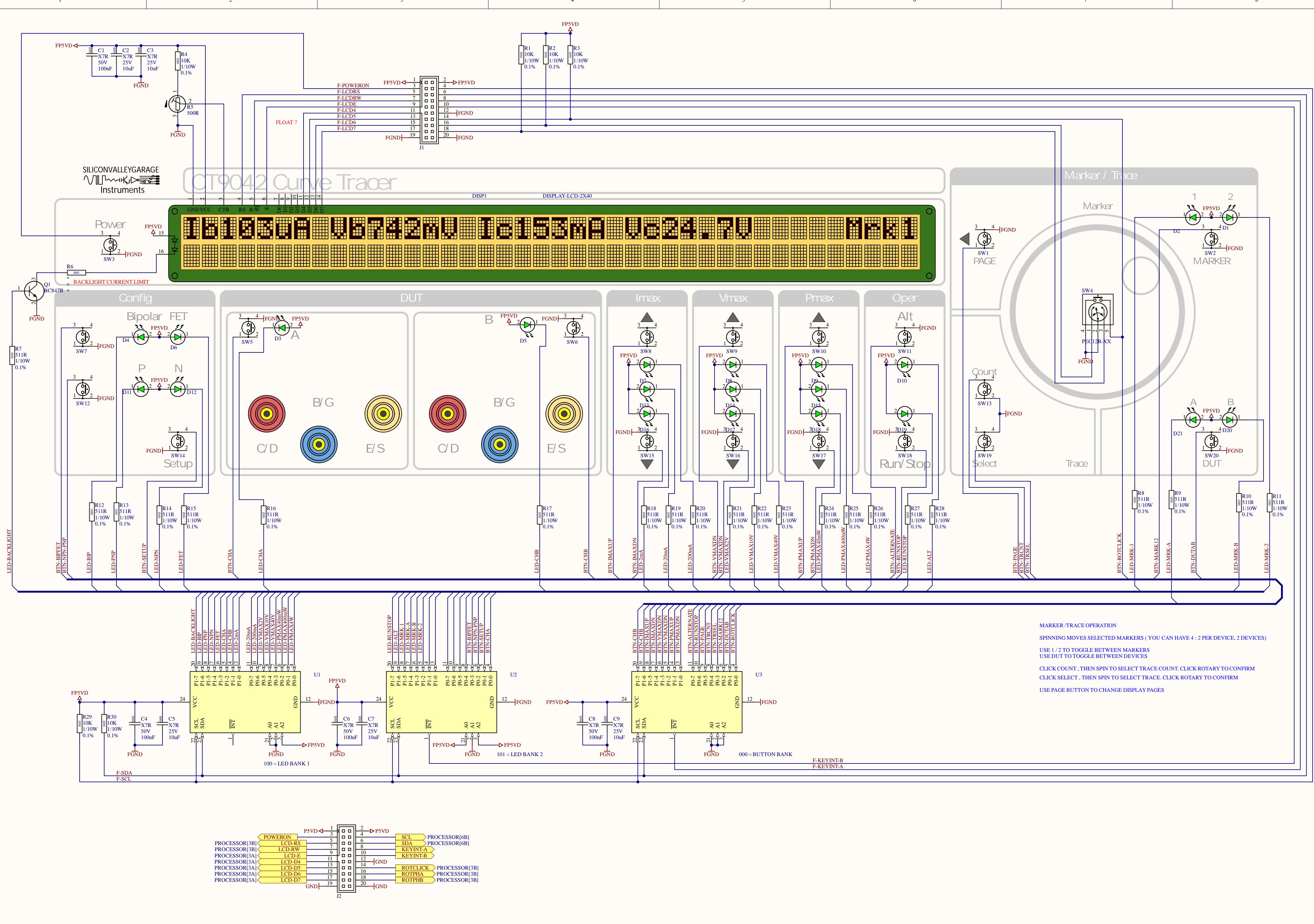
**U\_FrontPanel**  
FrontPanel.SchDoc



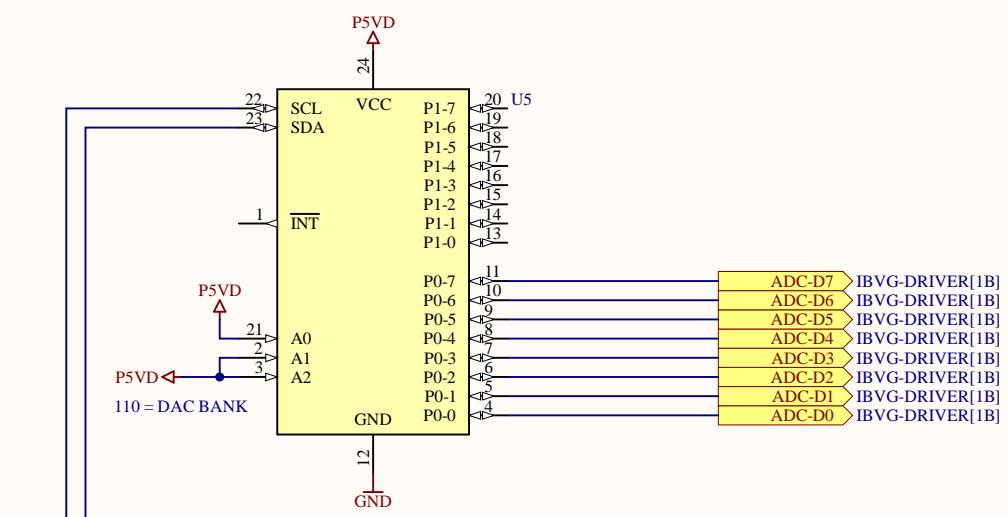
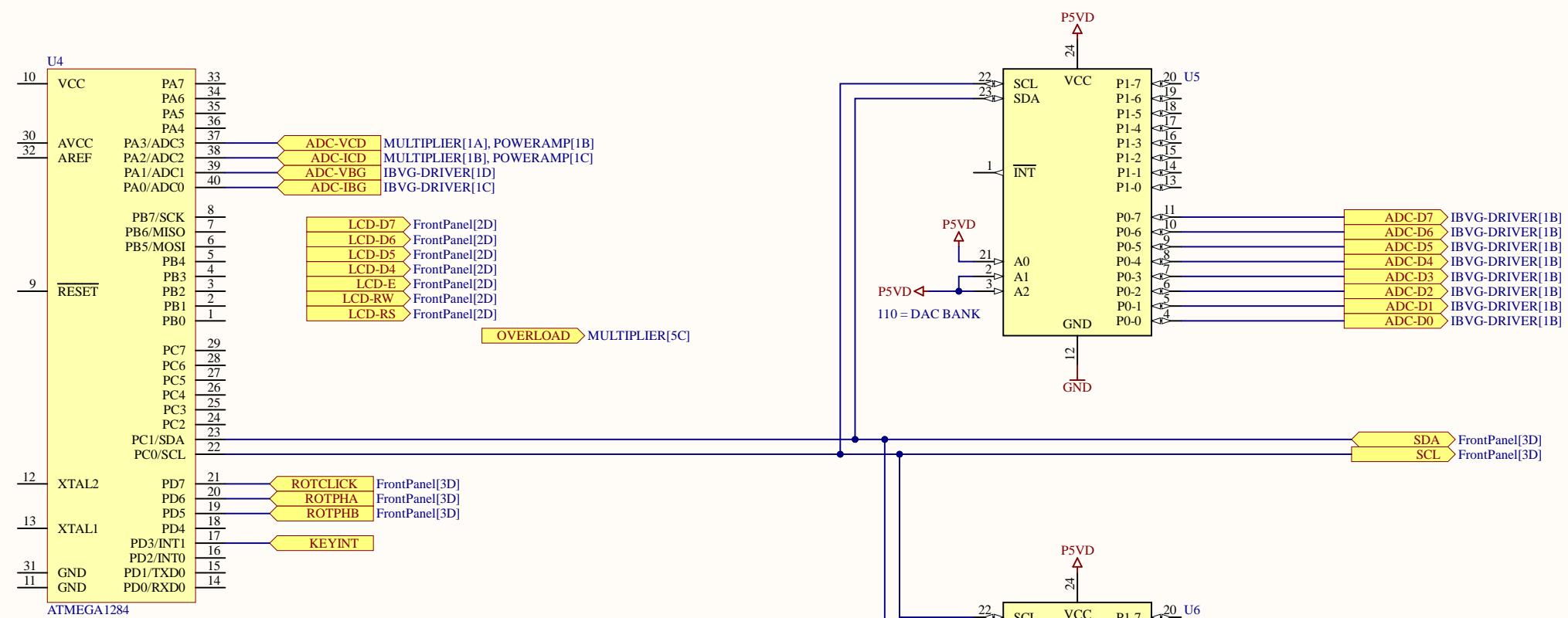
**U\_MULTIPLIER**  
MULTIPLIER.SchDoc



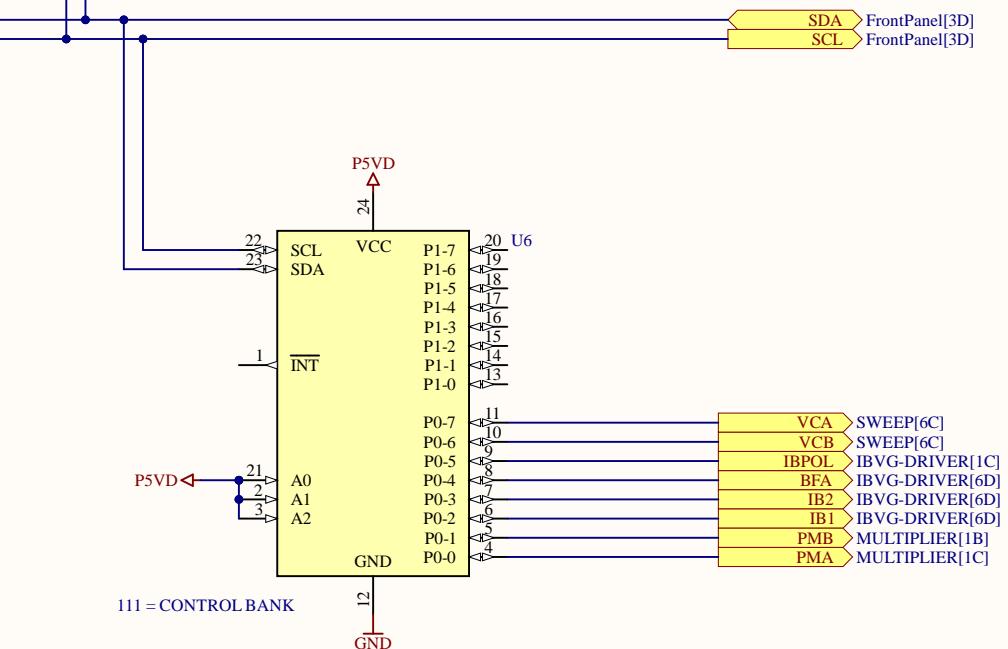
1 2 3 4 5 6



A



B



C

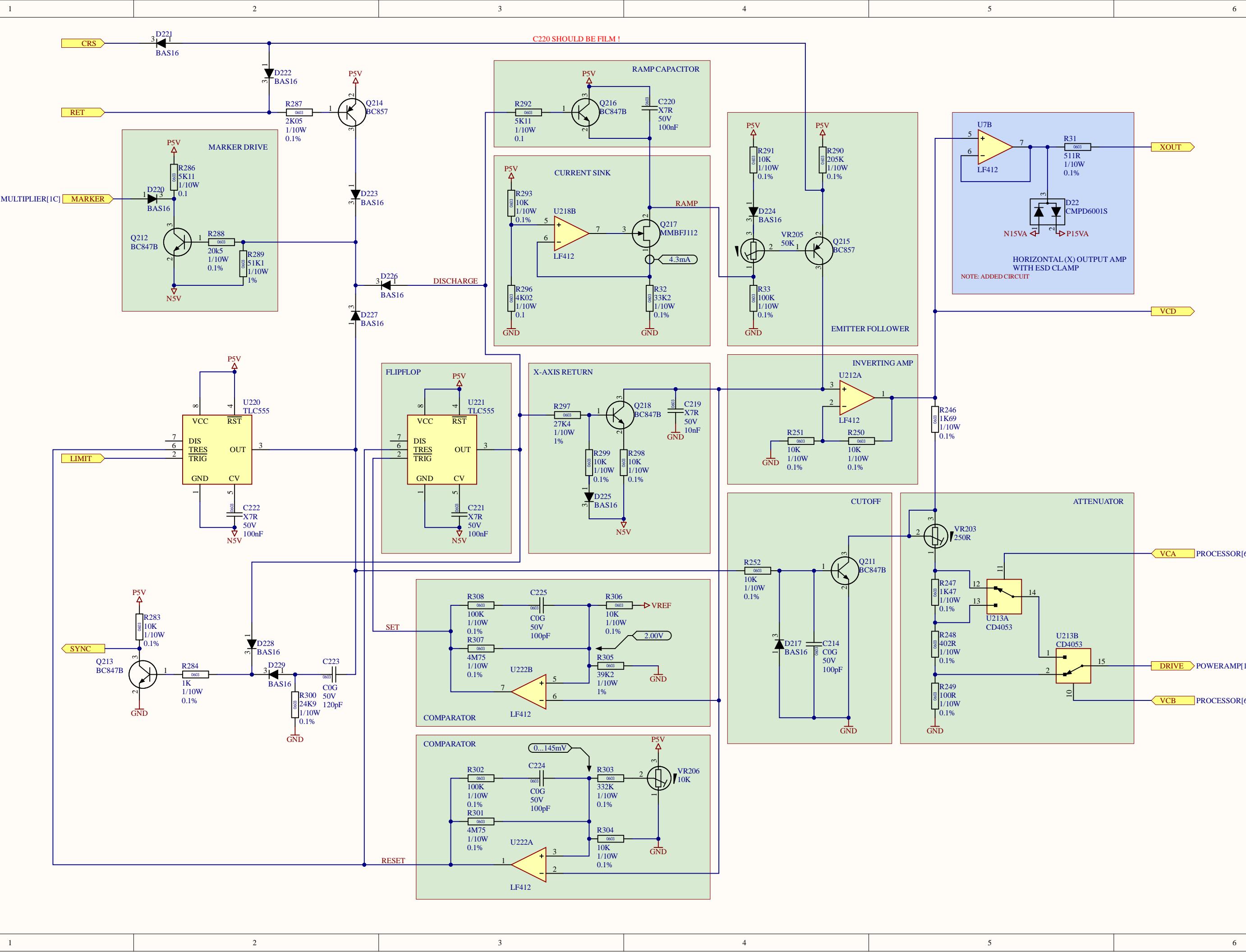
D

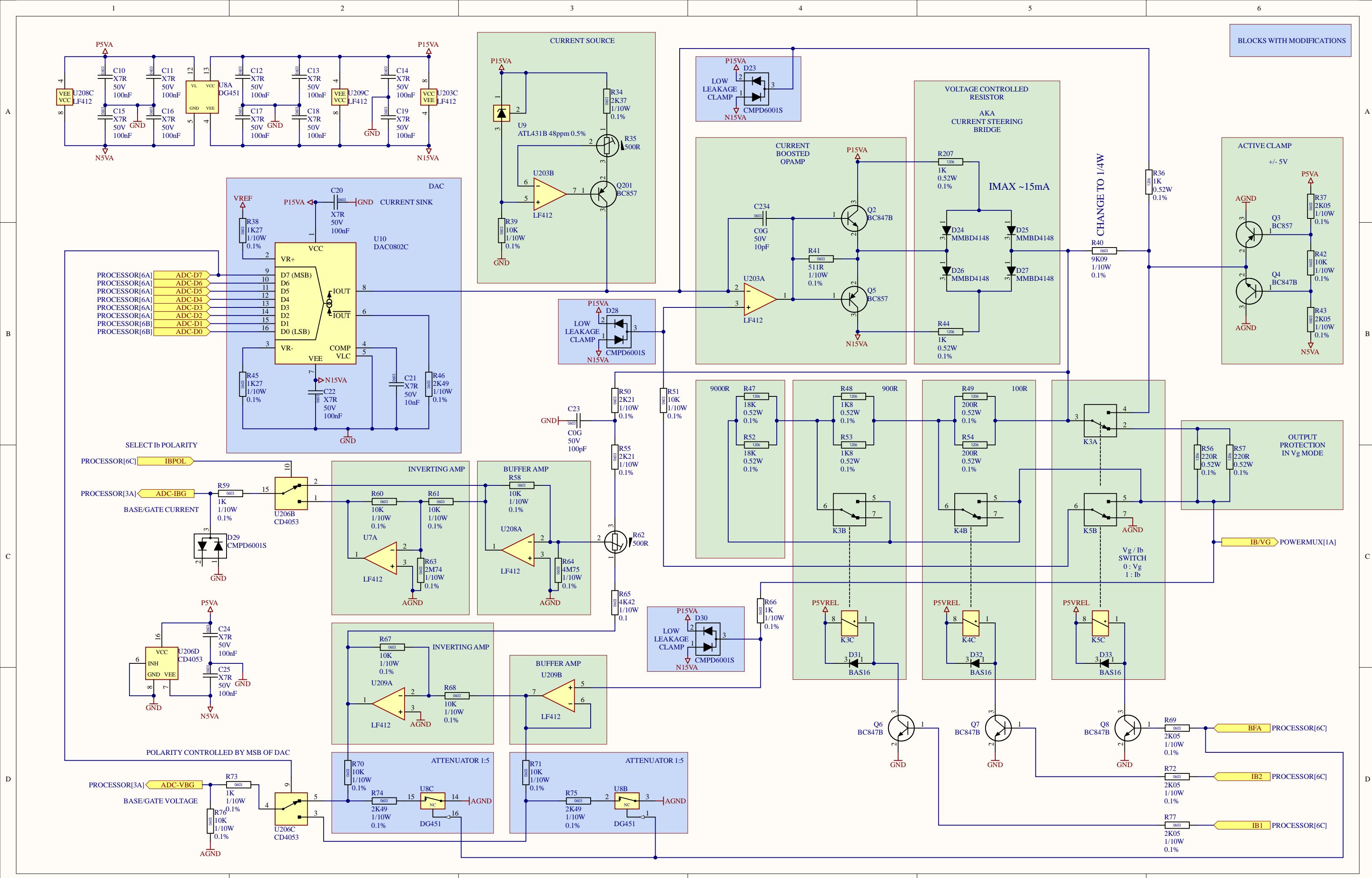
A

B

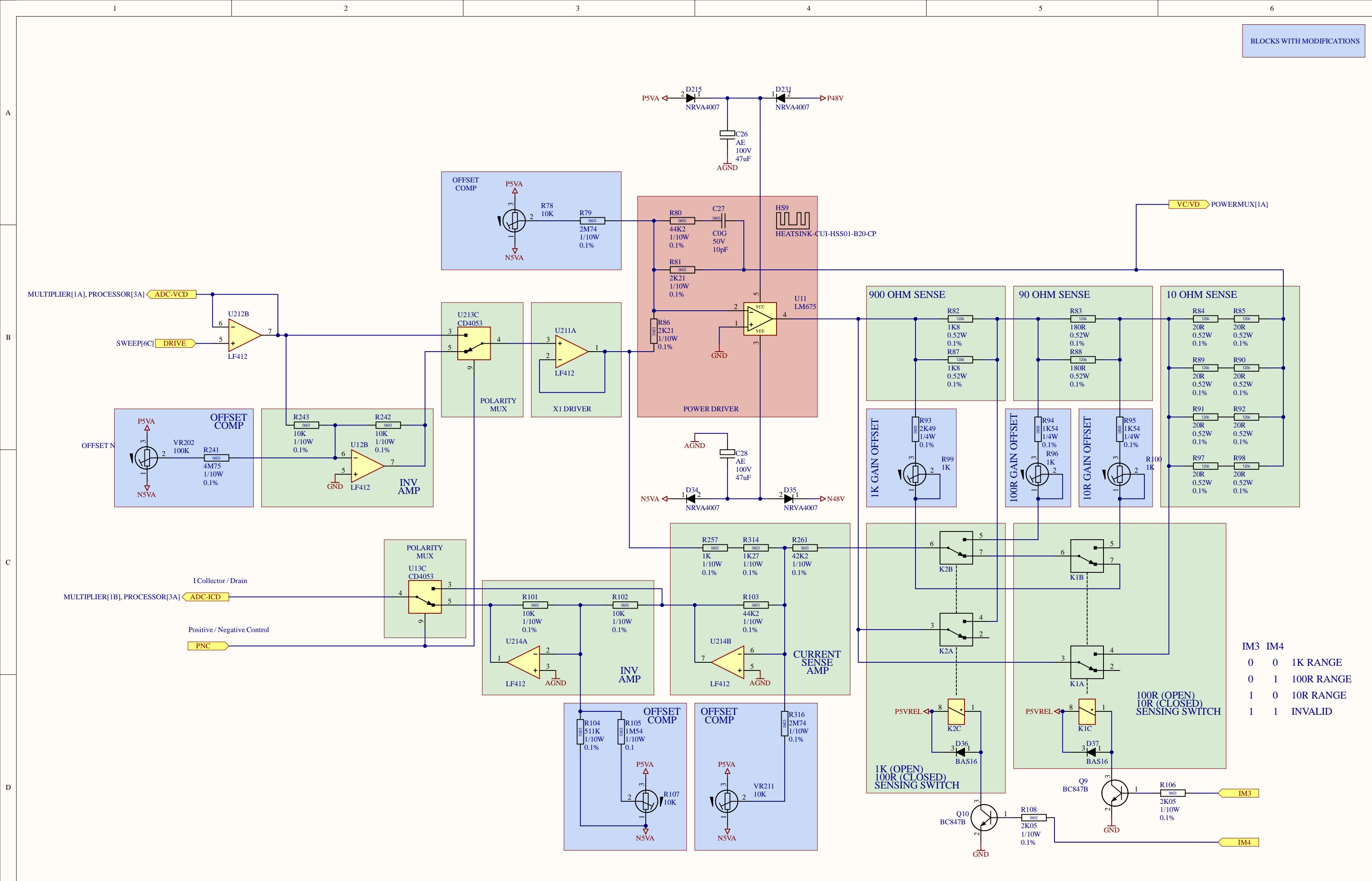
C

D

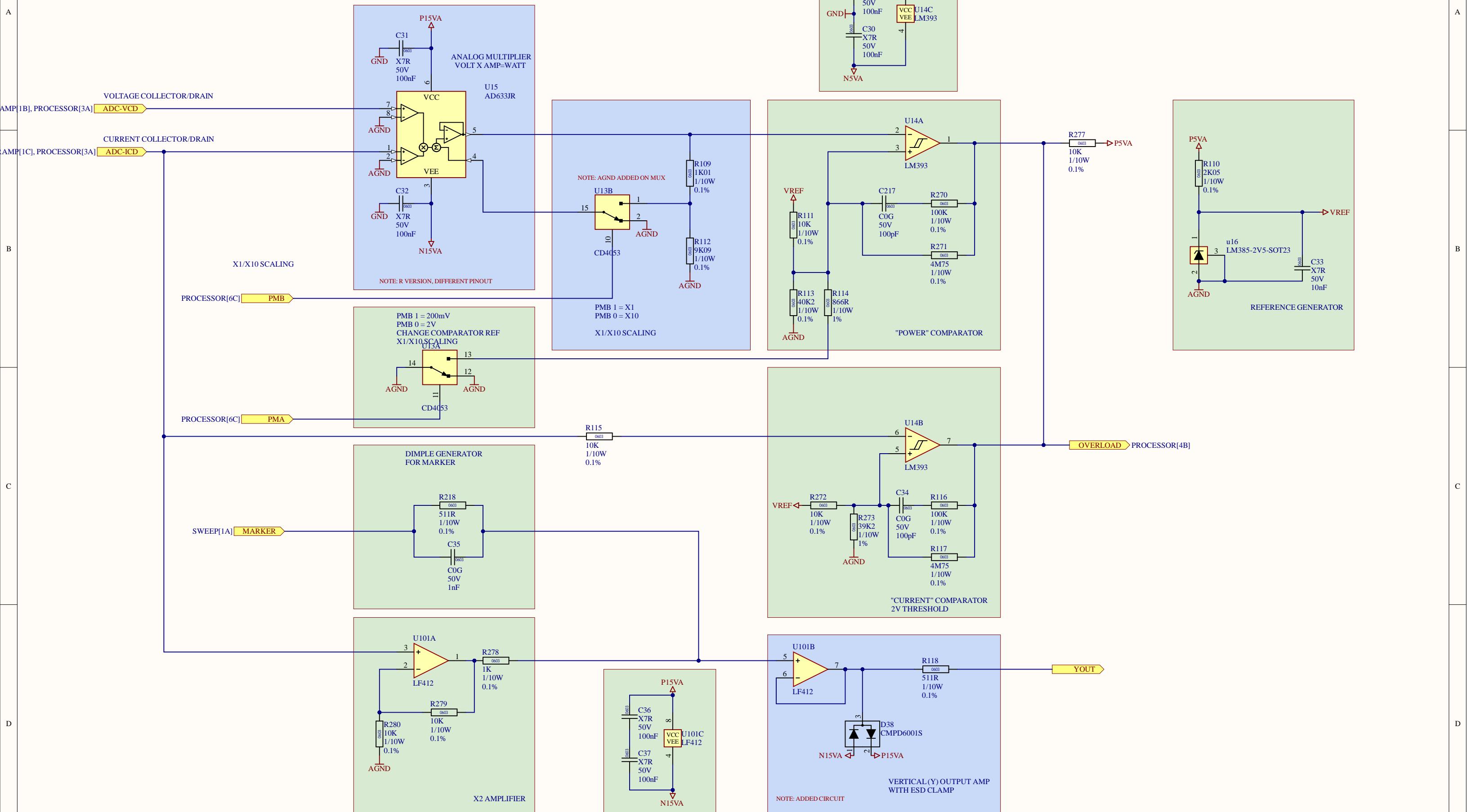


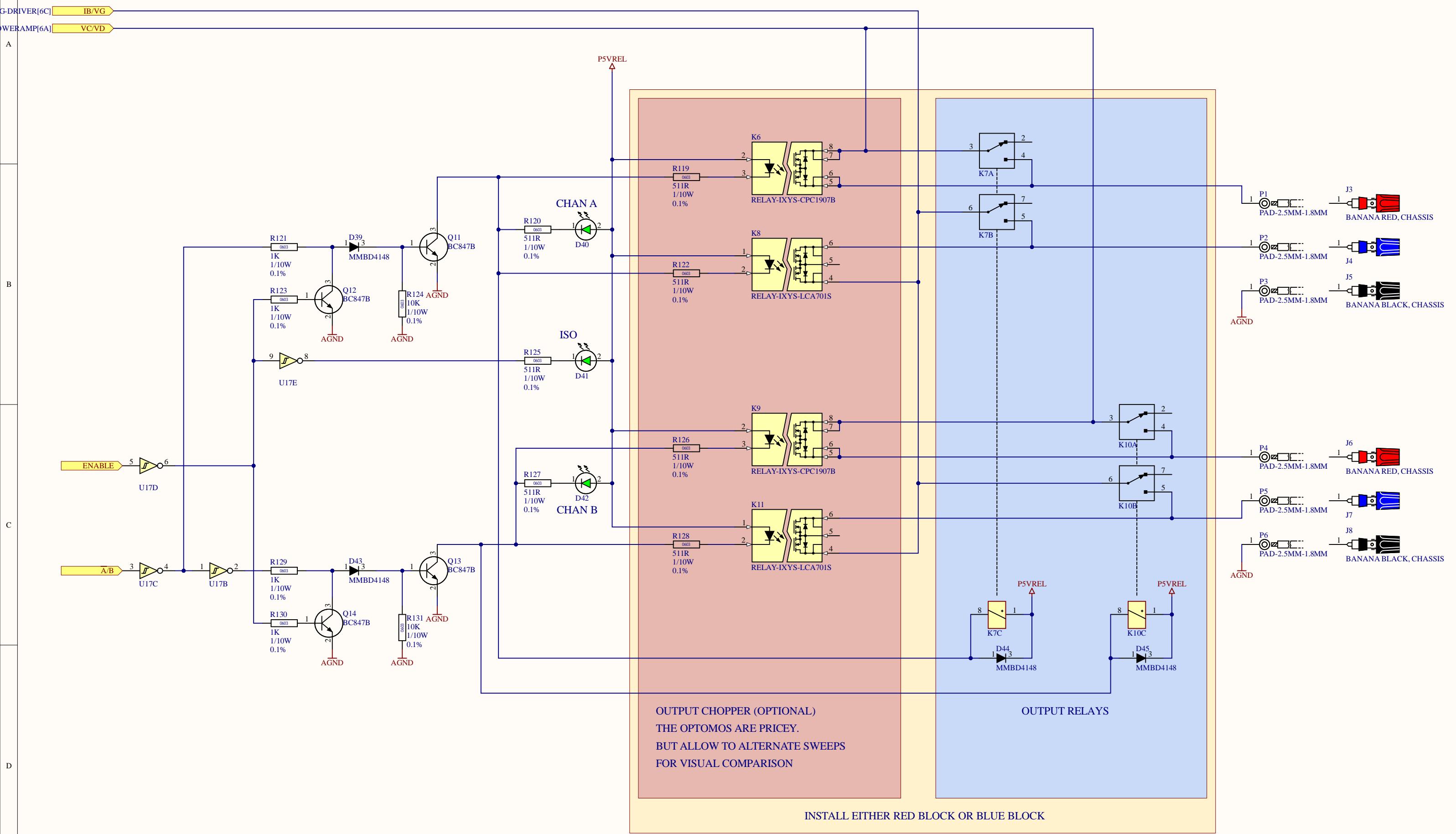


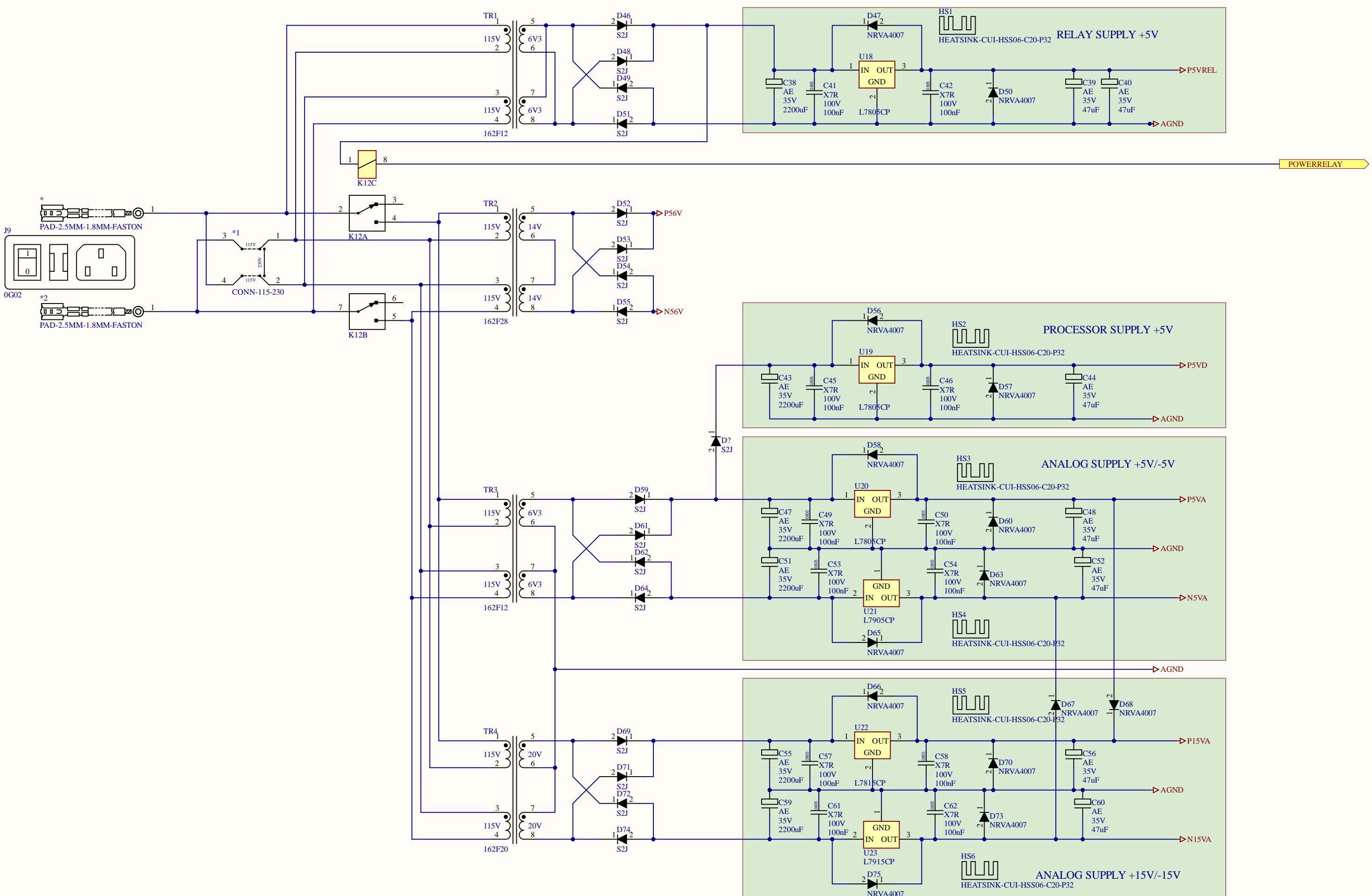
BLOCKS WITH MODIFICATIONS



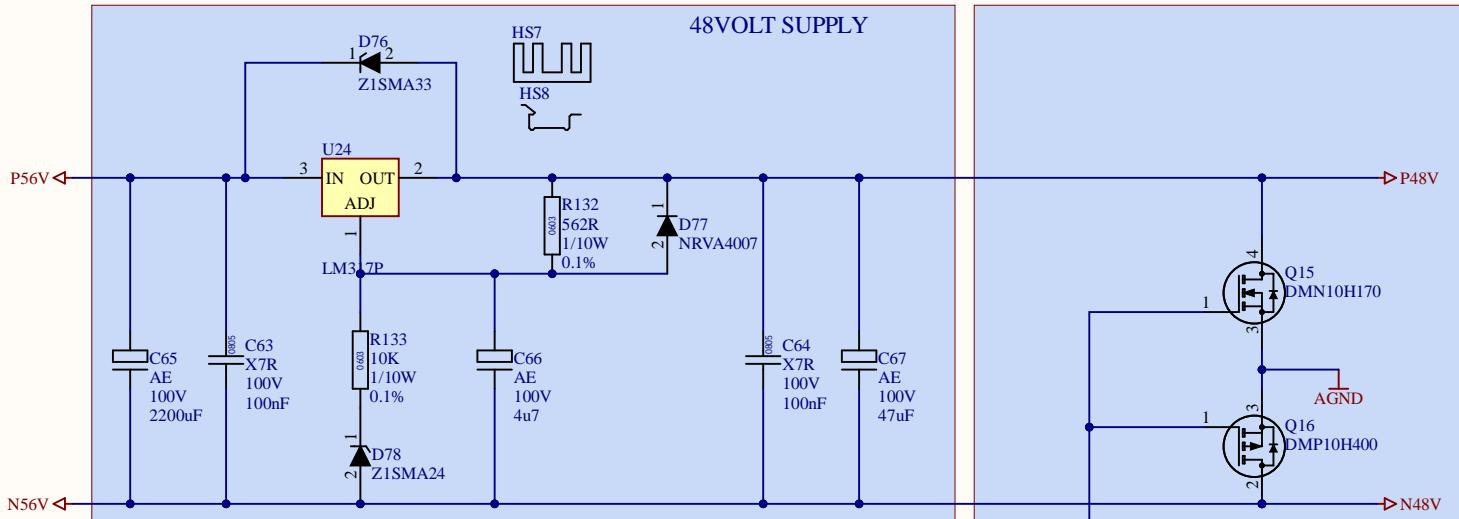
BLOCKS WITH MODIFICATIONS



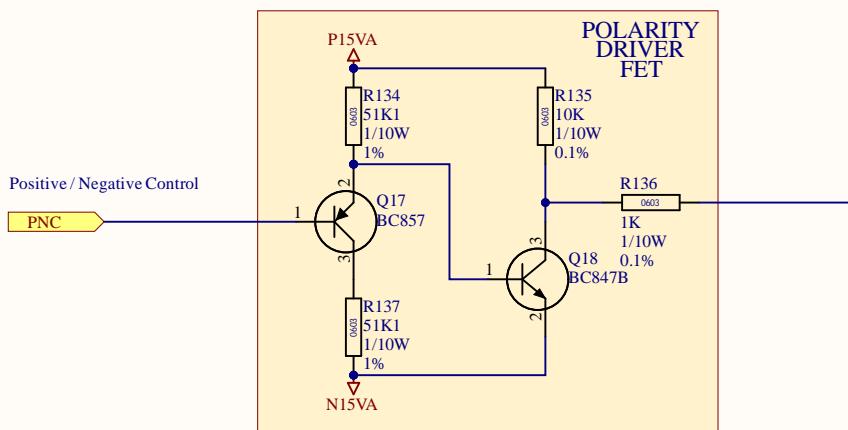




## BLOCKS WITH MODIFICATIONS



THIS MECHANISM PUSHES EITHER THE POSITIVE RAIL TO 40 VOLTS OR THE NEGATIVE RAIL TO -40 VOLTS. THE POWER AMP EITHER RUNS FROM +5 TO -40 VOLTS, OR FROM -5 TO +40 VOLTS



1

2

3

4

5

6

# CT9042.PrjPcb

A

A

B

B

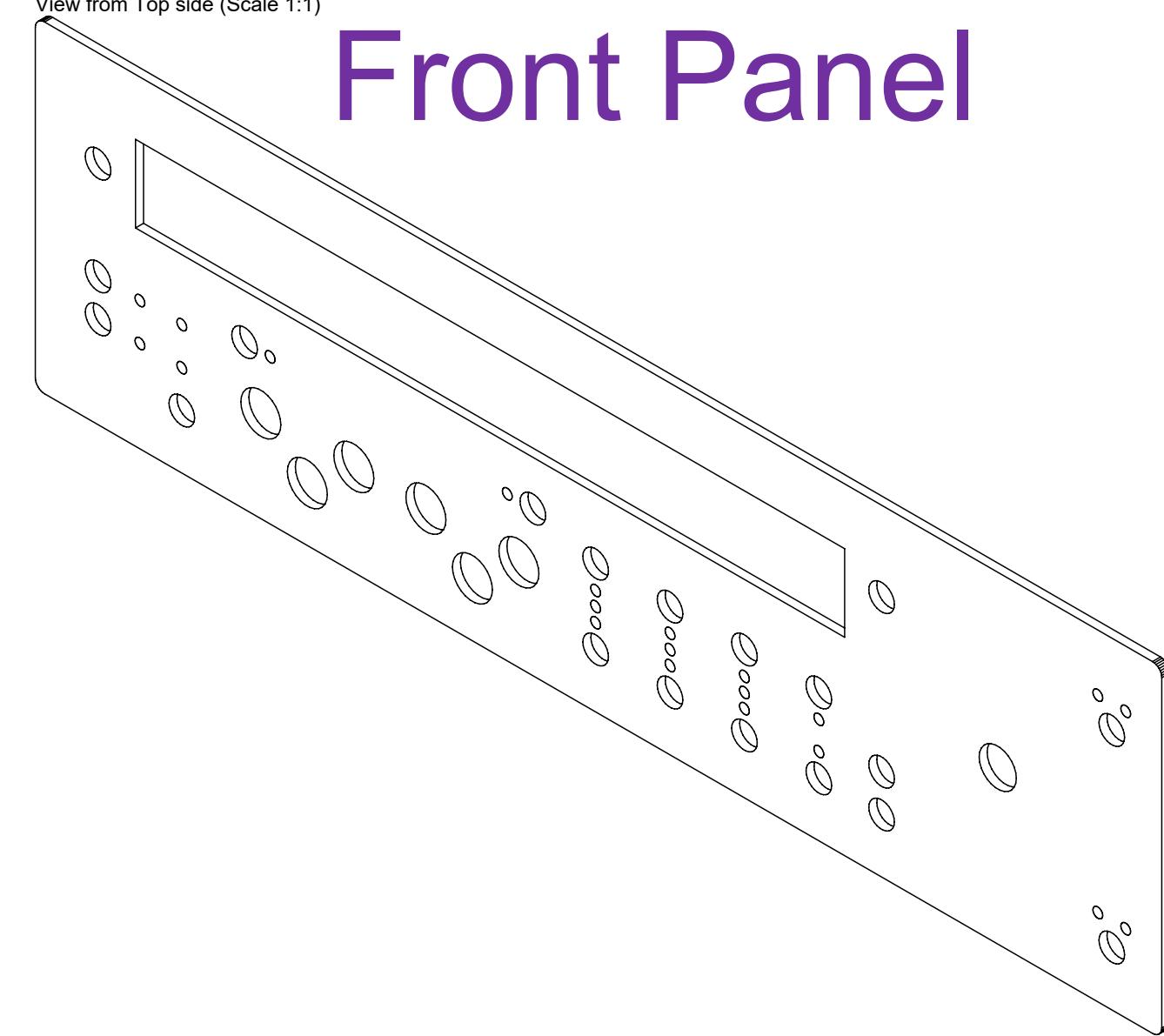
C

C

D

D

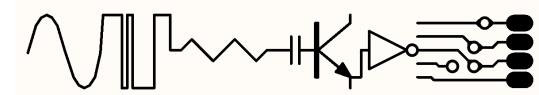
View from Top side (Scale 1:1)



## Front Panel

Design : free\_electron

SILICONVALLEYGARAGE



1

2

3

4

5

6

# GENERAL

## GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.
3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER
4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2
5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

## MATERIALS

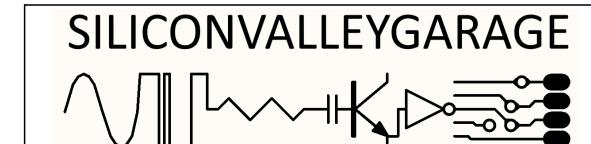
7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

## STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

## QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY



Project CT9042.PrjPcb

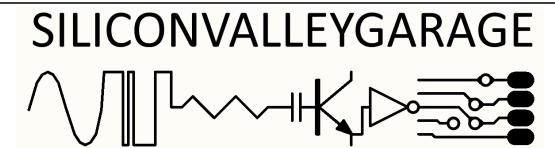
Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER STACK

## Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material Type	Gerber Dk	Weight	Constructions	Df	Resin
A		Top Overlay		Legend GTO					
B	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask GTS	3.5			
C	<b>Copper</b>	<b>Top Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal GTL</b>	<b>1oz</b>			
D		Prepreg	0.102mm(4.000mil)	Core-009	Dielectric	4.5	1-2116	0.02	47%
			1.450mm(57.087mil)	FR-4	Dielectric	4.8			
		Prepreg	0.102mm(4.000mil)	Core-009	Dielectric	4.5	1-2116	0.02	47%
	<b>Copper</b>	<b>Bottom Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal GBL</b>	<b>1oz</b>			
	Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask GBS	3.5			
		Bottom Overlay		Legend GBO					
	Total thickness: 1.745mm(68.687mil)								



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
▽	21	2.100mm(82.677mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
□	19	5.500mm(216.535mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
☆	1	8.000mm(314.961mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
○	6	8.600mm(338.583mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
47 Total											

A

A

B

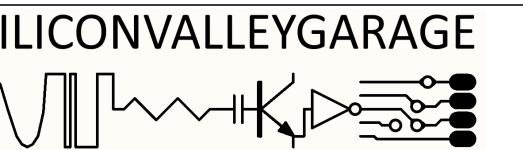
B

C

C

D

D



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

19

20

21

22

23

24

# DRILL DRAWING

A

A

Drill Drawing View (Scale 1.5:1)



B

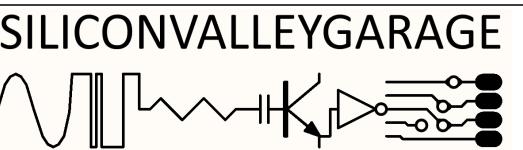
B

C

C

D

D



**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

19

20

21

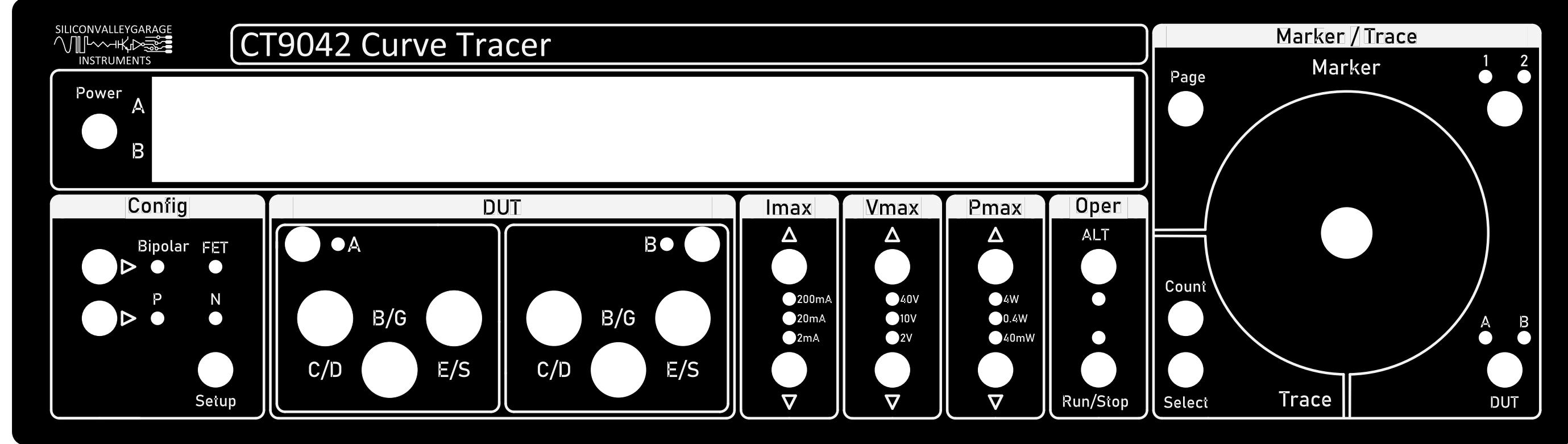
22

23

24

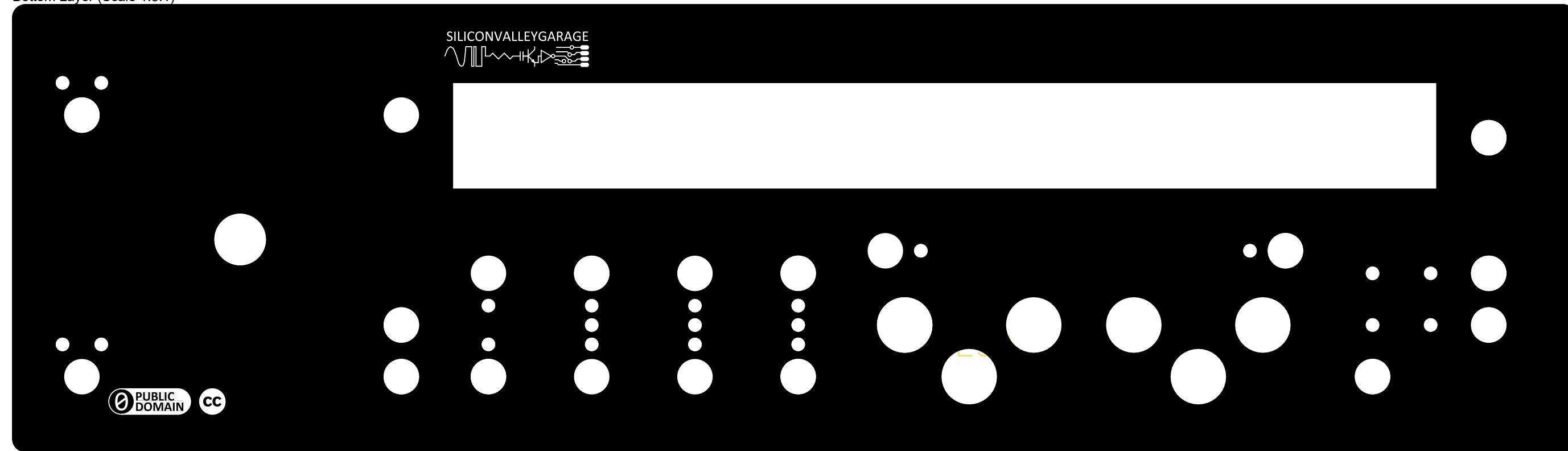
# COMPOSITE VIEW FRONT

Top Layer (Scale 1.5:1)



## COMPOSITE VIEW BACK

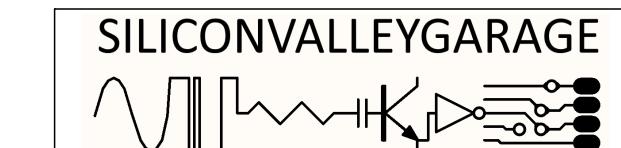
Bottom Layer (Scale 1.5:1)



# LAYER VIEW : TOP LAYER

Top Layer (Scale 1.5:1)

WORK IN PROGRESS



**Project CT9042.PrjPcb**

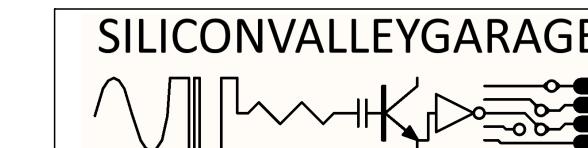
Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER VIEW : BOTTOM LAYER

Bottom Layer (Scale 1.5:1)

MORK IN PROGRESS



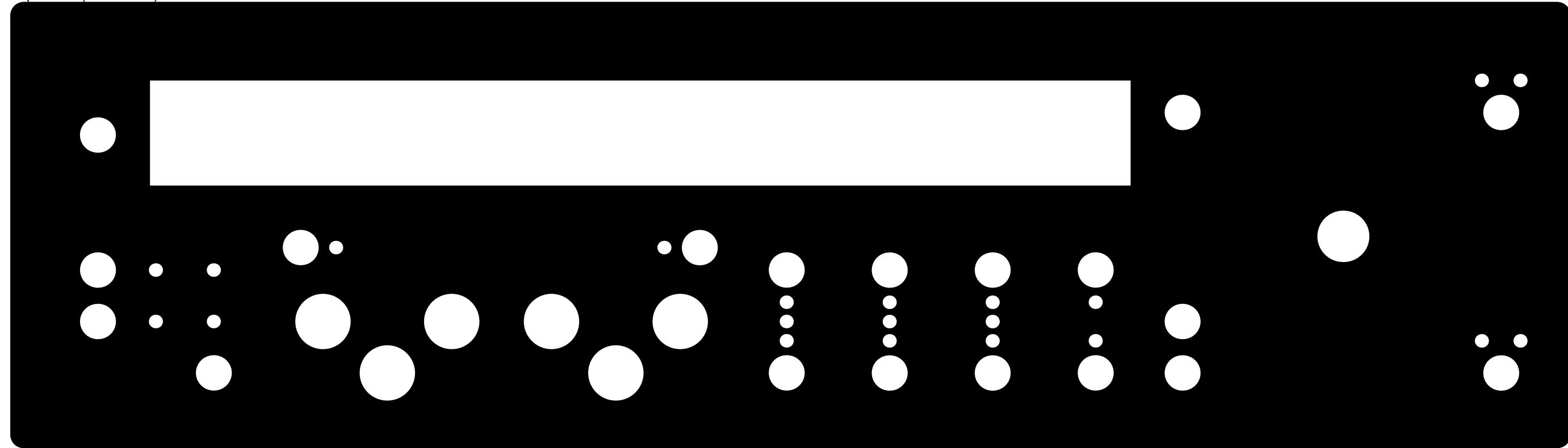
**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER VIEW : TOP SOLDER MASK

Top Solder (Scale 1.5:1)



A

A

B

B

C

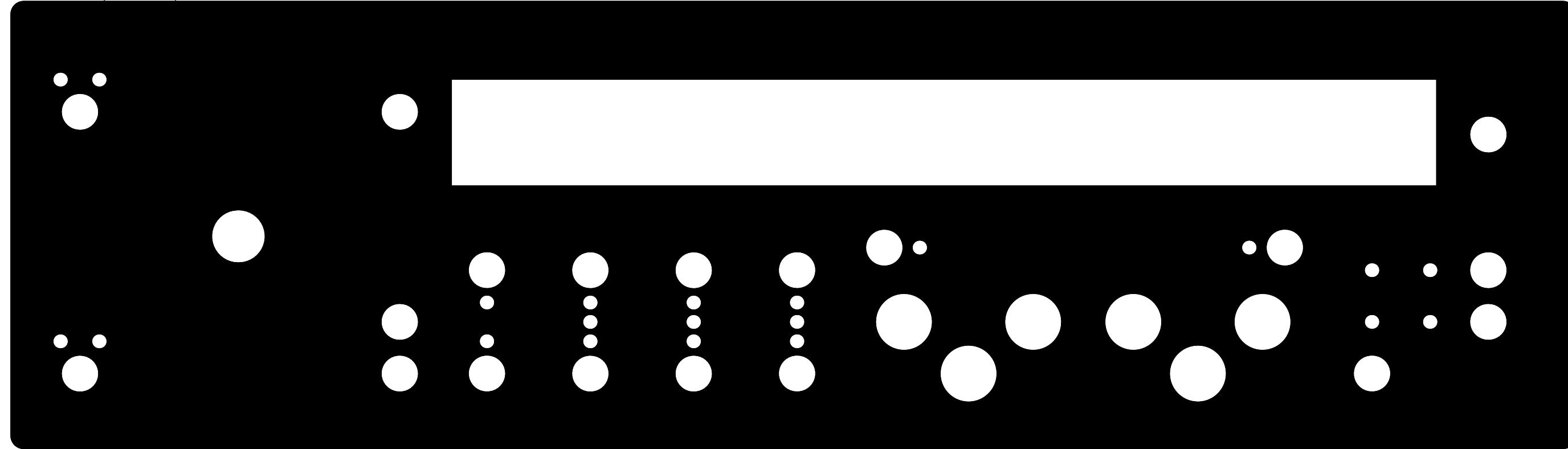
C

D

D

# LAYER VIEW : BOTTOM SOLDER MASK

Bottom Solder (Scale 1.5:1)



A

A

B

B

C

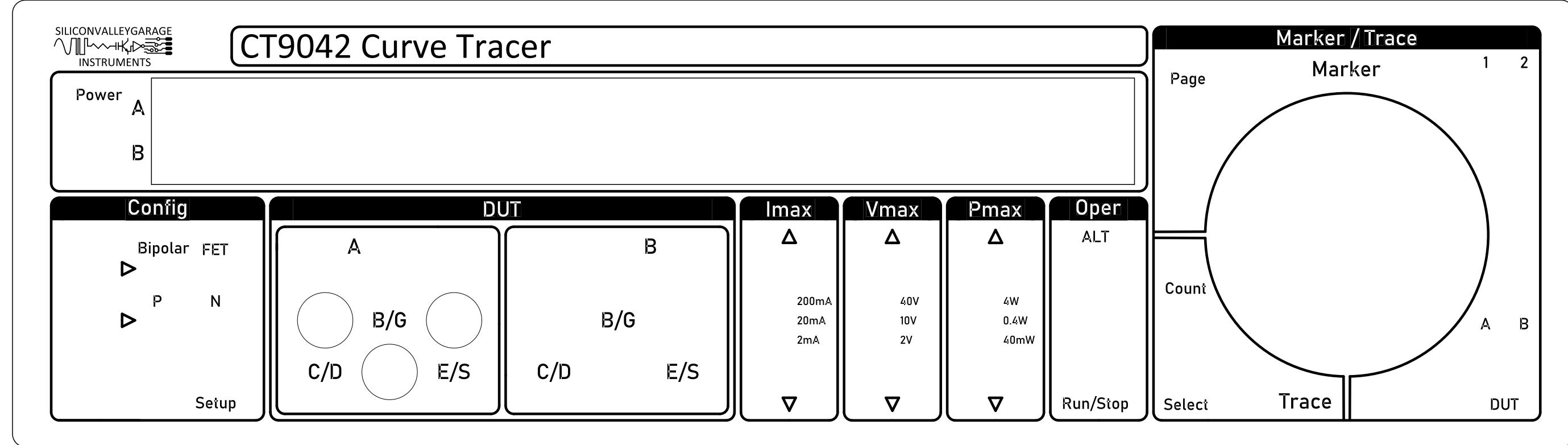
C

D

D

# LAYER VIEW : TOP SILKSCREEN (LEGEND)

Top Overlay (Scale 1.5:1)

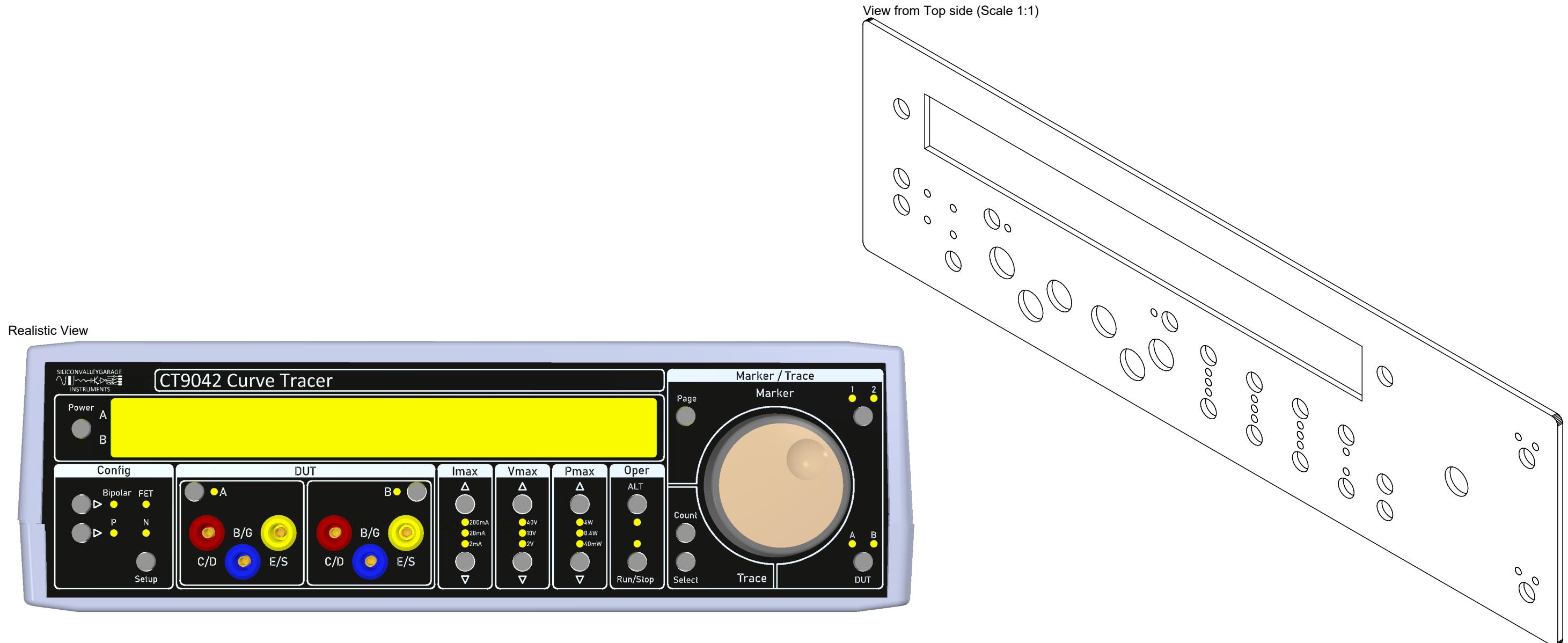


# LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

Bottom Overlay (Scale 1.5:1)



# Front Board



Document Creation Date: 8/28/2025

Design : free\_electron

# GENERAL

## GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
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5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

## MATERIALS

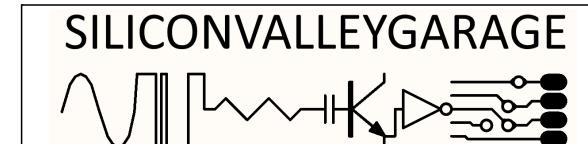
7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

## STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

## QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY



Project CT9042.PjPcb

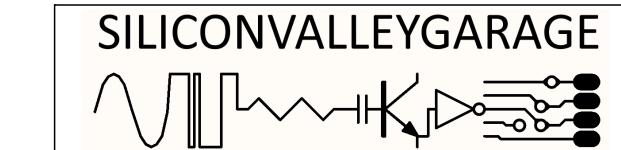
Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER STACK

## Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material Type	Gerber Dk	Weight	Constructions	Df	Resin
A	Top Overlay			Legend	GTO				
B	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5		
C	<b>Copper</b>	<b>Top Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal</b>	<b>GTL</b>	<b>1oz</b>		
D	Prepreg		0.102mm(4.000mil)	Core-009	Dielectric		4.5	1-2116	0.02 47%
	CF-004	Layer 1	0.035mm(1.378mil)		Signal	G1	1oz		
			1.450mm(57.087mil)	FR-4	Dielectric		4.8		
	CF-004	Layer 2	0.035mm(1.378mil)		Signal	G2	1oz		
	Prepreg		0.102mm(4.000mil)	Core-009	Dielectric		4.5	1-2116	0.02 47%
	<b>Copper</b>	<b>Bottom Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal</b>	<b>GBL</b>	<b>1oz</b>		
	Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5		
	Bottom Overlay			Legend	GBO				
	Total thickness: 1.815mm(71.443mil)								



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
□	125	1.000mm(39.370mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
▽	2	2.600mm(102.362mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✖	2	3.200mm(125.984mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✖	6	10.000mm(393.701mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
135 Total											

A

A

B

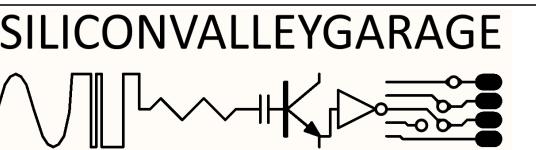
B

C

C

D

D



Project CT9042.PjPcb

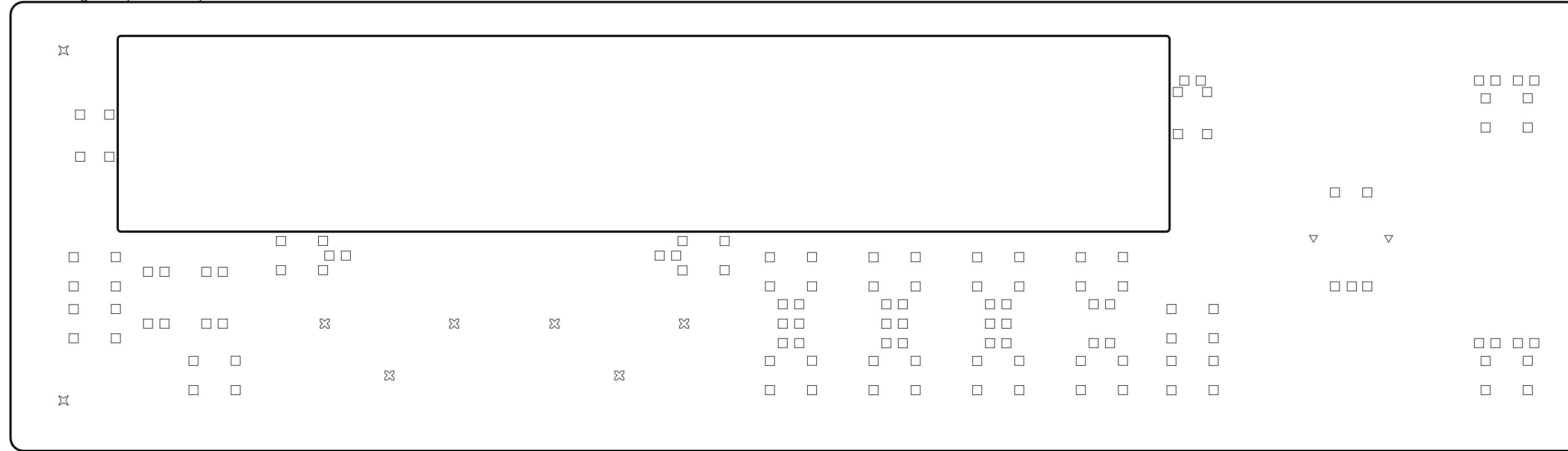
Version: | Variant [No Variations]

FABRICATION DRAWING

# DRILL DRAWING

A

Drill Drawing View (Scale 1.5:1)



A

B

B

C

C

D

D

25

26

27

28

29

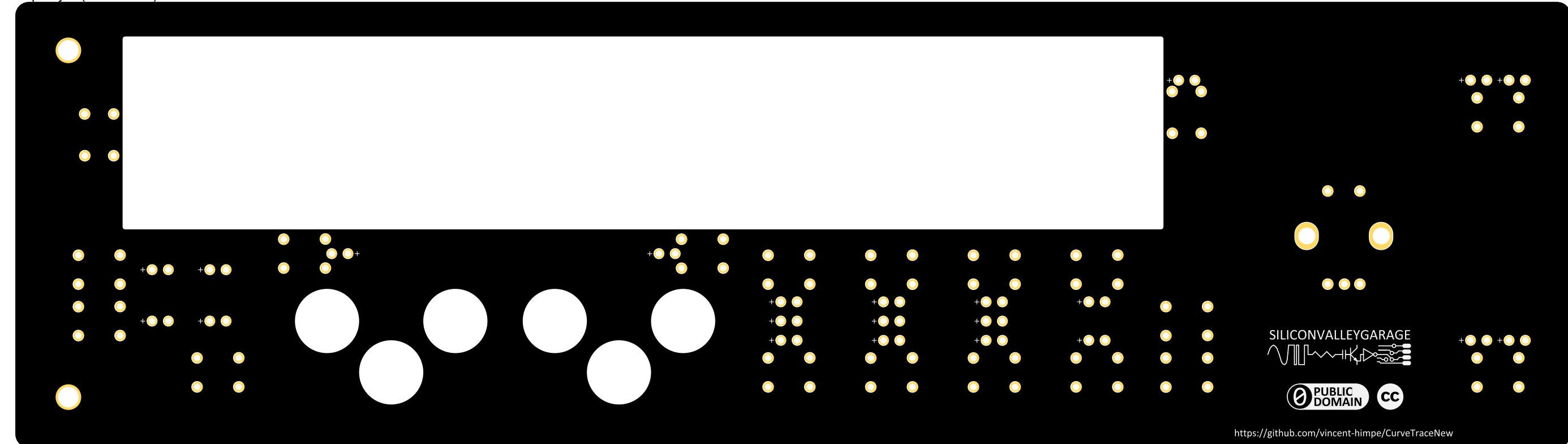
30

# COMPOSITE VIEW FRONT

A

A

Top Layer (Scale 1.5:1)



B

B

C

C

D

D

31

32

33

34

35

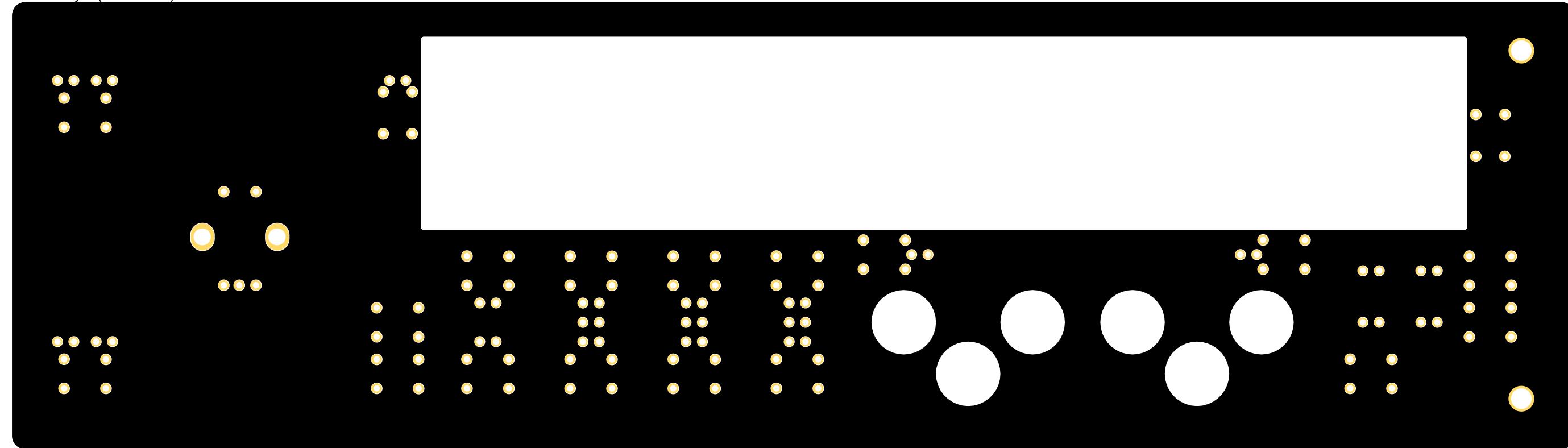
36

# COMPOSITE VIEW BACK

A

A

Bottom Layer (Scale 1.5:1)



B

B

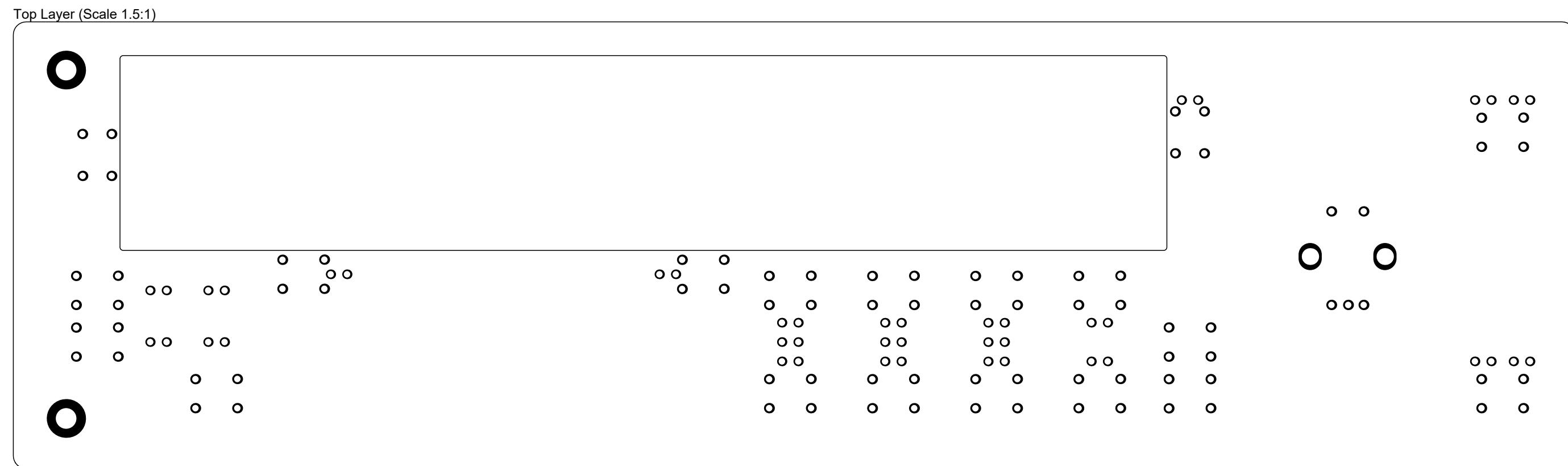
C

C

D

D

# LAYER VIEW : TOP LAYER

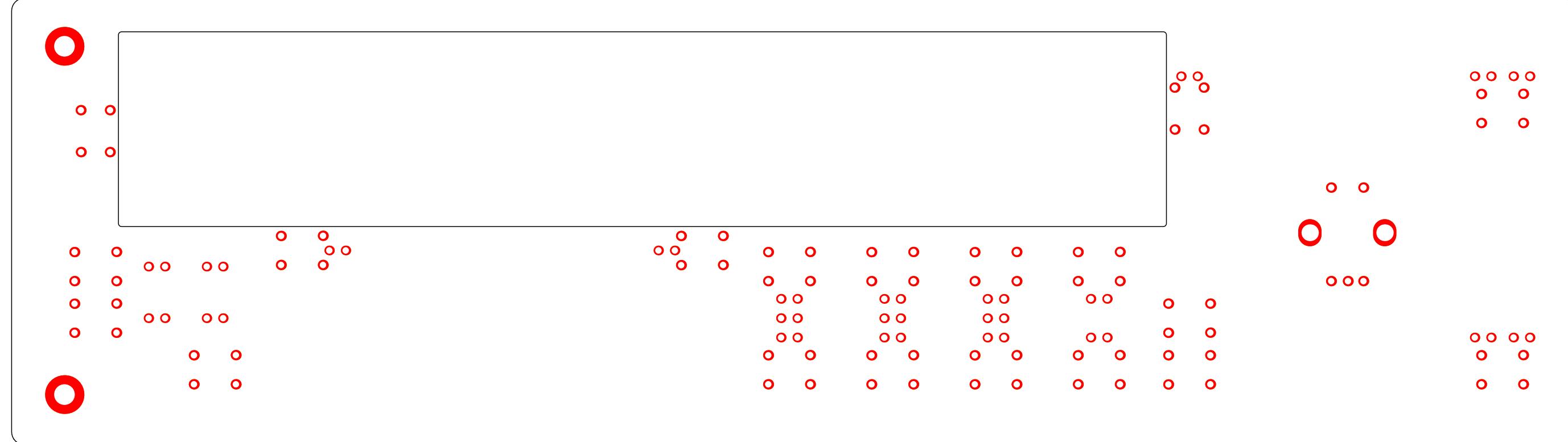


## LAYER VIEW : MID LAYER 1

A

A

Layer 1 (Scale 1.5:1)



B

B

C

C

D

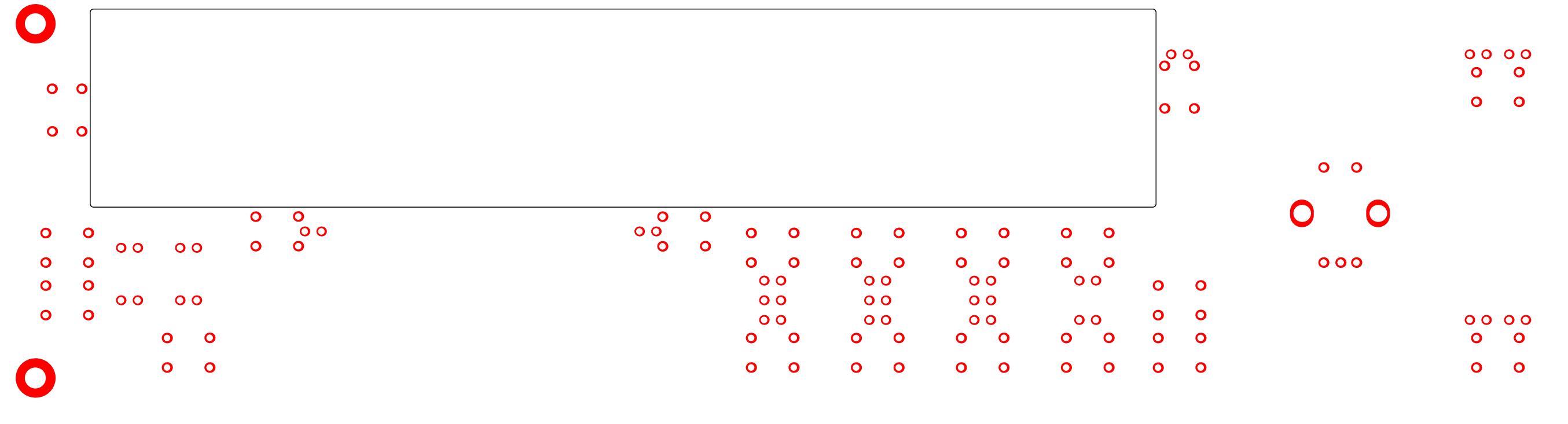
D

## LAYER VIEW : MID LAYER 2

A

A

Layer 2 (Scale 1.5:1)



B

B

C

C

D

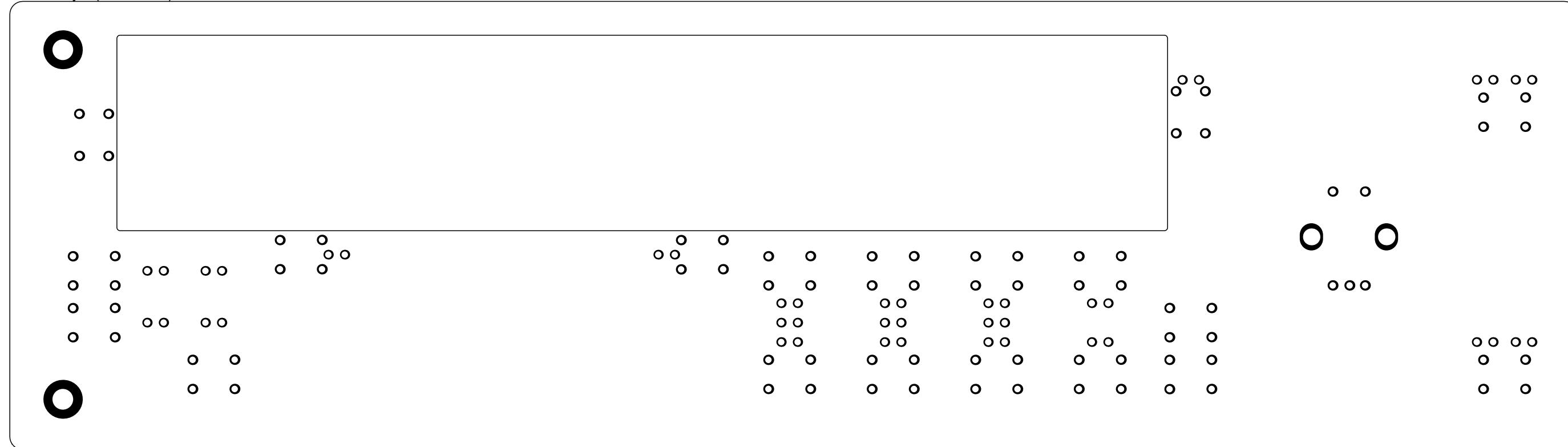
D

## LAYER VIEW : BOTTOM LAYER

A

A

Bottom Layer (Scale 1.5:1)



B

B

C

C

D

D

61

62

63

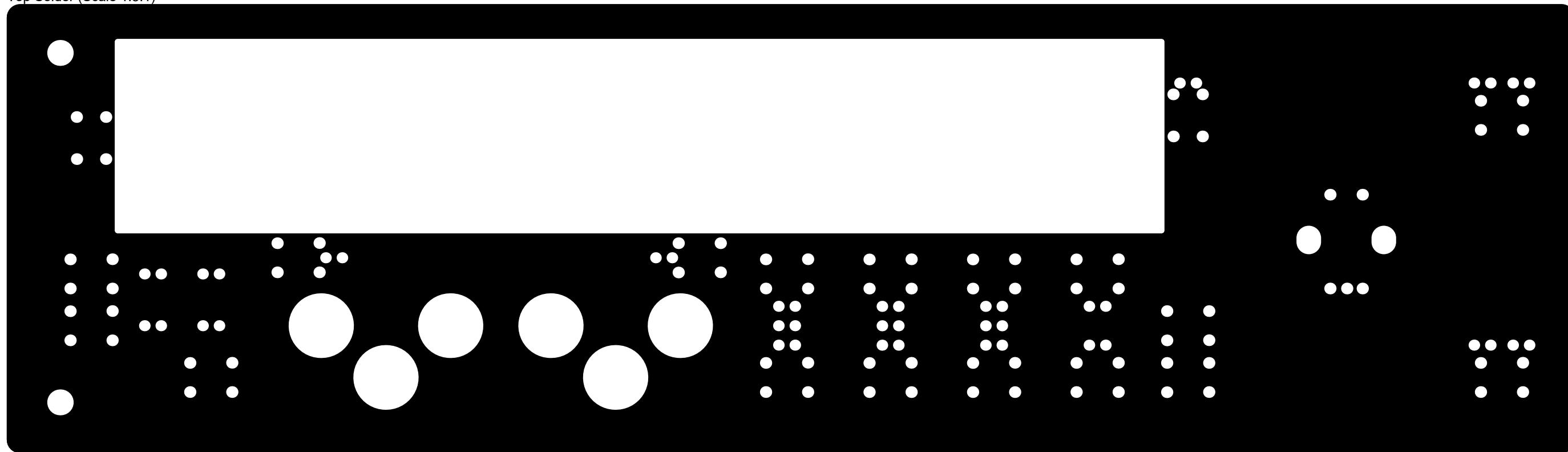
64

65

66

# LAYER VIEW : TOP SOLDER MASK

Top Solder (Scale 1.5:1)



A

A

B

B

C

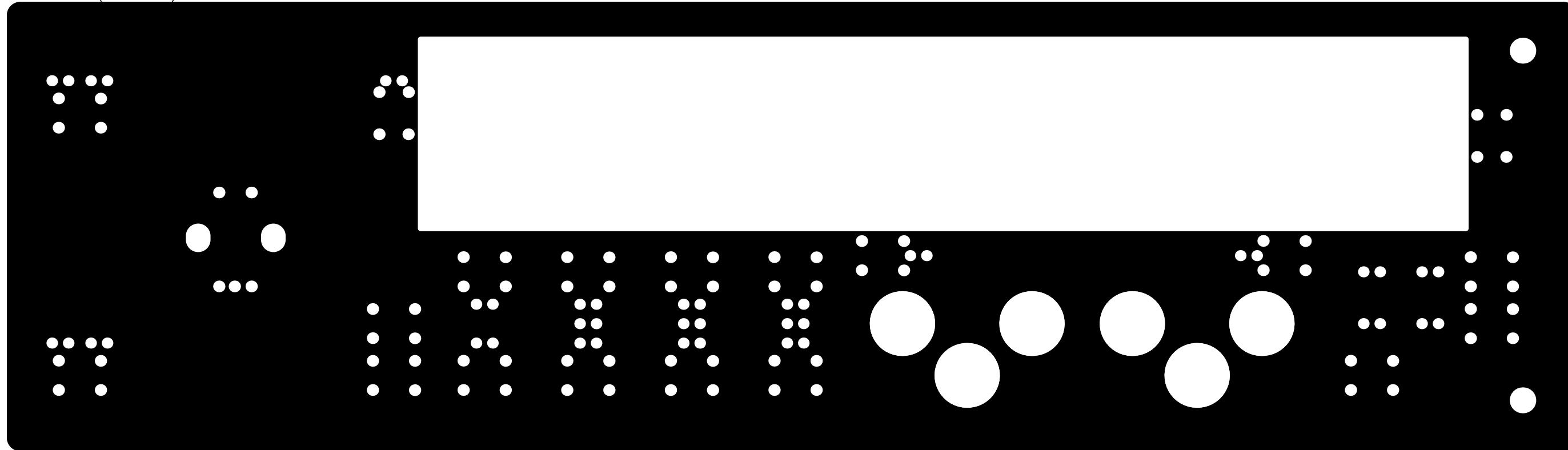
C

D

D

# LAYER VIEW : BOTTOM SOLDER MASK

Bottom Solder (Scale 1.5:1)



A

A

B

B

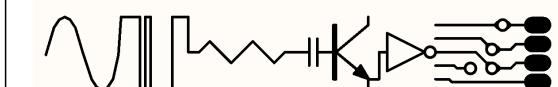
C

C

D

D

SILICONVALLEYGARAGE



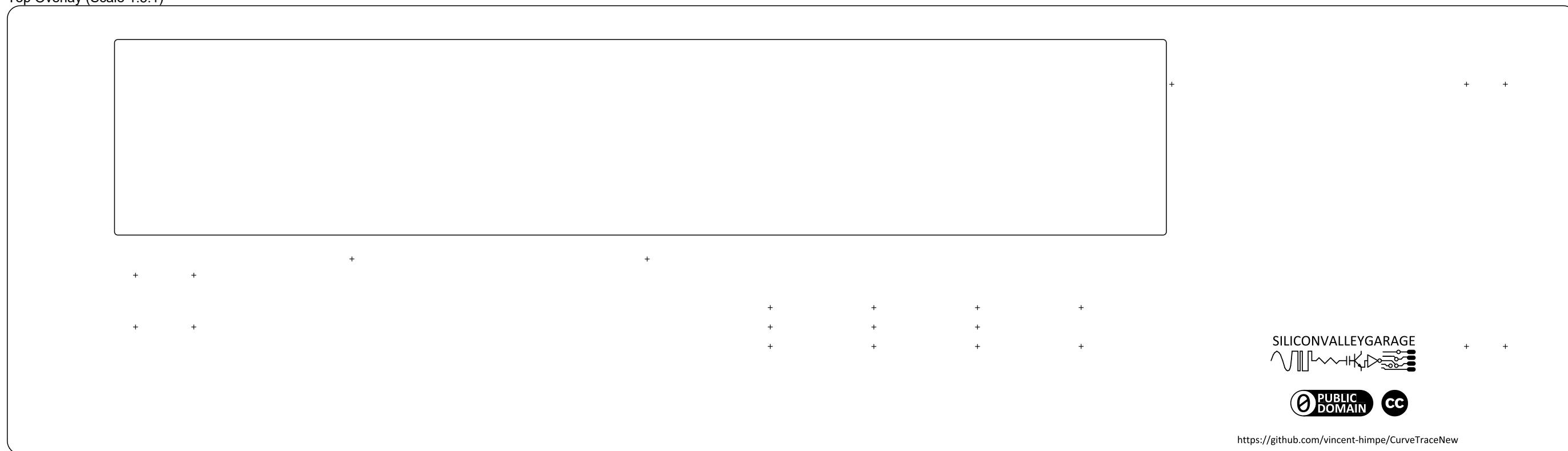
Project CT9042.PjPcb

Version: | Variant [No Variations]

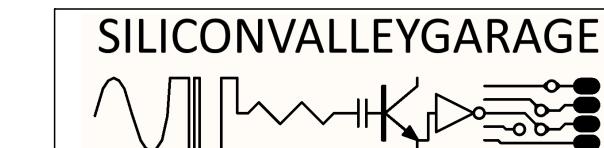
FABRICATION DRAWING

# LAYER VIEW : TOP SILKSCREEN (LEGEND)

Top Overlay (Scale 1.5:1)



<https://github.com/vincent-himpe/CurveTraceNew>



Project CT9042.PrjPcb

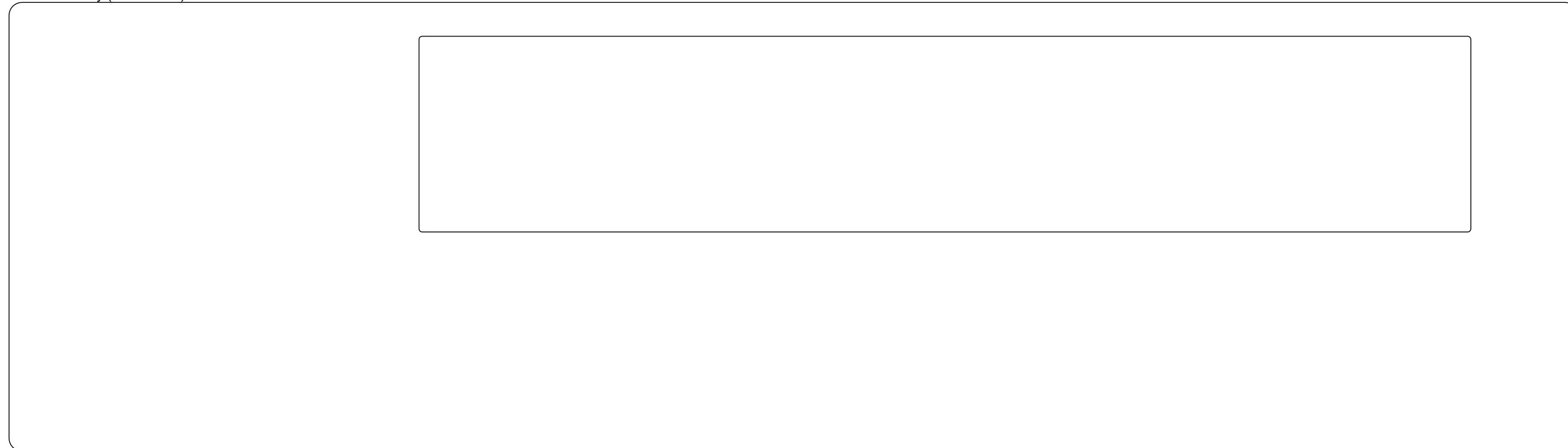
Version: | Variant [No Variations]

## FABRICATION DRAWING

# LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

A

Bottom Overlay (Scale 1.5:1)



A

B

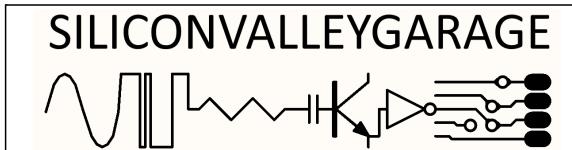
B

C

C

D

D

**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

# GENERAL



## A Unless otherwise specified the following rules apply:

1. DO NOT DEVIATE FROM ARTWORK OR BOM WITHOUT PRIOR AUTHORIZATION.
2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

## B Bill of Materials and Material Handling

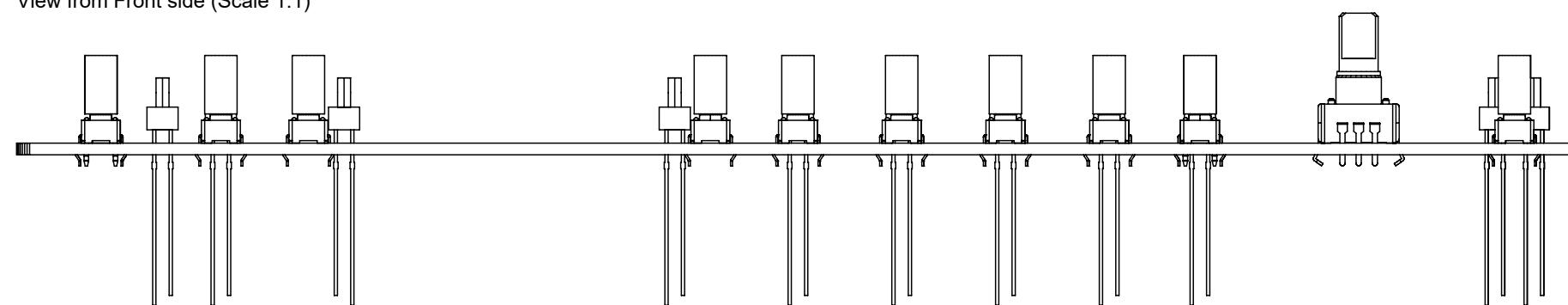
3. THE BOM CONTAINED IN THIS DOCUMENT IS AS-BUILT. NON-INSTALLED PARTS HAVE BEEN REMOVED. ADDITIONAL BOM FORMATS ARE AVAILABLE IN THE PROJECT FILES
4. ANY PART SUBSTITUTIONS MUST BE APPROVED IN WRITING BEFORE ASSEMBLY
5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
7. ESD CONTROL PER IPC RULES

## B Soldering

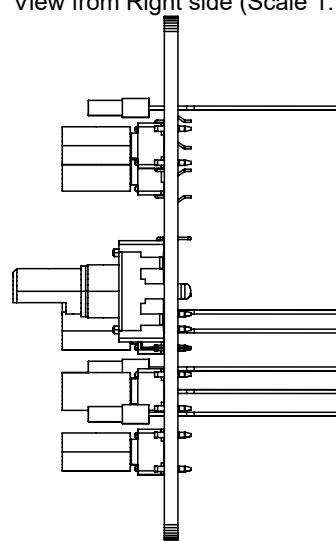
8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
10. SOLDERING PREFERABLY TO BE DONE USING NITROGEN ATMOSPHERE
11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

2D VIEW

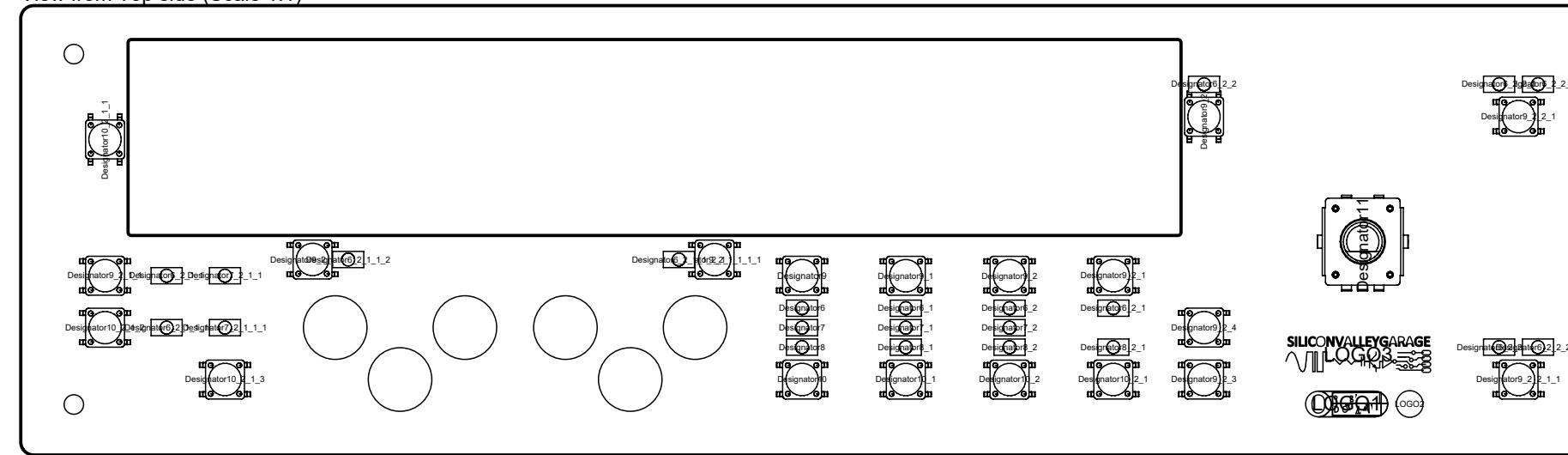
View from Front side (Scale 1:1)



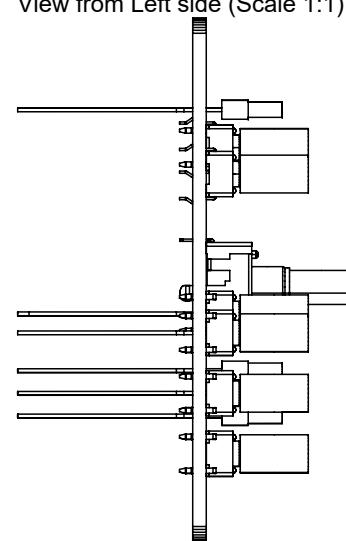
View from Right side (Scale 1:1)



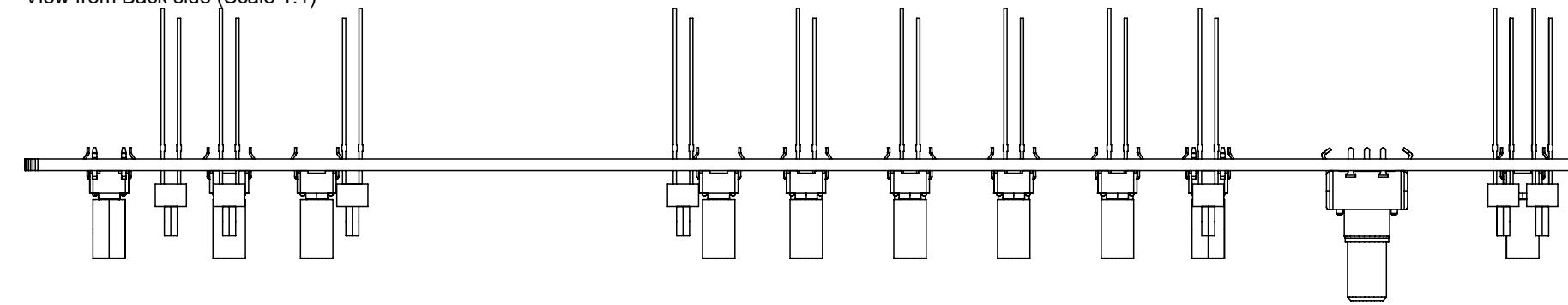
View from Top side (Scale 1:1)



View from Left side (Scale 1:1)



View from Back side (Scale 1:1)



SILICONVALLEYGARAGE

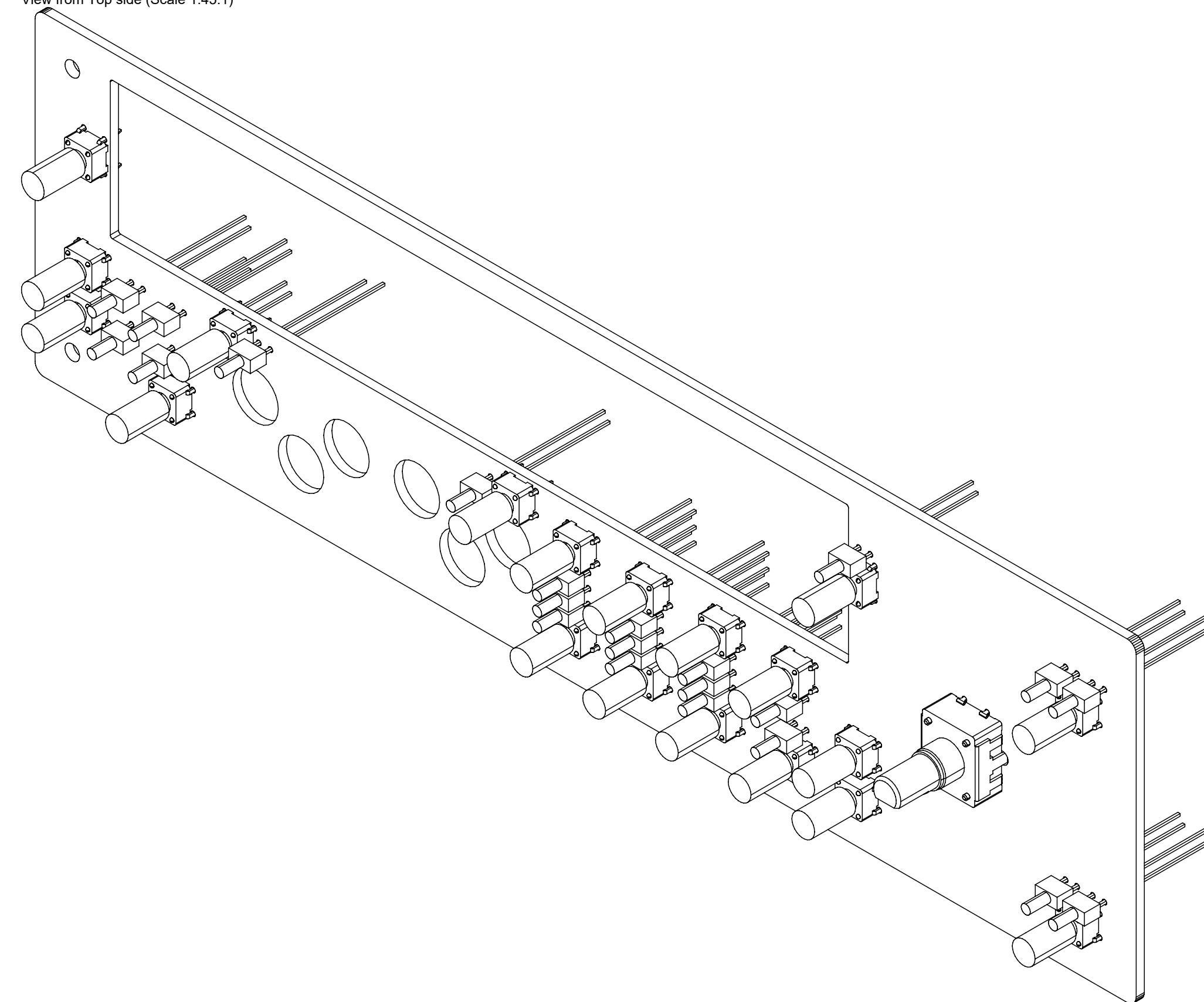
Project CT9042.PrjPcb

Version: | Variant [No Variations]

## **ASSEMBLY DRAWING**

## 3D VIEW

View from Top side (Scale 1.45:1)



# Bill Of Materials

A

Quantity	Designator	Description	LCSC	MOUSER
1	*1			
27	C1, C4, C6, C8, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C22, C24, C25, C29, C30, C31, C32, C36, C37, C220, C221, C222	CAPACITOR,CERAMIC,100nF,50V,X7R,0603	C127833	80-C0603C104K5R
5	C2, C3, C5, C7, C9	CAPACITOR,CERAMIC,10uF,25V,X5R,0805	C3039694	187-CL21B106KAYQNNE
3	C21, C33, C219	CAPACITOR,CERAMIC,10nF,50V,X7R,0603		
6	C23, C34, C214, C217, C224, C225	CAPACITOR,CERAMIC,100pF,50V,C0G,0603		
3	C26, C28, C67	CAPACITOR,ALU,47uF,100V,TH,P5mm,D10mm,H14mm		
2	C27, C234	CAPACITOR,CERAMIC,10pF,50V,C0G,0603		80-C0603C100J5GAC
1	C35	CAPACITOR,CERAMIC,1nF,50V,C0G,0603		
6	C38, C43, C47, C51, C55, C59	CAPACITOR,ALU,2200uF,35V,TH,P7.5mm,D16mm,H27mm		
7	C39, C40, C44, C48, C52, C56, C60	CAPACITOR,ALU,47uF,35V,TH,P0.25mm,D6.3mm,H12.5mm		
14	C41, C42, C45, C46, C49, C50, C53, C54, C57, C58, C61, C62, C63, C64	CAPACITOR,CERAMIC,100nF,100V,X7R,0805		
1	C65	CAPACITOR,ALU,2200uF,100V,TH,P10mm,D35mm,H32mm,SNAP		
1	C66	CAPACITOR,ALU,4u7,100V,TH,P0.25mm,D50mm,H12mm		
1	C223	CAPACITOR,CERAMIC,120pF,50V,C0G,0603		
21	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21	LED,TH,GREEN,42mCd,3MM		78-VLMPG33N1P2
6	D22, D23, D28, D29, D30, D38	DIODE,75V,250mA,SOT23,500pA ULTRA LOW LEAKAGE		
8	D24, D25, D26, D27, D39, D43, D44, D45	DIODE,RECTIFIER,75V,0.3A,MMBD4148,SOT23		
16	D31, D32, D33, D36, D37, D217, D220, D221, D222, D223, D224, D225, D226, D227, D228, D229	DIODE,RECTIFIER,75V,0.3A,BAS16,SOT23		
19	D34, D35, D47, D50, D56, D57, D58, D60, D63, D65, D66, D67, D68, D70, D73, D75, D77, D215, D231	DIODE,RECTIFIER,1000V,1A,ONSEMI,NRVA4007,SMA		
3	D40, D41, D42	LED,GREEN,TH,3MM		
17	D46, D48, D49, D51, D52, D53, D54, D55, D59, D61, D62, D64, D69, D71, D72, D74, D?	DIODE,RECTIFIER,600V,2A,S2J,DO214AA(SMB)		637-SK115
1	D76	DIODE,ZENER,33V,1W,Z1SMA33,DO214AC(SMA)		
1	D78	DIODE,ZENER,24V,1W,Z1SMA24,DO214AC(SMA)		
1	DISP1	DISPLAY,LCD,ALPHA,2X40CHAR,HD44780,YELLOW BL		
7	HS1, HS2, HS3, HS4, HS5, HS6, HS7	HEATSINKSTAMPED,CLIP-ON,BOARDMOUNT,3W,25C/W,CUI,HSS06-C20-P32		
1	HS8	HEATSINK,CLIP FOR HSS01-B20-CP		
1	HS9	HEATSINKSTAMPED,CLIP-ON,BOARDMOUNT,3W,25C/W,CUI,HSS01-B20-CP		
2	J1, J2			
2	J3, J6			
2	J4, J7	CONNECTOR,BANANA,BLUE,CHASSIS,CLIFF		
2	J5, J8			
1	J9	CONN,POWER,IEC,SWITCH,FUSE ASSEMBLY,PANELMOUNT		
5	K1, K2, K3, K4, K5			
2	K6, K9	RELAY,OPTOMOS,6A,60V,AC,IXYS,CPC1907B,SMD		
2	K7, K10	RELAY,DPDT,1A,250VAC,220VDC,5V COIL,KEMET,UA2-5NJ		
2	K8, K11	RELAY,OPTOMOS,1.5A,100V,AC,IXYS,LCA701S,SMD		
1	K12	RELAY,DPDT,5V COIL,250VAC,3A		
18	Q1, Q2, Q4, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q18, Q211, Q212, Q213, Q216, Q218	XSTR,NPN,45V,0.1A,,BC847B,SOT23		
6	Q3, Q5, Q17, Q201, Q214, Q215	XSTR,PNP,SOT23,BC857,SOT23		
1	Q15	XSTR,NMOS,100V,12A,DMN10H170SK3-13,DPAK		
1	Q16	XSTR,PMOS,100V,5.6A,DMP10H400SK3-13,DPAK		
1	Q217	XSTR,JFET,NCHAN,ONSEMI,MMBFJ112,SOT23		

A

A

B

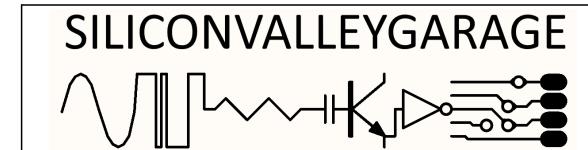
B

C

C

D

D



Project CT9042.PjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6

# DESIGNATORS FRONT

A

A

B

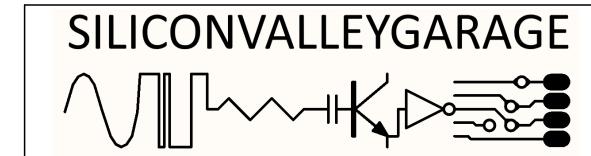
B

C

C

D

D

**SILICONVALLEYGARAGE****Project CT9042.PrjPcb**

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6

1

2

3

4

5

6

# DESIGNATORS BACK

A

A

B

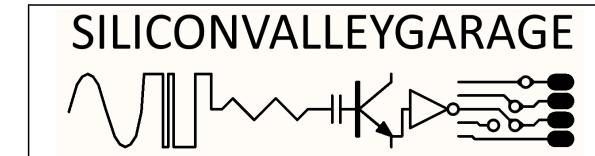
B

C

C

D

D

**SILICONVALLEYGARAGE****Project CT9042.PrjPcb**

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6

1

2

3

4

5

6

# PASTE MASK TOP

A

A

B

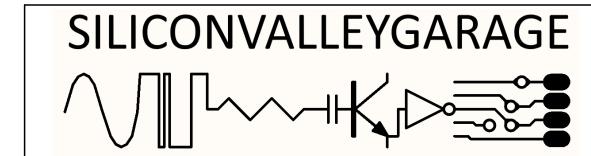
B

C

C

D

D



**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

4

5

6

1

2

3

4

5

6

# PASTE MASK BACK

A

A

B

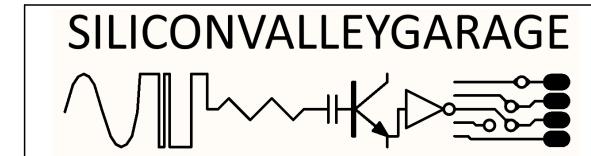
B

C

C

D

D



**Project CT9042.PrjPcb**  
Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

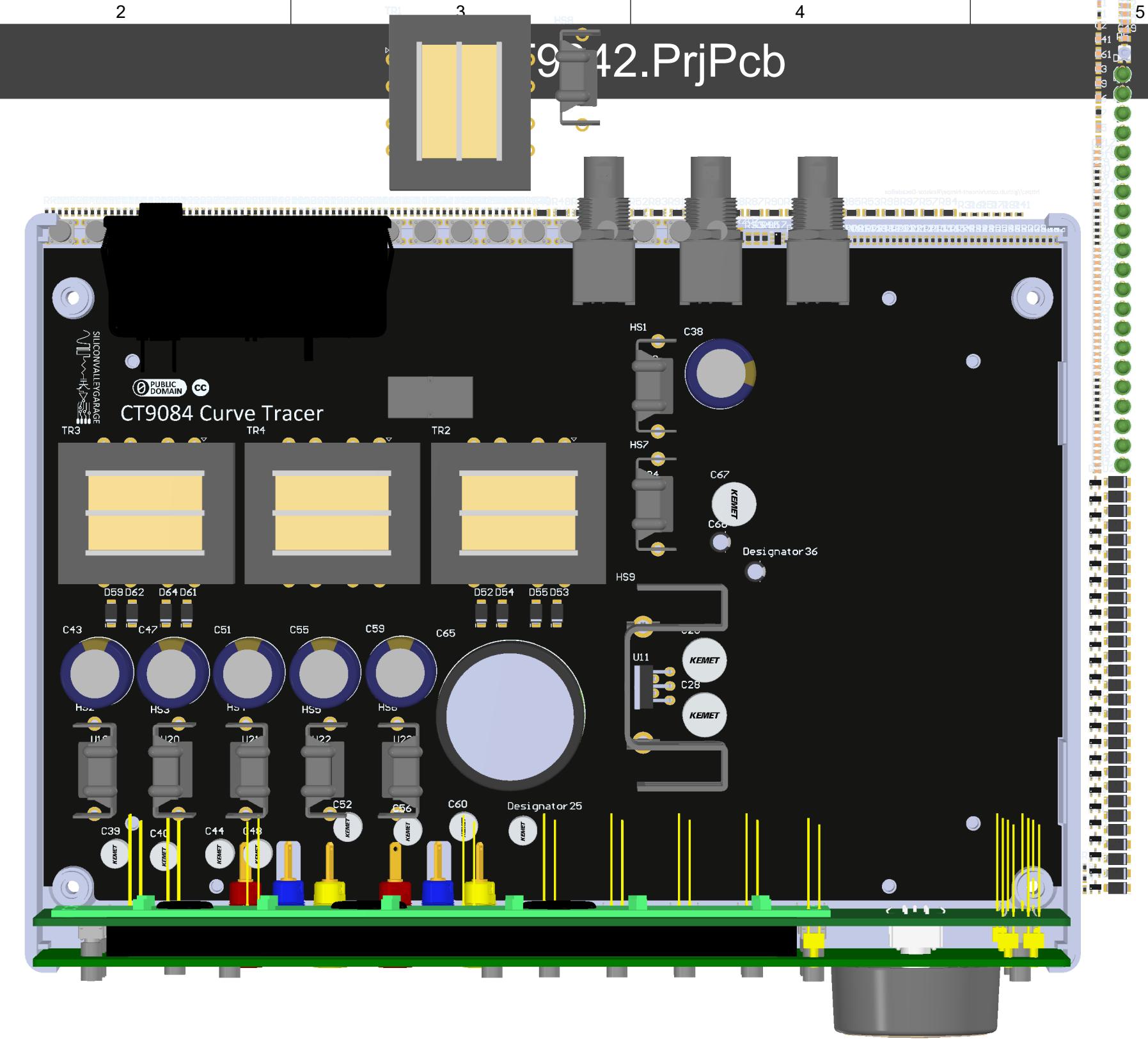
4

5

6

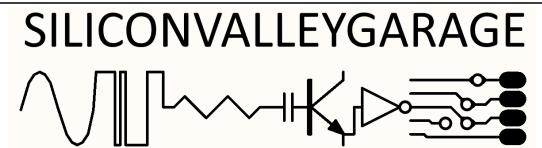
1 2 3 4 5 6

942.PrjPcb



Document Creation Date: 8/28/2025

Design : free\_electron



1 2 3 4 5 6

# GENERAL

## GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.
3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER
4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2
5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

## MATERIALS

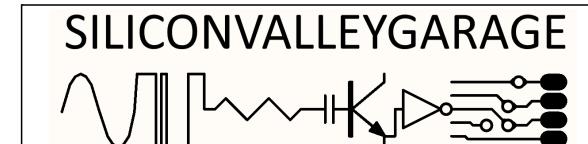
7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

## STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

## QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY



Project CT9042.PrjPcb

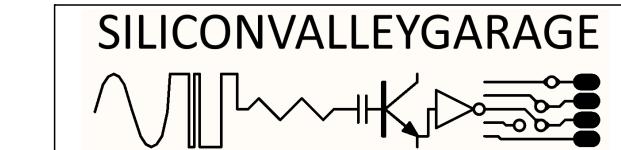
Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER STACK

## Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material Type	Gerber Dk	Weight	Constructions	Df	Resin
A	Top Overlay			Legend	GTO				
B	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5		
C	<b>Copper</b>	<b>Top Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal</b>	<b>GTL</b>	<b>1oz</b>		
D	Prepreg		0.102mm(4.000mil)	Core-009	Dielectric		4.5	1-2116	0.02 47%
	CF-004	Layer 1	0.035mm(1.378mil)		Signal	G1	1oz		
			1.450mm(57.087mil)	FR-4	Dielectric		4.8		
	CF-004	Layer 2	0.035mm(1.378mil)		Signal	G2	1oz		
	Prepreg		0.102mm(4.000mil)	Core-009	Dielectric		4.5	1-2116	0.02 47%
	<b>Copper</b>	<b>Bottom Layer</b>	<b>0.036mm(1.400mil)</b>		<b>Signal</b>	<b>GBL</b>	<b>1oz</b>		
	Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5		
	Bottom Overlay			Legend	GBO				
	Total thickness: 1.815mm(71.443mil)								



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# CONTROLLED IMPEDANCE

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Substack	Clearance	Target Tolerance
1	Coated Microstrip	50	50.02	Top Layer	6.370mil(6.370mil)	6.370mil(6.370mil)	Layer 1	Board Layer Stack	5.000mil(5.000mil)	10%
2	Offset stripline	50	50.01	Layer 1	4.239mil(4.239mil)	4.239mil(4.239mil)	Top Layer,Layer 2	Board Layer Stack	5.000mil(5.000mil)	10%
3	Offset stripline	50	50.01	Layer 2	4.239mil(4.239mil)	4.239mil(4.239mil)	Layer 1,Bottom Layer	Board Layer Stack	5.000mil(5.000mil)	10%
4	Coated Microstrip	50	50.02	Bottom Layer	6.370mil(6.370mil)	6.370mil(6.370mil)	Layer 2	Board Layer Stack	5.000mil(5.000mil)	10%

A

A

B

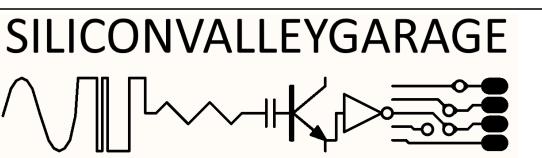
B

C

C

D

D



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
☒	20	0.800mm(31.496mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
☆	18	1.000mm(39.370mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
☒	118	1.000mm(39.370mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✚	5	1.200mm(47.244mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
▽	53	1.600mm(62.992mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
□	16	2.000mm(78.740mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
❖	2	2.100mm(82.677mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
○	2	3.200mm(125.984mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
◇	8	3.500mm(137.795mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✳	2	10.000mm(393.701mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
244 Total											

A

A

B

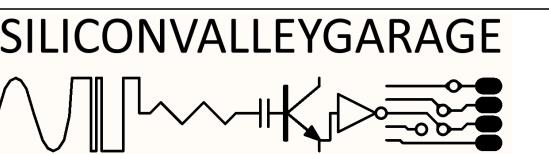
B

C

C

D

D



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

25

26

27

28

29

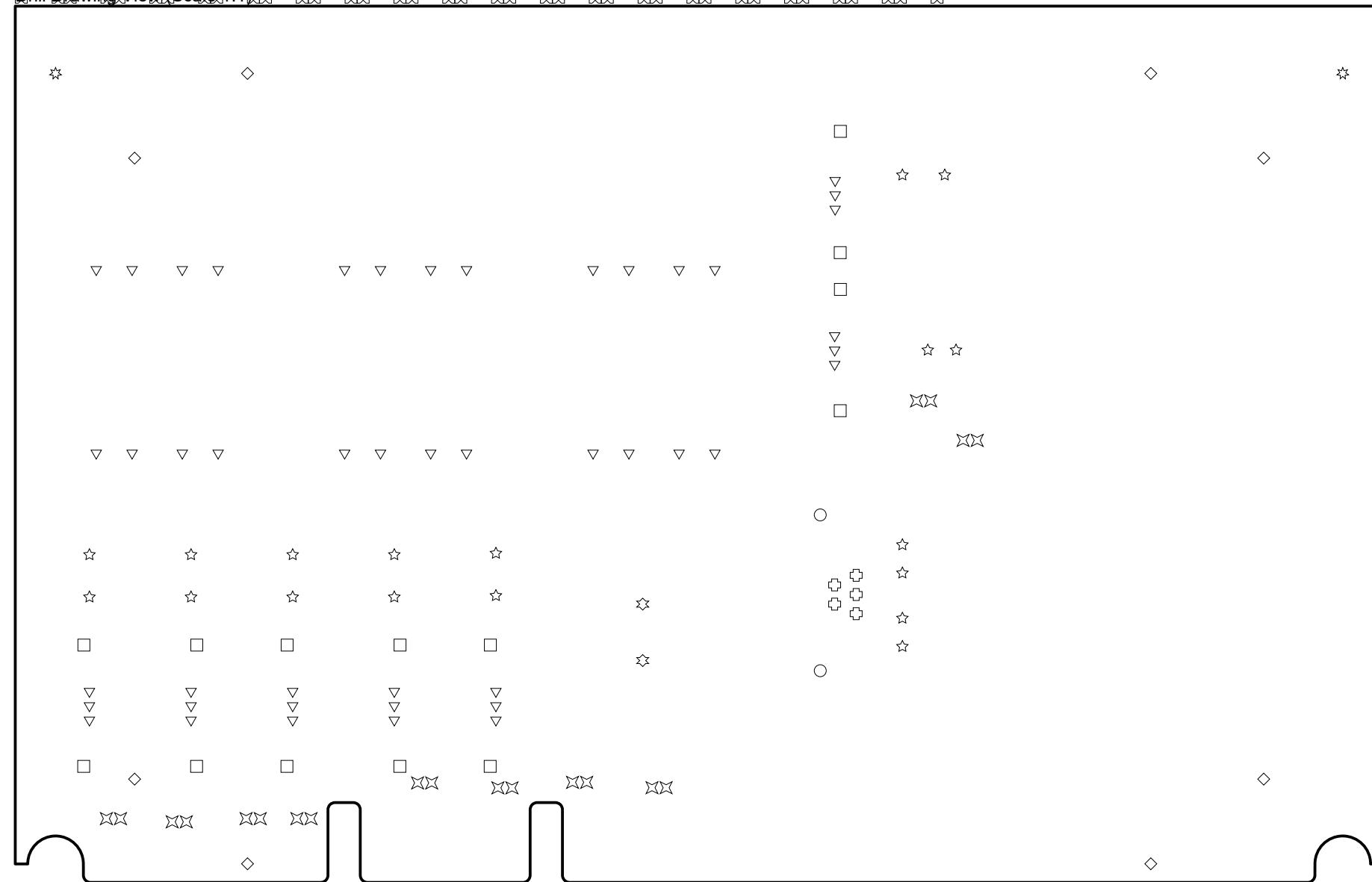
30

# DRILL DRAWING

A

A

XX  
Drill Drawing View (Scale 1:1) XX XX



B

B

C

C

D

D

SILICONVALLEYGARAGE



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

25

26

27

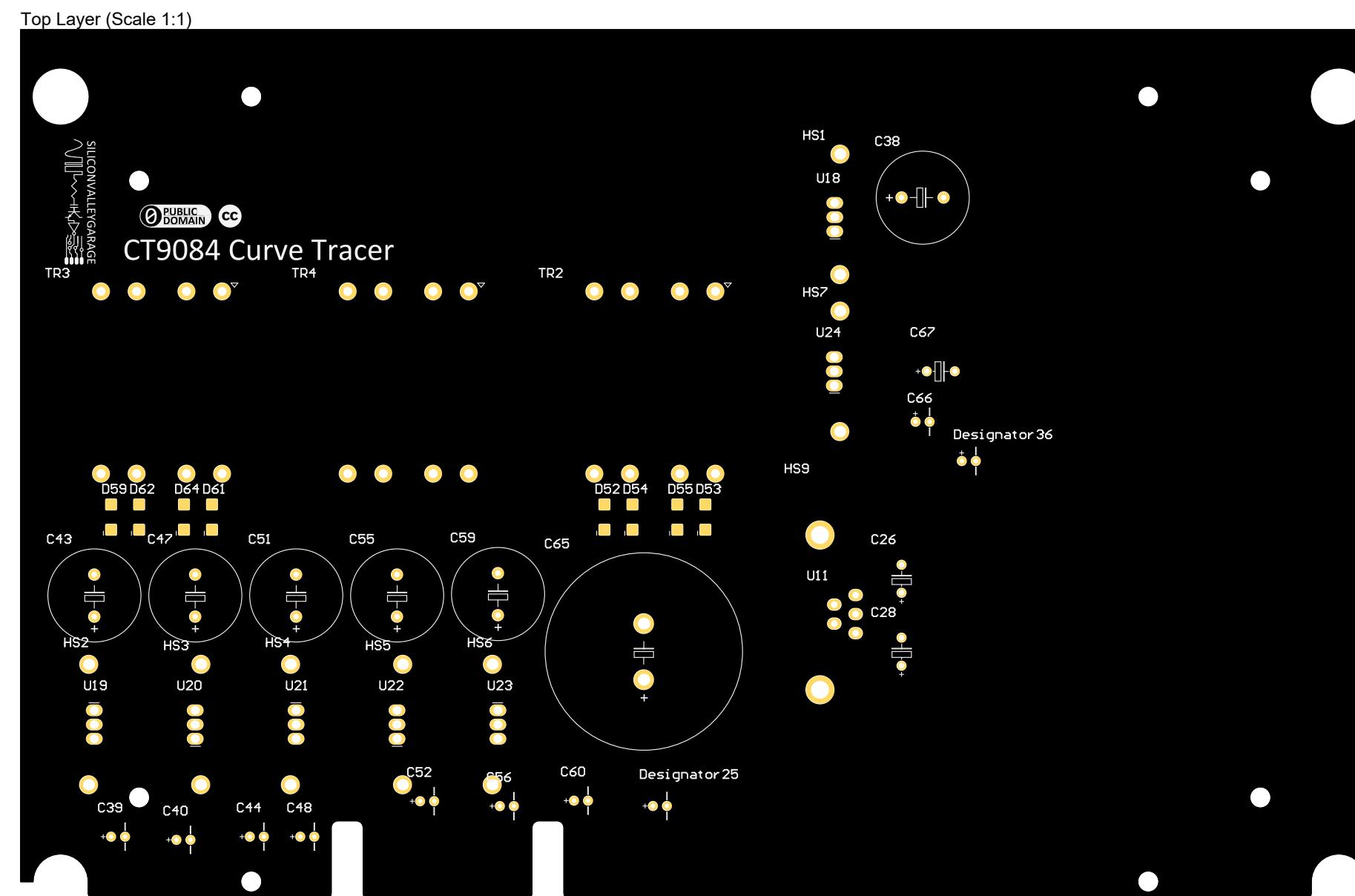
28

29

30

# COMPOSITE VIEW FRONT

A A  
B B  
C C  
D D

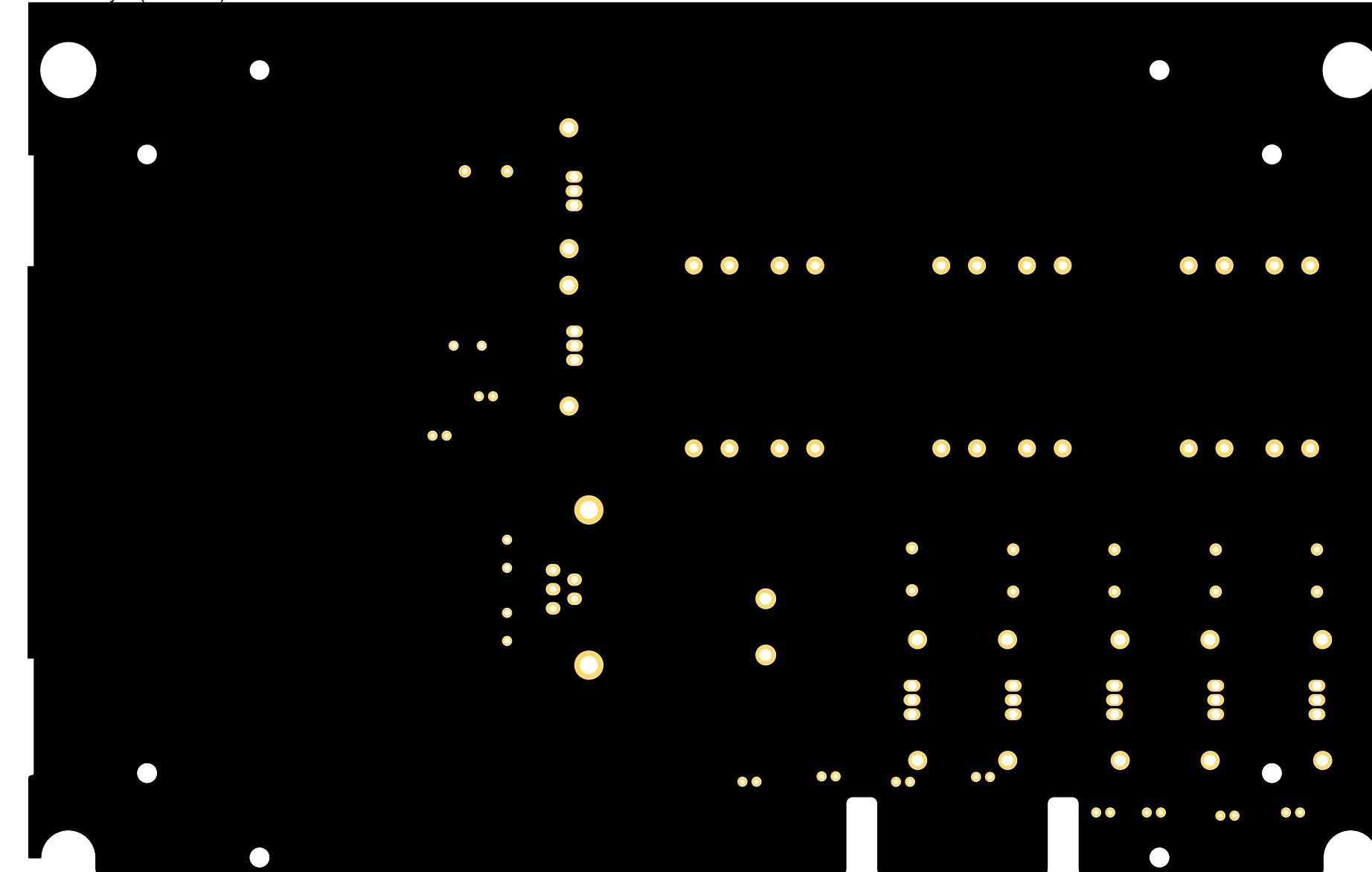


## COMPOSITE VIEW BACK

A

A

Bottom Layer (Scale 1:1)



B

B

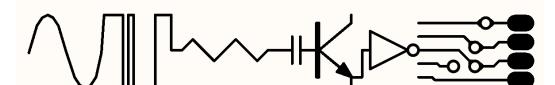
C

C

D

D

SILICONVALLEYGARAGE



Project CT9042.PjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER VIEW : TOP LAYER

A

A

B

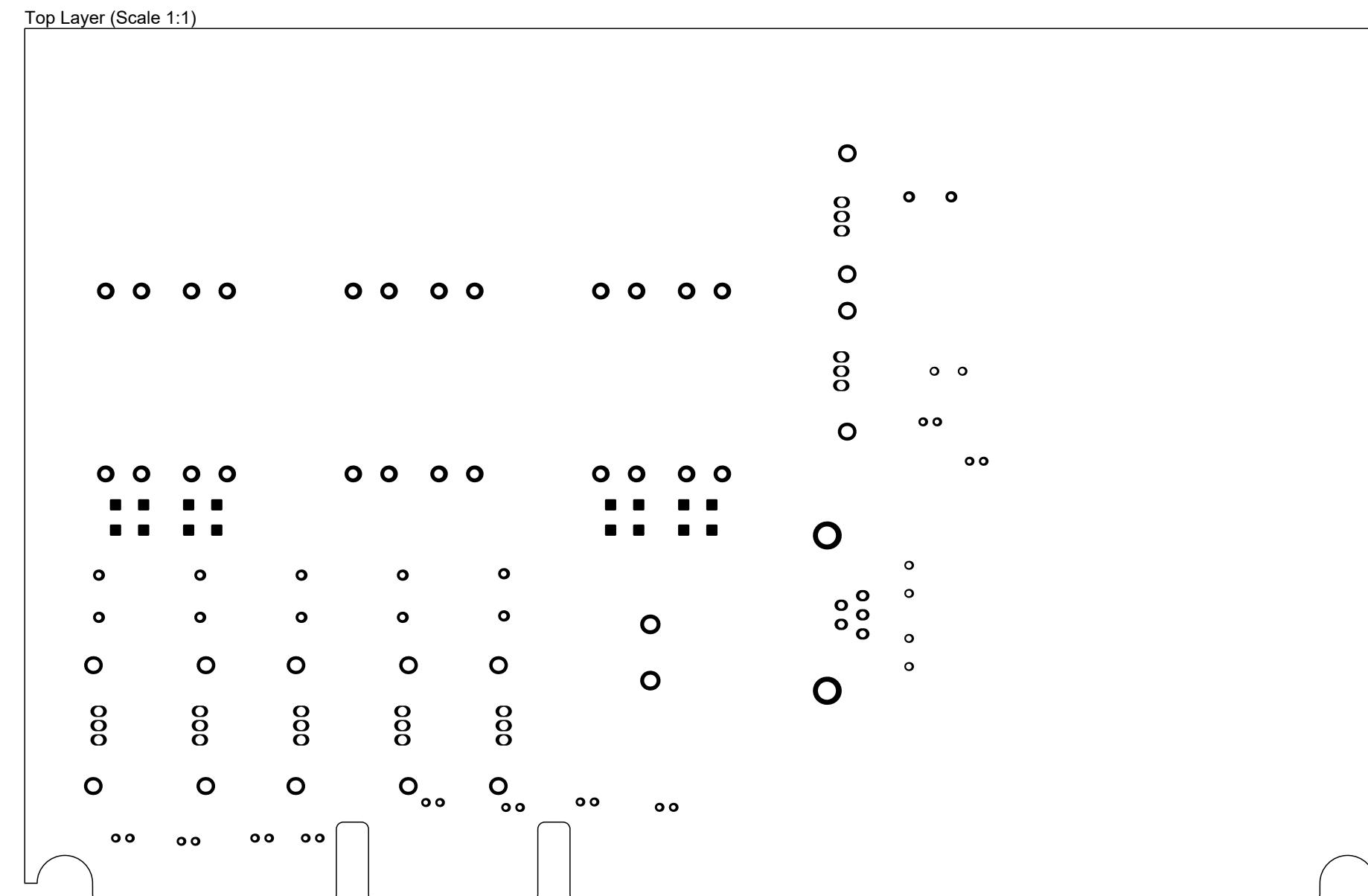
B

C

C

D

D



## LAYER VIEW : MID LAYER 1

A

A

B

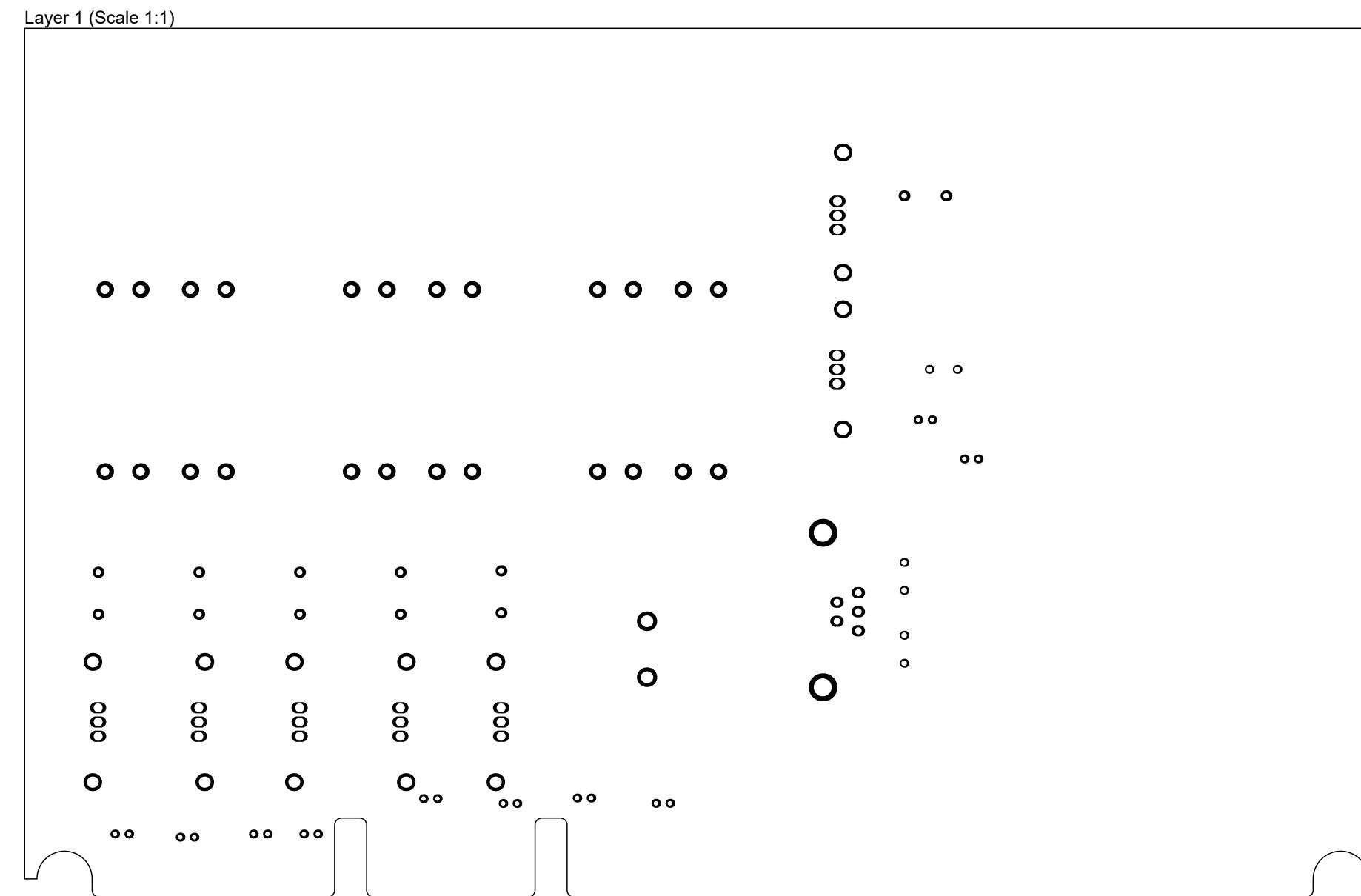
B

C

C

D

D



## LAYER VIEW : MID LAYER 2

A

A

B

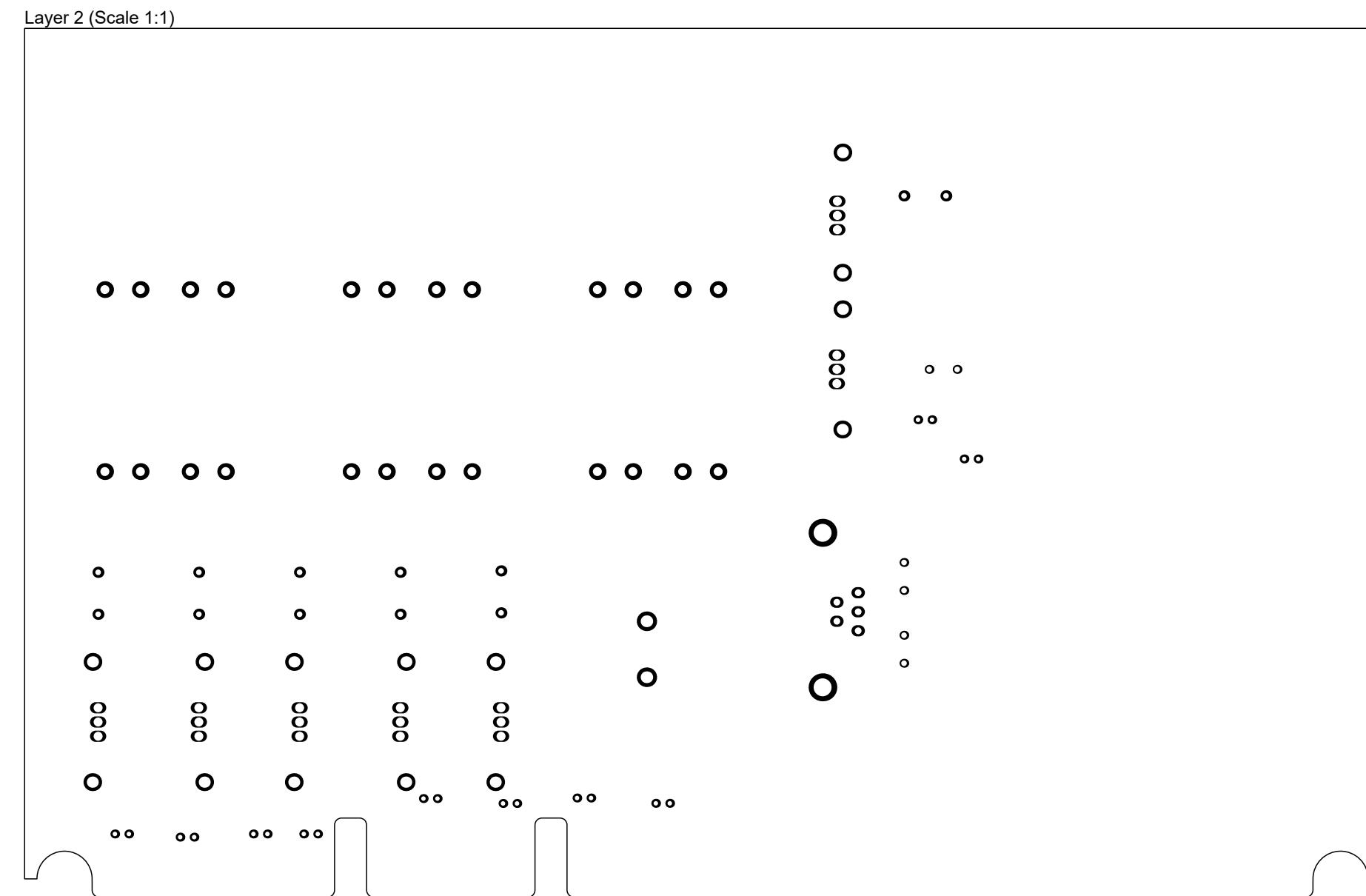
B

C

C

D

D



## LAYER VIEW : BOTTOM LAYER

A

A

B

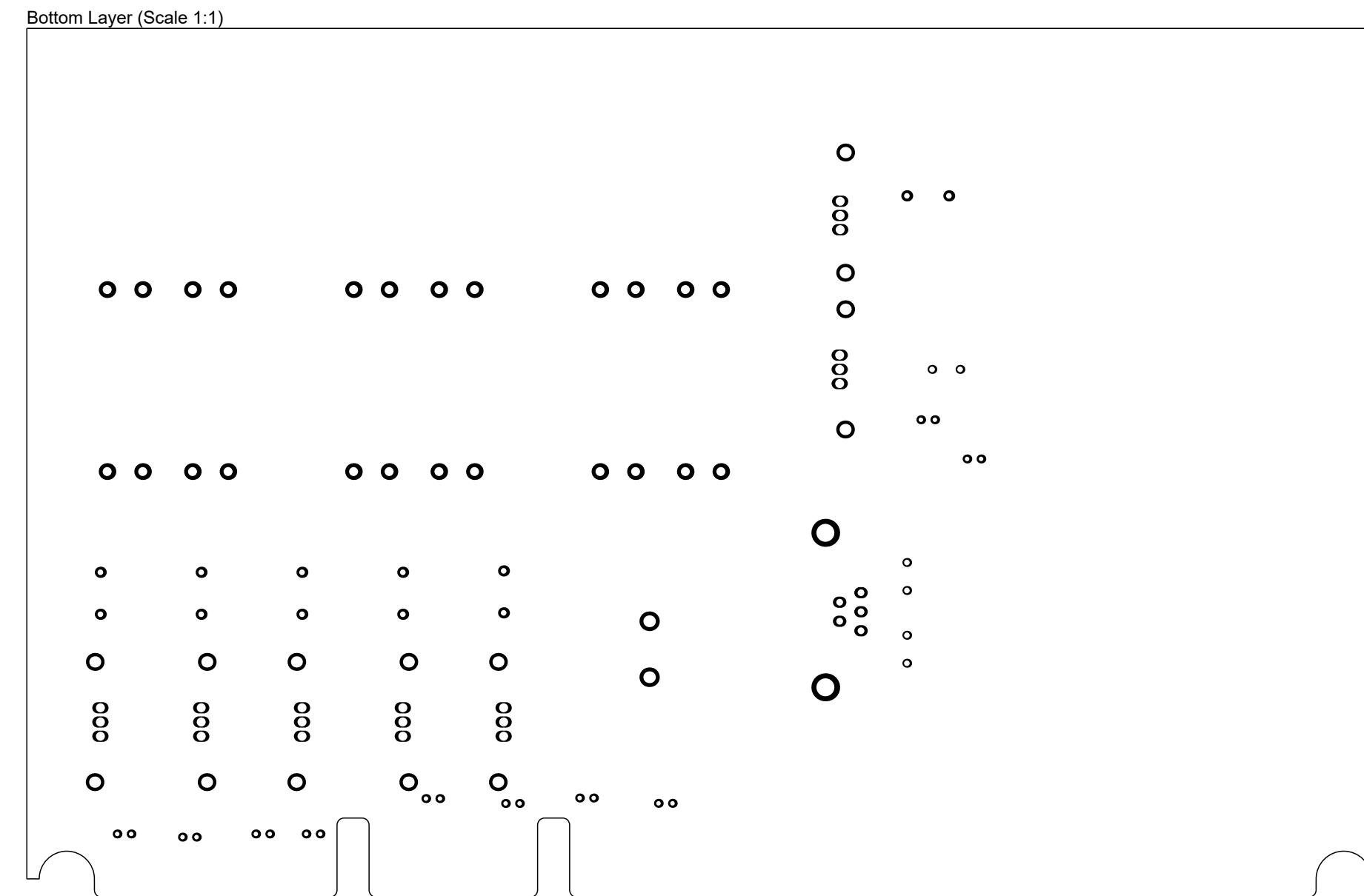
B

C

C

D

D



67

68

69

70

71

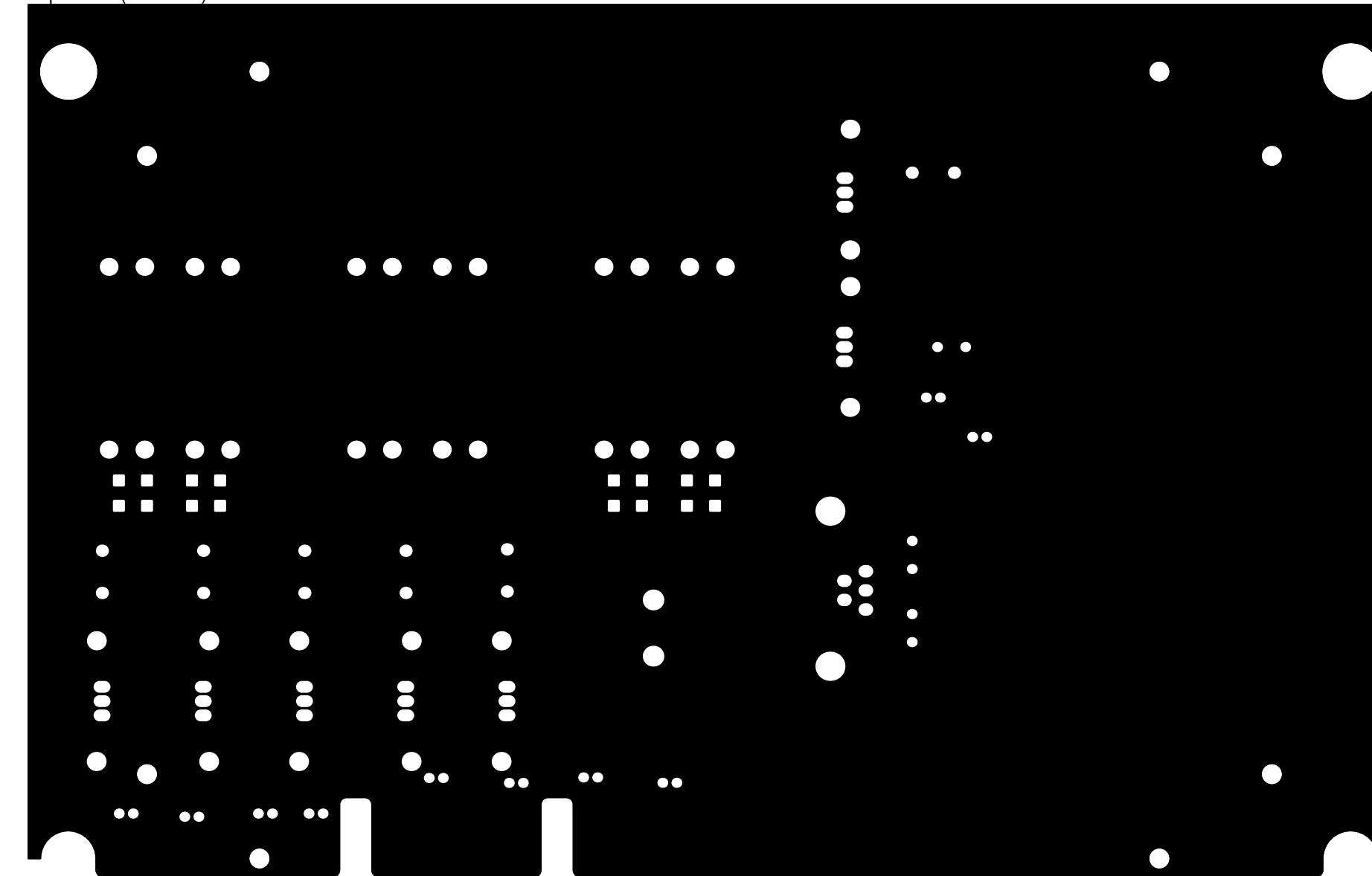
72

# LAYER VIEW : TOP SOLDER MASK

A

A

Top Solder (Scale 1:1)



B

B

C

C

D

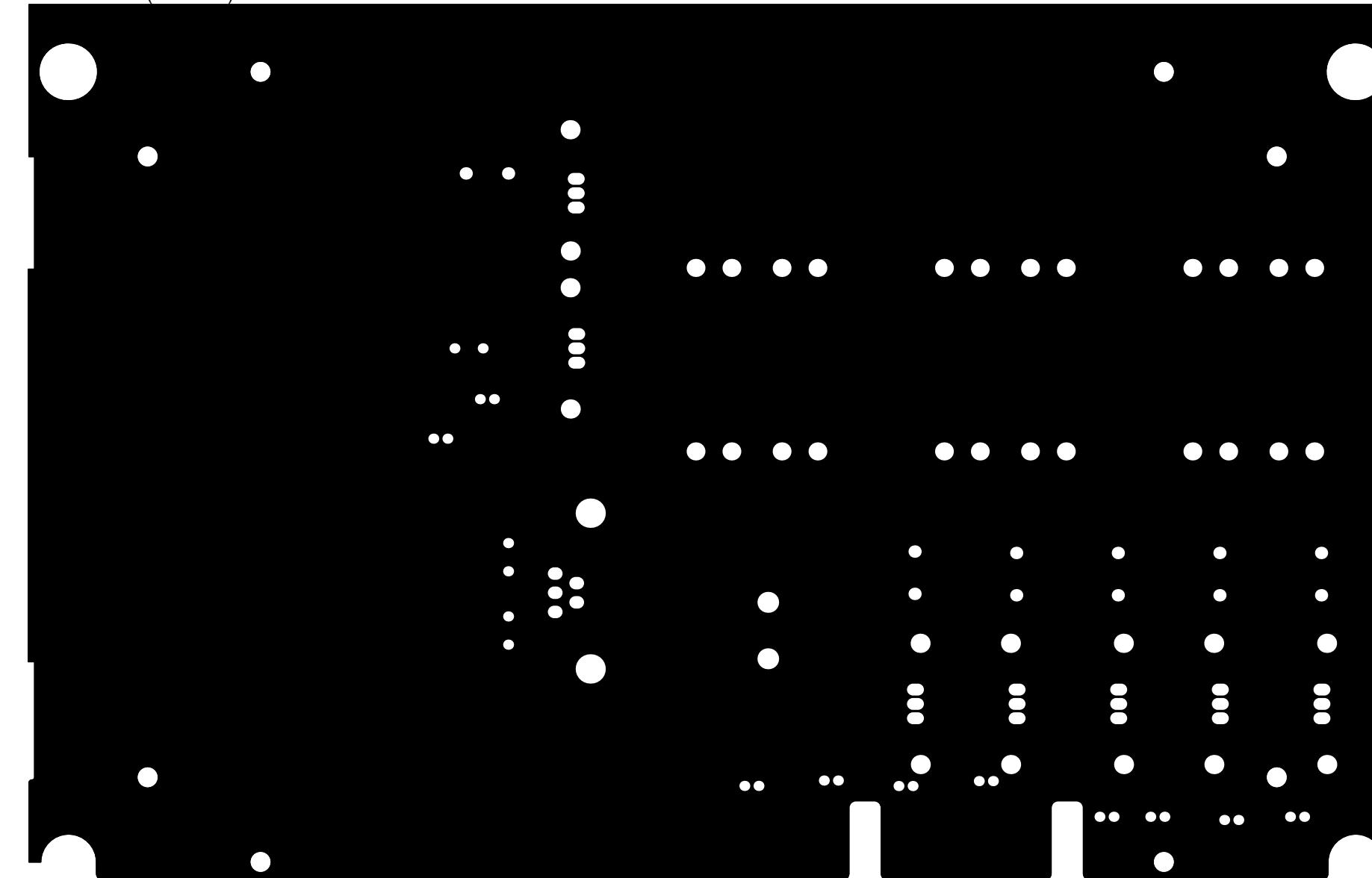
D

## LAYER VIEW : BOTTOM SOLDER MASK

A

A

Bottom Solder (Scale 1:1)



B

B

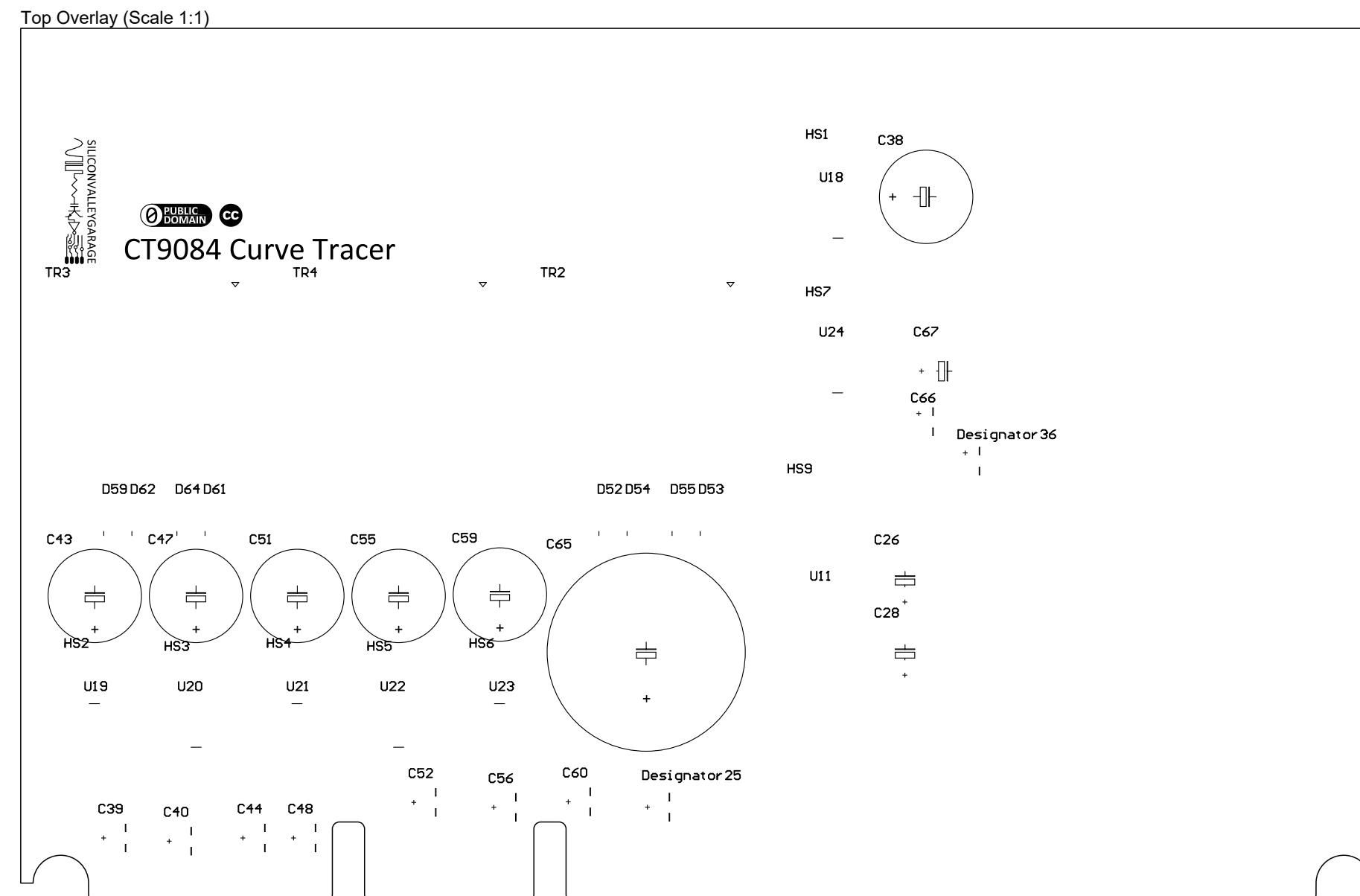
C

C

D

D

# LAYER VIEW : TOP SILKSCREEN (LEGEND)



# LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

A

A

B

B

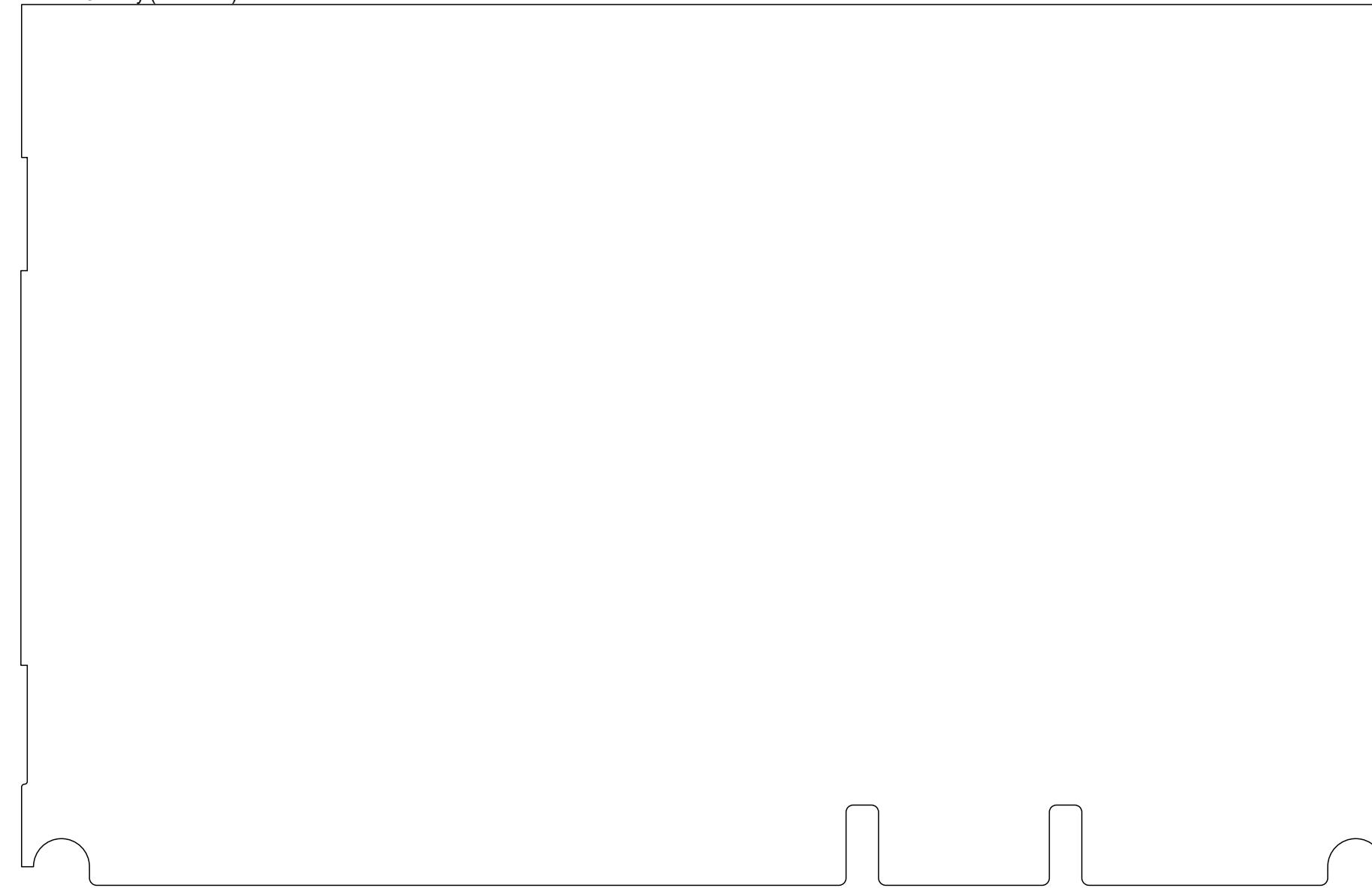
C

C

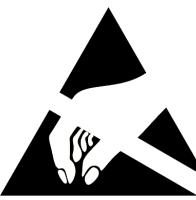
D

D

Bottom Overlay (Scale 1:1)



# GENERAL



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## B Bill of Materials and Material Handling

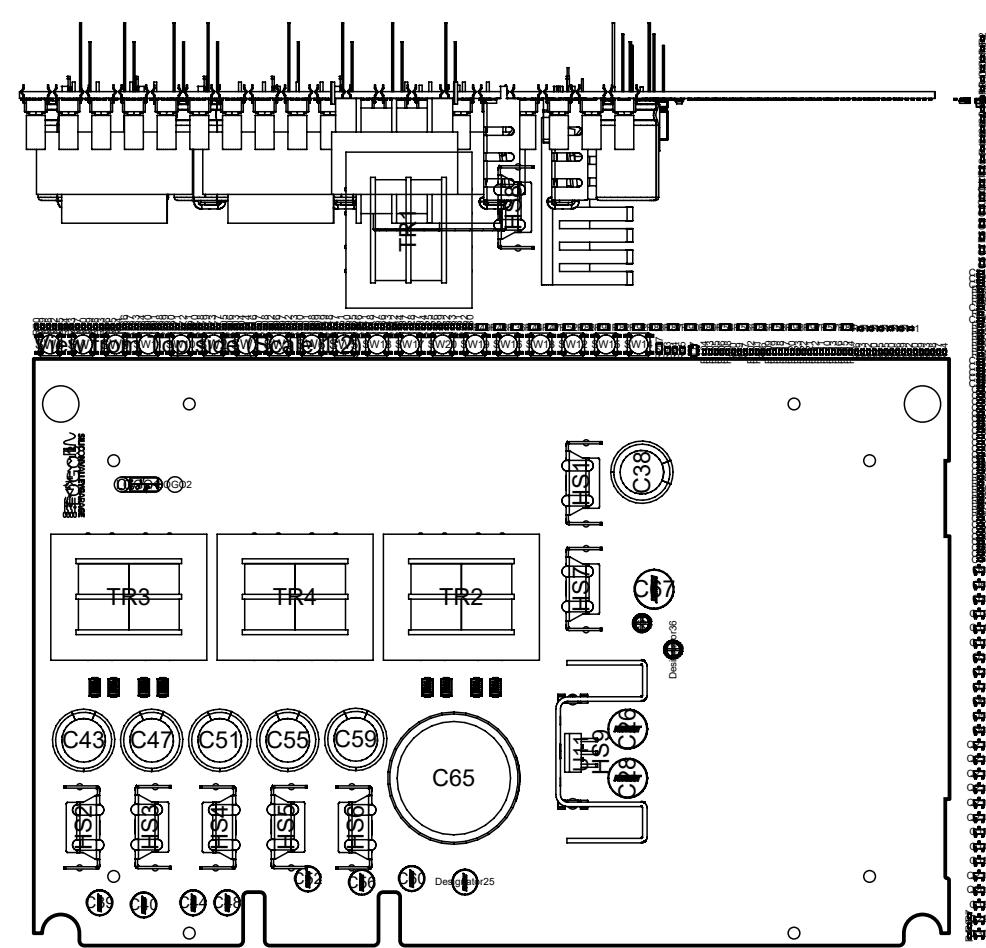
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5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
7. ESD CONTROL PER IPC RULES

## B Soldering

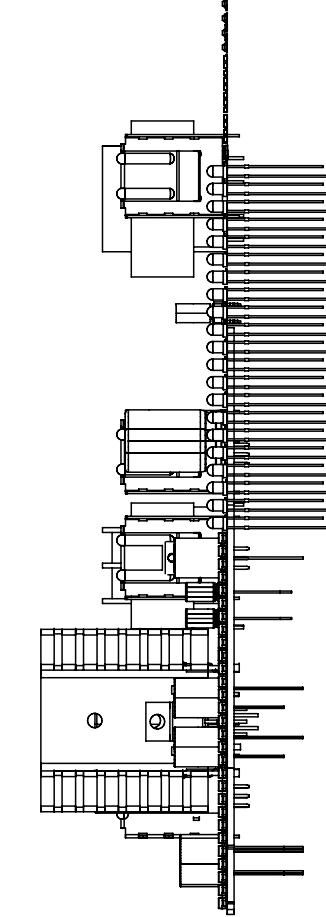
8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
10. SOLDERING PREFERABLY TO BE DONE USING NITROGEN ATMOSPHERE
11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

# 2D VIEW

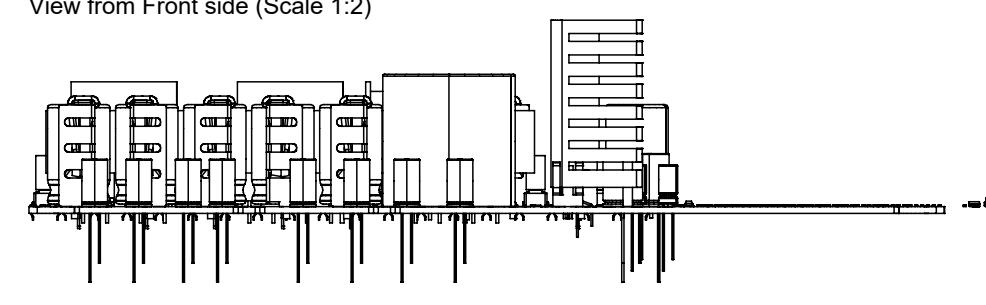
View from Back side (Scale 1:2)



View from Right side (Scale 1:2)



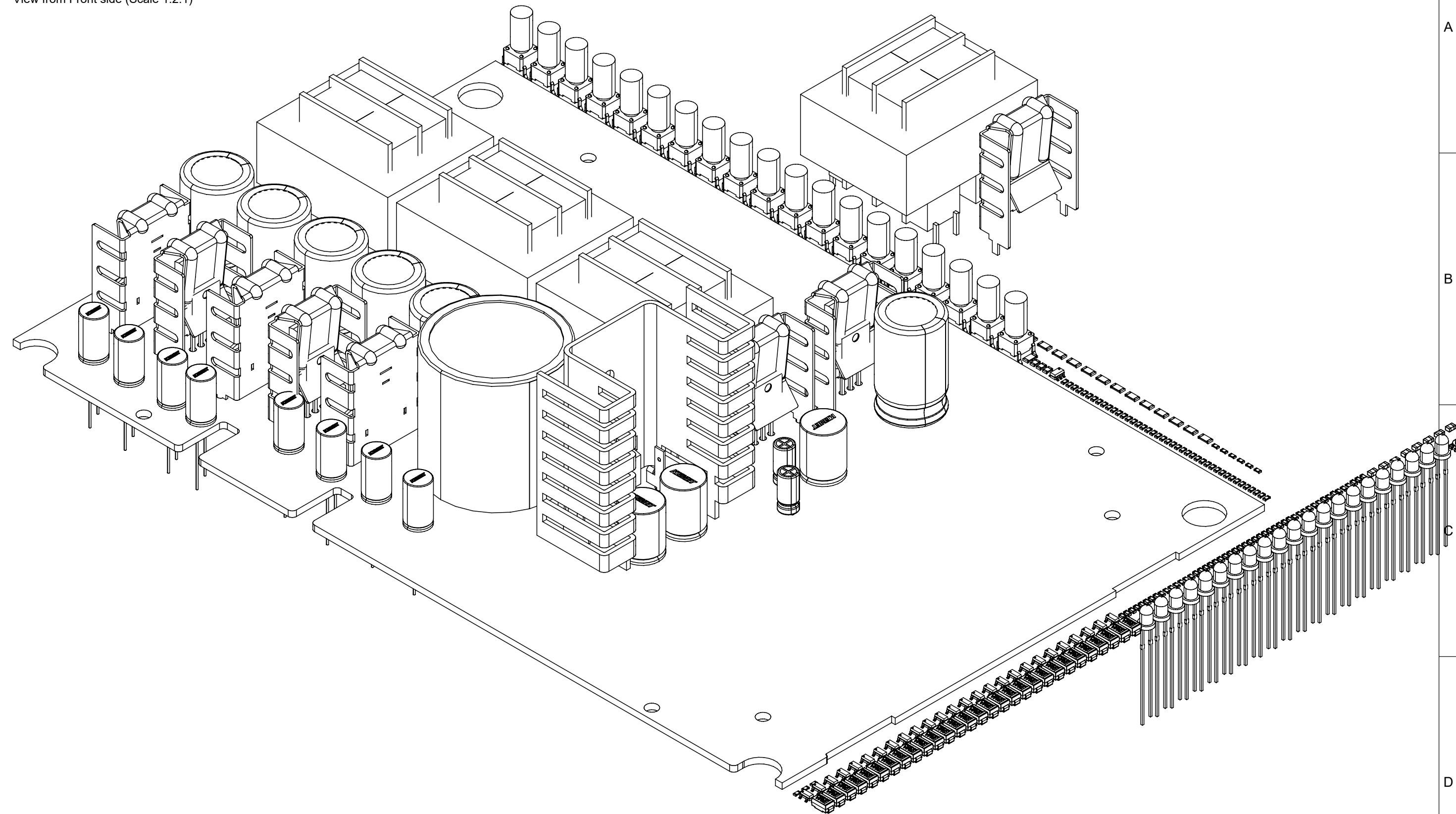
View from Front side (Scale 1:2)



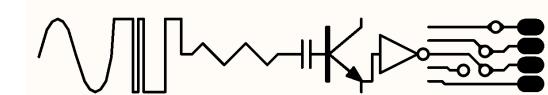
1 2 3 4 5 6

# 3D VIEW

View from Front side (Scale 1.2:1)



SILICONVALLEYGARAGE



Project CT9042.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1 2 3 4 5 6

# Bill Of Materials

A

Quantity	Designator	Description	LCSC	MOUSER
1	*1			
27	C1, C4, C6, C8, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C22, C24, C25, C29, C30, C31, C32, C36, C37, C220, C221, C222	CAPACITOR,CERAMIC,100nF,50V,X7R,0603	C127833	80-C0603C104K5R
5	C2, C3, C5, C7, C9	CAPACITOR,CERAMIC,10uF,25V,X5R,0805	C3039694	187-CL21B106KAYQNNE
3	C21, C33, C219	CAPACITOR,CERAMIC,10nF,50V,X7R,0603		
6	C23, C34, C214, C217, C224, C225	CAPACITOR,CERAMIC,100pF,50V,C0G,0603		
3	C26, C28, C67	CAPACITOR,ALU,47uF,100V,TH,P5mm,D10mm,H14mm		
2	C27, C234	CAPACITOR,CERAMIC,10pF,50V,C0G,0603		80-C0603C100J5GAC
1	C35	CAPACITOR,CERAMIC,1nF,50V,C0G,0603		
6	C38, C43, C47, C51, C55, C59	CAPACITOR,ALU,2200uF,35V,TH,P7.5mm,D16mm,H27mm		
7	C39, C40, C44, C48, C52, C56, C60	CAPACITOR,ALU,47uF,35V,TH,P0.25mm,D6.3mm,H12.5mm		
14	C41, C42, C45, C46, C49, C50, C53, C54, C57, C58, C61, C62, C63, C64	CAPACITOR,CERAMIC,100nF,100V,X7R,0805		
1	C65	CAPACITOR,ALU,2200uF,100V,TH,P10mm,D35mm,H32mm,SNAP		
1	C66	CAPACITOR,ALU,4u7,100V,TH,P0.25mm,D50mm,H12mm		
1	C223	CAPACITOR,CERAMIC,120pF,50V,C0G,0603		
21	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21	LED,TH,GREEN,42mCd,3MM		78-VLMPG33N1P2
6	D22, D23, D28, D29, D30, D38	DIODE,75V,250mA,SOT23,500pA ULTRA LOW LEAKAGE		
8	D24, D25, D26, D27, D39, D43, D44, D45	DIODE,RECTIFIER,75V,0.3A,MMBD4148,SOT23		
16	D31, D32, D33, D36, D37, D217, D220, D221, D222, D223, D224, D225, D226, D227, D228, D229	DIODE,RECTIFIER,75V,0.3A,BAS16,SOT23		
19	D34, D35, D47, D50, D56, D57, D58, D60, D63, D65, D66, D67, D68, D70, D73, D75, D77, D215, D231	DIODE,RECTIFIER,1000V,1A,ONSEMI,NRVA4007,SMA		
3	D40, D41, D42	LED,GREEN,TH,3MM		
17	D46, D48, D49, D51, D52, D53, D54, D55, D59, D61, D62, D64, D69, D71, D72, D74, D?	DIODE,RECTIFIER,600V,2A,S2J,DO214AA(SMB)		637-SK115
1	D76	DIODE,ZENER,33V,1W,Z1SMA33,DO214AC(SMA)		
1	D78	DIODE,ZENER,24V,1W,Z1SMA24,DO214AC(SMA)		
1	DISP1	DISPLAY,LCD,ALPHA,2X40CHAR,HD44780,YELLOW BL		
7	HS1, HS2, HS3, HS4, HS5, HS6, HS7	HEATSINKSTAMPED,CLIP-ON,BOARDMOUNT,3W,25C/W,CUI,HSS06-C20-P32		
1	HS8	HEATSINK,CLIP FOR HSS01-B20-CP		
1	HS9	HEATSINKSTAMPED,CLIP-ON,BOARDMOUNT,3W,25C/W,CUI,HSS01-B20-CP		
2	J1, J2			
2	J3, J6			
2	J4, J7	CONNECTOR,BANANA,BLUE,CHASSIS,CLIFF		
2	J5, J8			
1	J9	CONN,POWER,IEC,SWITCH,FUSE ASSEMBLY,PANELMOUNT		
5	K1, K2, K3, K4, K5			
2	K6, K9	RELAY,OPTOMOS,6A,60V,AC,IXYS,CPC1907B,SMD		
2	K7, K10	RELAY,DPDT,1A,250VAC,220VDC,5V COIL,KEMET,UA2-5NJ		
2	K8, K11	RELAY,OPTOMOS,1.5A,100V,AC,IXYS,LCA701S,SMD		
1	K12	RELAY,DPDT,5V COIL,250VAC,3A		
18	Q1, Q2, Q4, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q18, Q211, Q212, Q213, Q216, Q218	XSTR,NPN,45V,0.1A,,BC847B,SOT23		
6	Q3, Q5, Q17, Q201, Q214, Q215	XSTR,PNP,SOT23,BC857,SOT23		
1	Q15	XSTR,NMOS,100V,12A,DMN10H170SK3-13,DPAK		
1	Q16	XSTR,PMOS,100V,5.6A,DMP10H400SK3-13,DPAK		
1	Q217	XSTR,JFET,NCHAN,ONSEMI,MMBFJ112,SOT23		

A

A

B

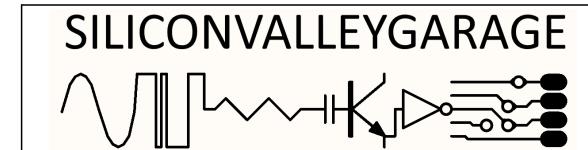
B

C

C

D

D



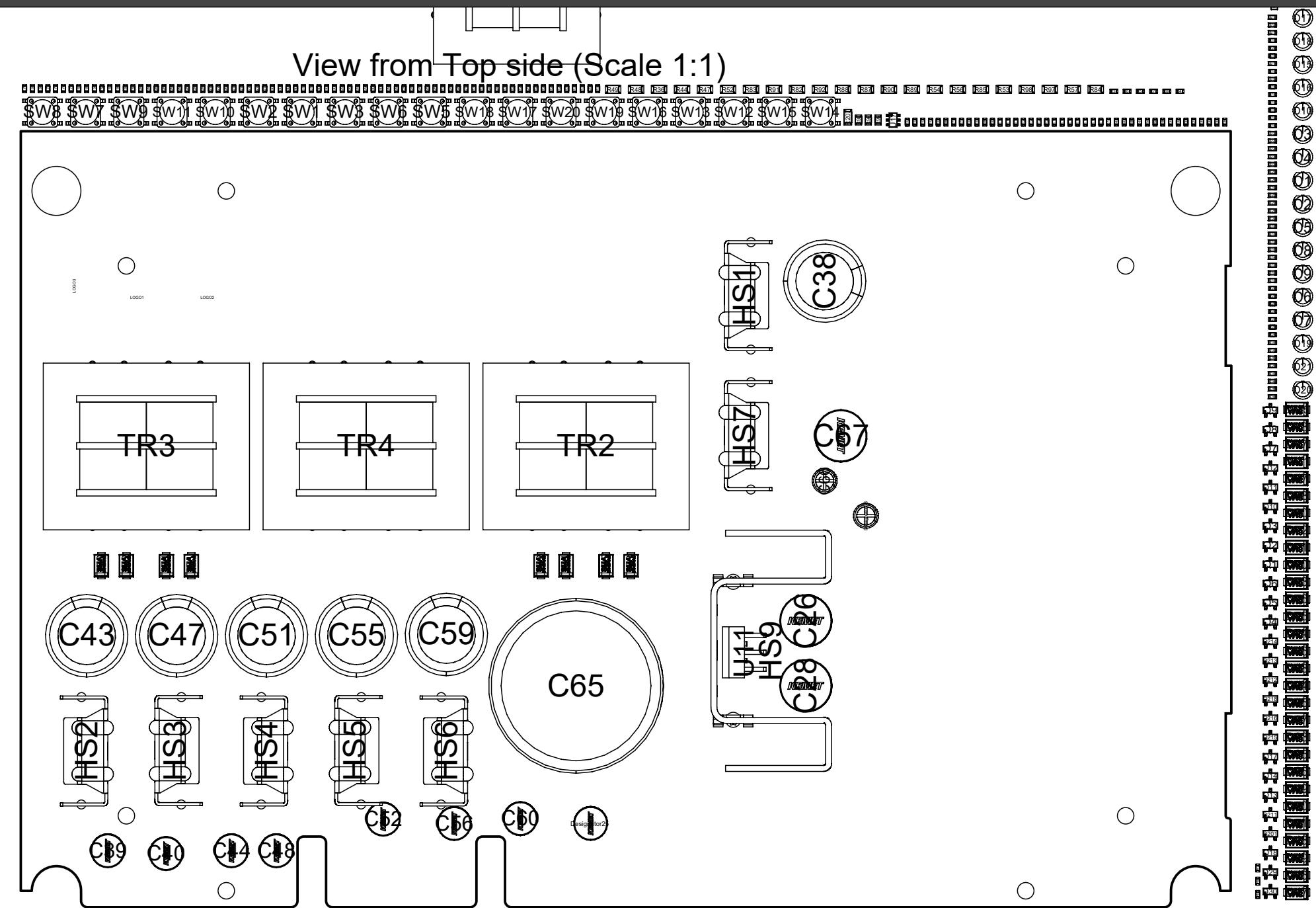
Project CT9042.PjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

## DESIGNATORS FRONT

View from Top side (Scale 1:1)



1

2

3

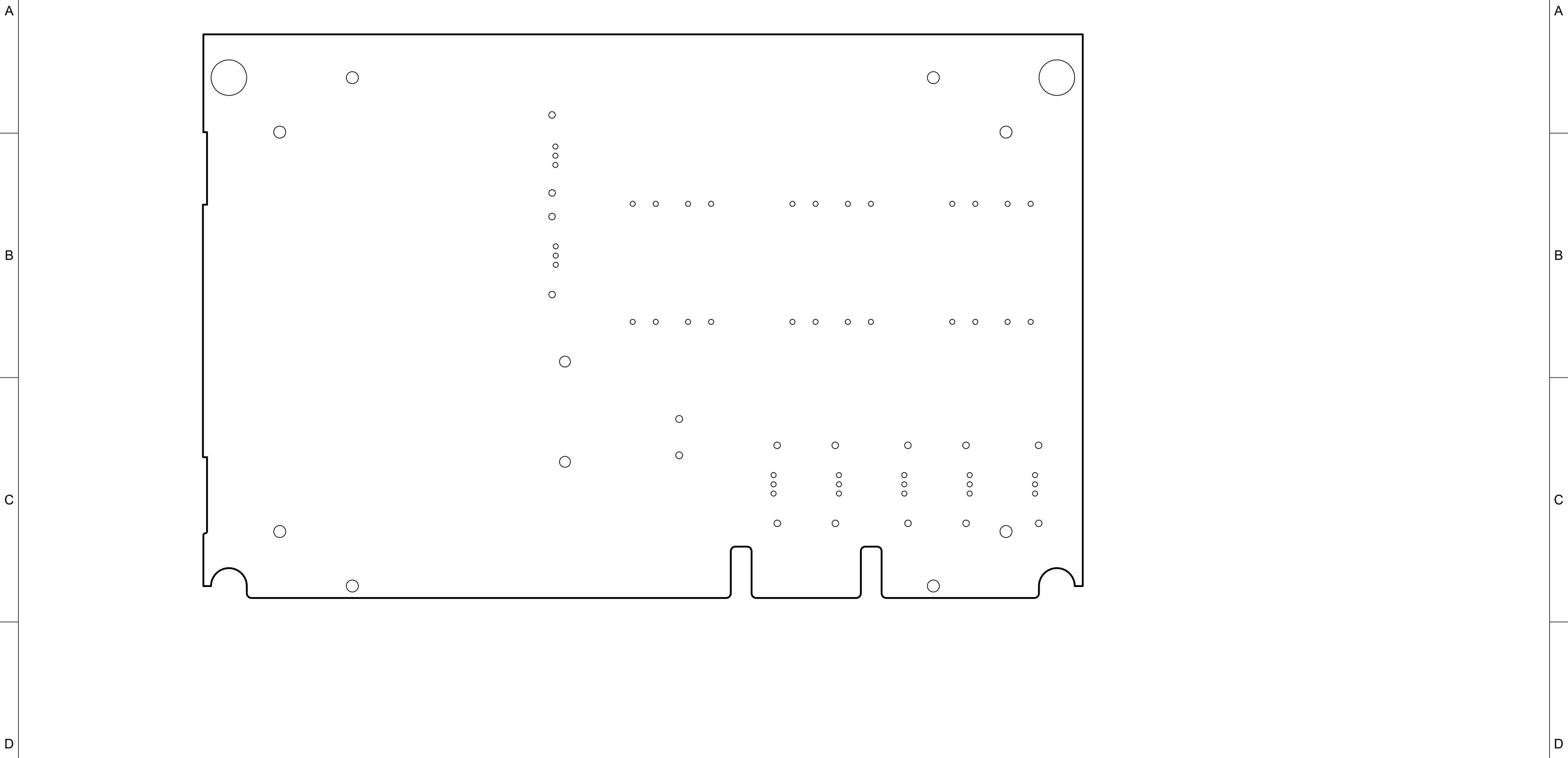
4

5

6

# DESIGNATORS BACK

View from Bottom side (Scale 1:1)



1

2

3

4

5

6

1

2

3

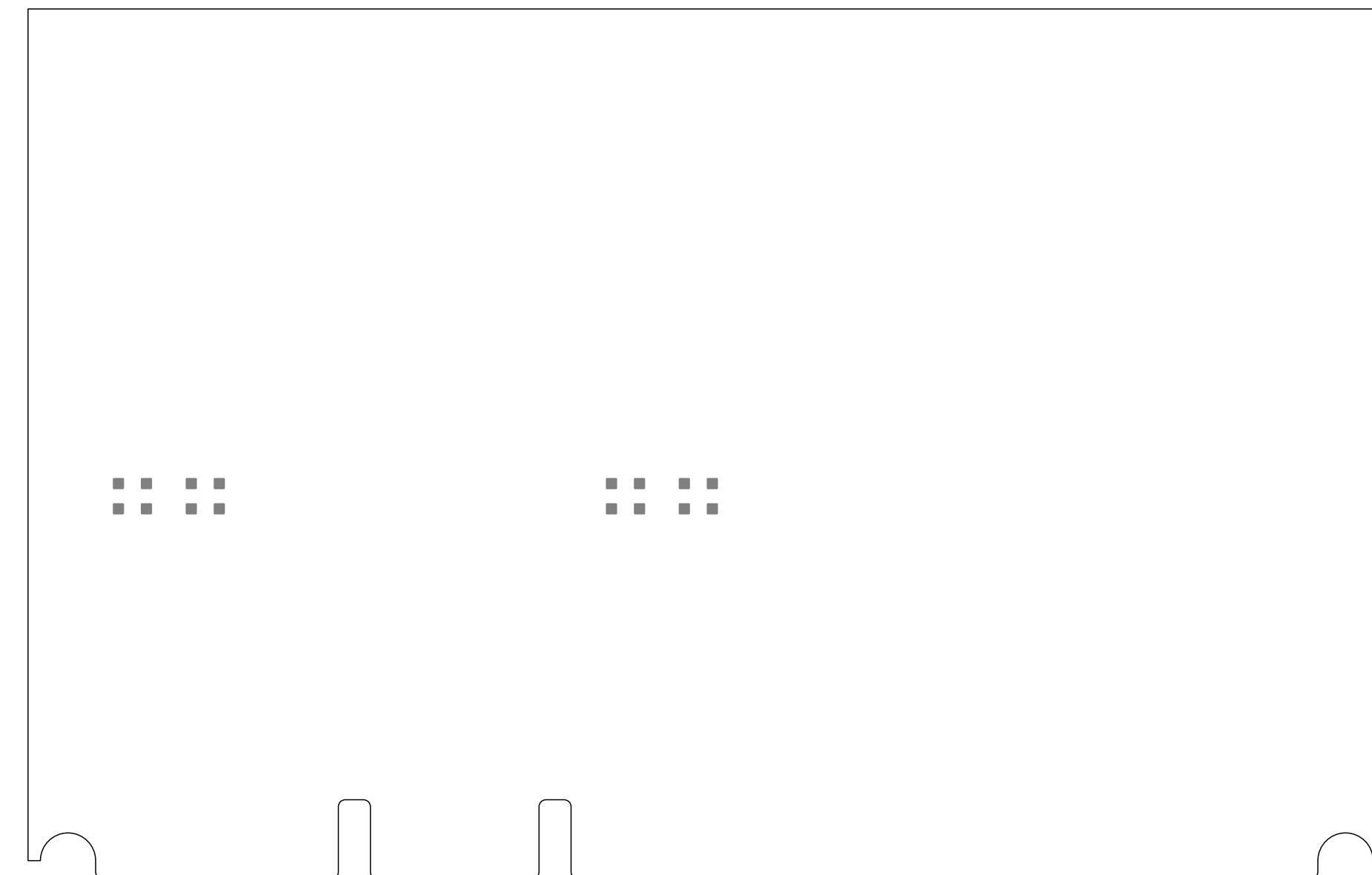
4

5

6

# PASTE MASK TOP

Top Paste (Scale 1:1)



1

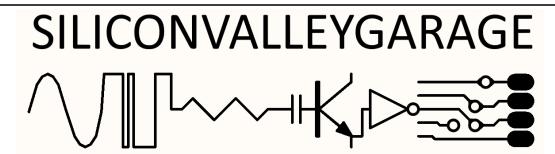
2

3

4

5

6



**Project CT9042.PrjPcb**

Version: | Variant [No Variations]

ASSEMBLY DRAWING

1

2

3

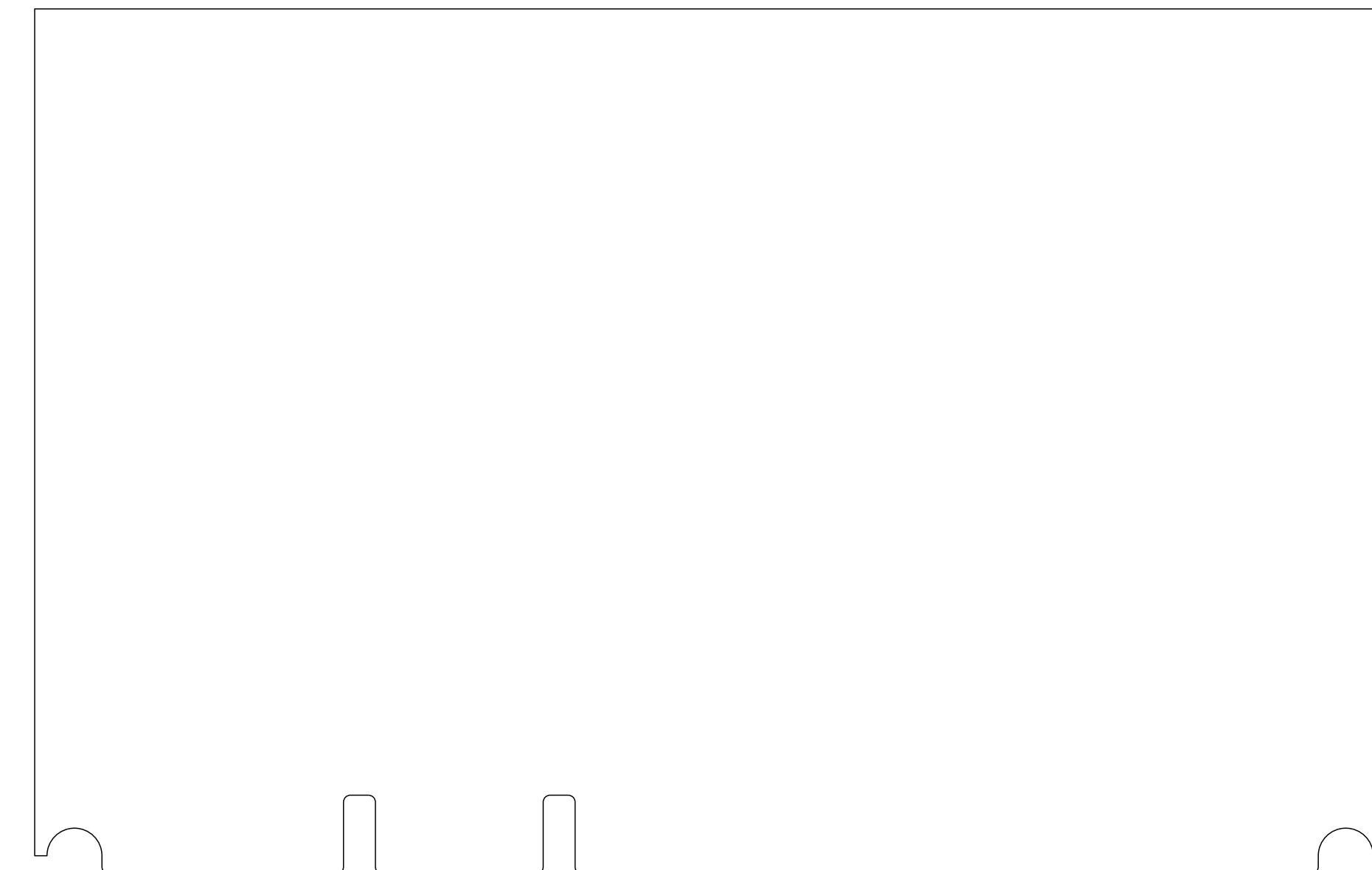
4

5

6

# PASTE MASK BACK

Bottom Paste (Scale 1:1)



A

A

B

B

C

C

D

D