

1

2

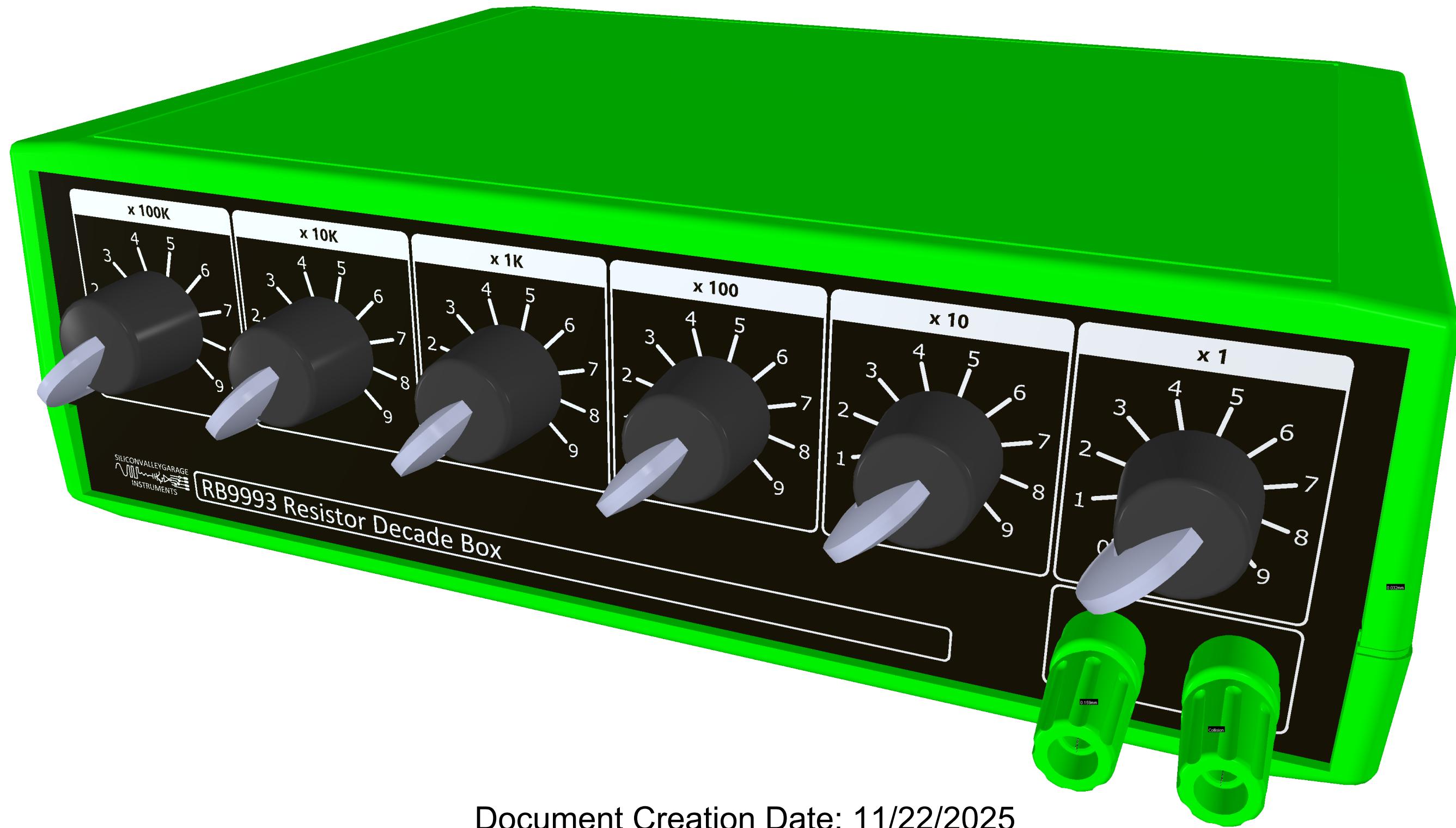
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4

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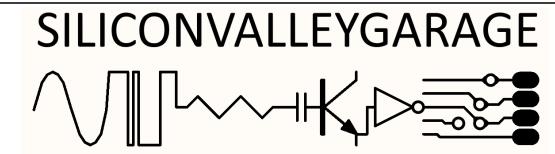
6

ResistorDecadeBox.PrjPcb



Document Creation Date: 11/22/2025

Design : Vincent Himpe



1

2

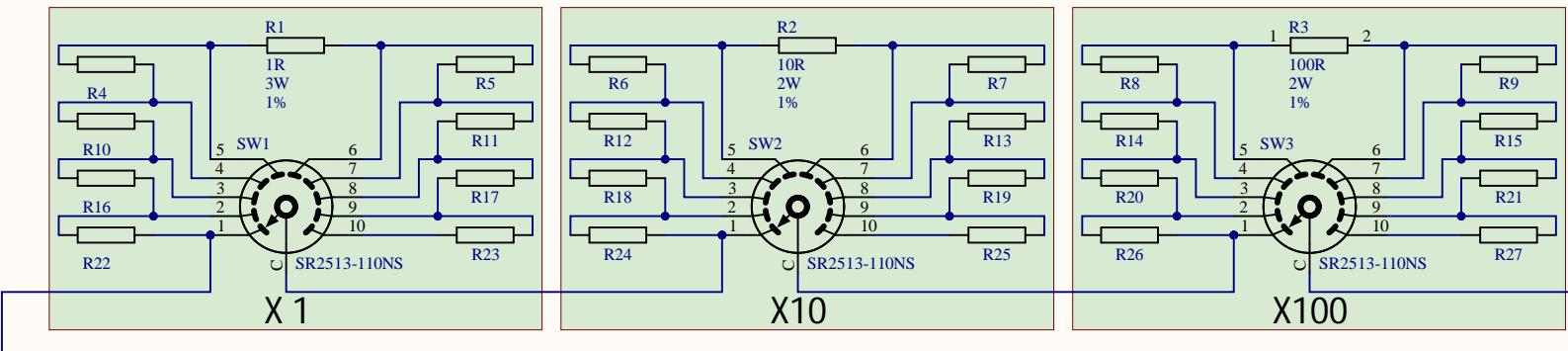
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4

5

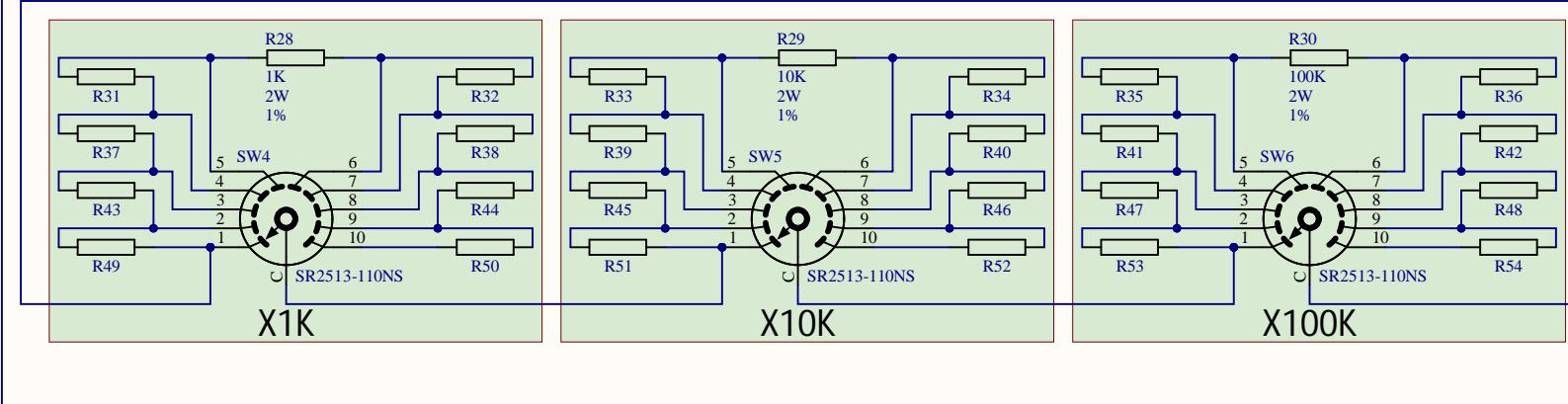
6

A



A

B



B

C



SILICONVALLEYGARAGE

 Instruments

RB9993
 Resistor Decade Box

GitHub :
<https://github.com/vincent-himpe/Resistor-DecadeBox>



D

GENERAL

GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.
3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER
4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2
5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

MATERIALS

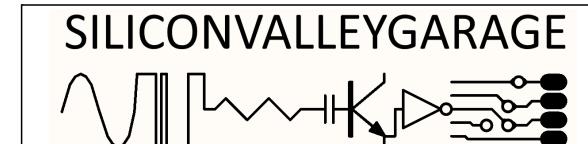
7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY



Project ResistorDecadeBox.PnjPcb

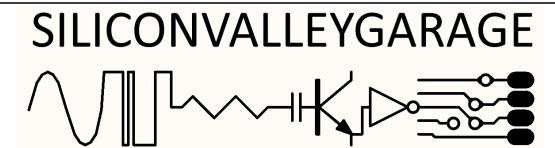
Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER STACK

Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material Type	Gerber Dk	Weight	Constructions	Df Resin
A		Top Overlay			Legend	GTO		
B	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5	
C	Copper	Top Layer	0.036mm(1.400mil)		Signal	GTL	1oz	
D				1.500mm(59.055mil) FR-4	Dielectric		4.8	
E								
F	Copper	Bottom Layer	0.036mm(1.400mil)		Signal	GBL	1oz	
G	Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5	
H		Bottom Overlay			Legend	GBO		
	Total thickness: 1.591mm(62.655mil)							



Project ResistorDecadeBox.PnjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
◊	108	1.100mm(43.307mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
▽	66	1.400mm(55.118mil)	Plated	Round	Top Layer - Bottom Layer	Pad	(Mixed)				
□	2	1.500mm(59.055mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
○	6	3.200mm(125.984mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✖	6	8.000mm(314.961mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
✚	2	14.000mm(551.181mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
190 Total											

A

A

B

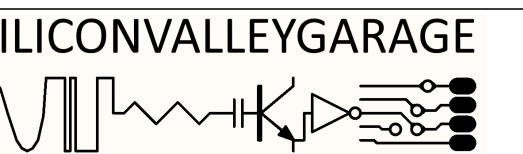
B

C

C

D

D



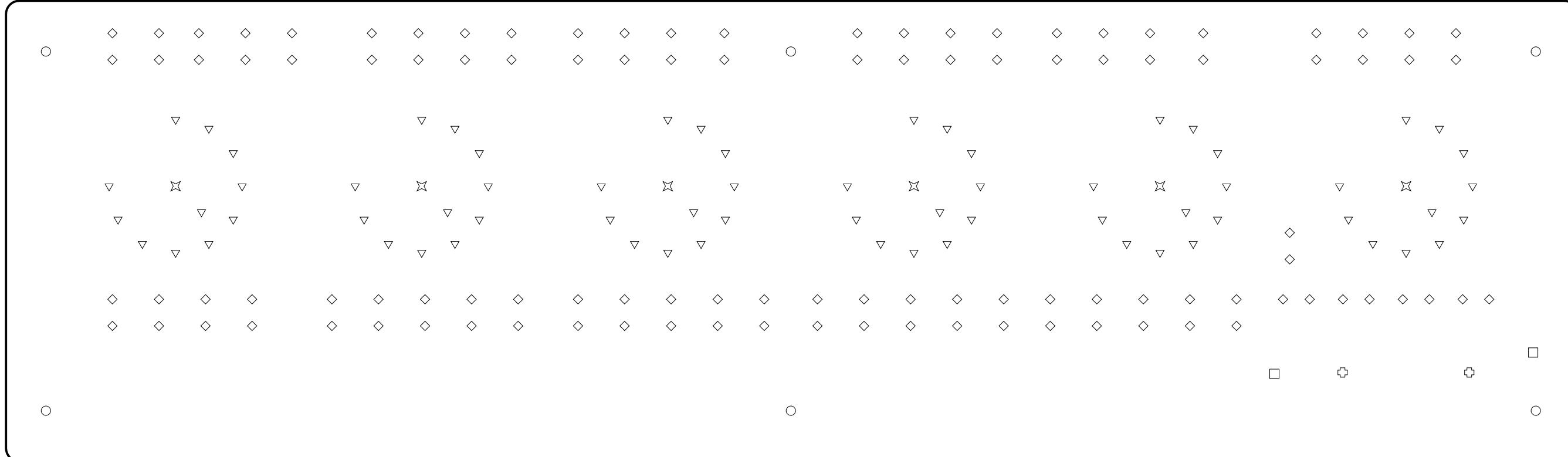
Project ResistorDecadeBox.PnjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL DRAWING

Drill Drawing View (Scale 1.5:1)



25

26

27

28

29

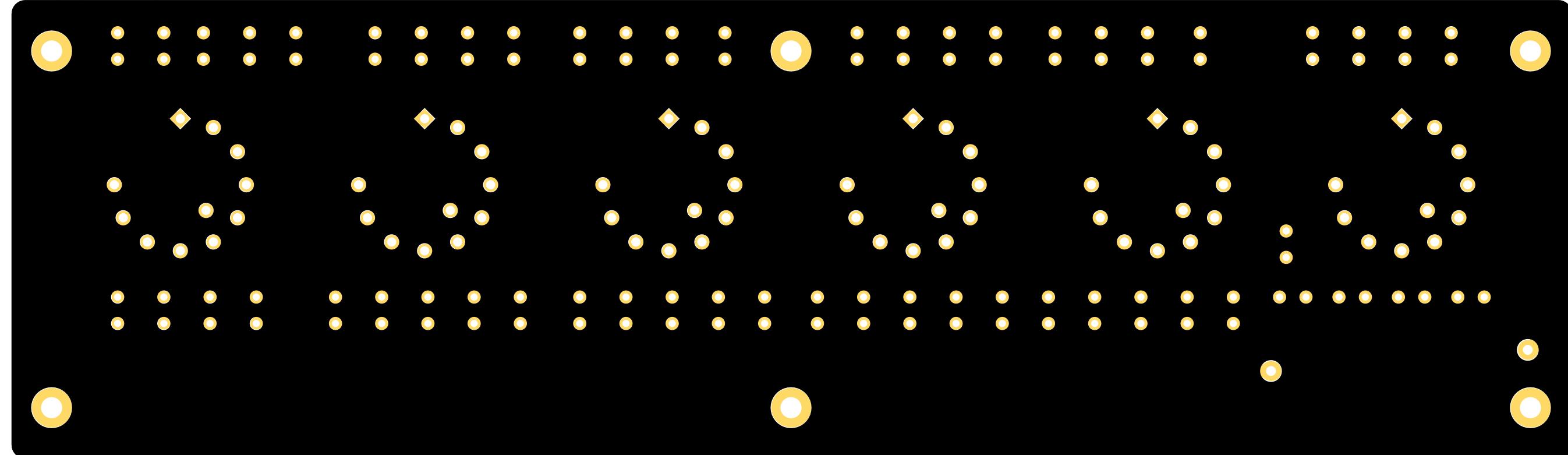
30

COMPOSITE VIEW FRONT

A

A

Top Layer (Scale 1.5:1)



B

B

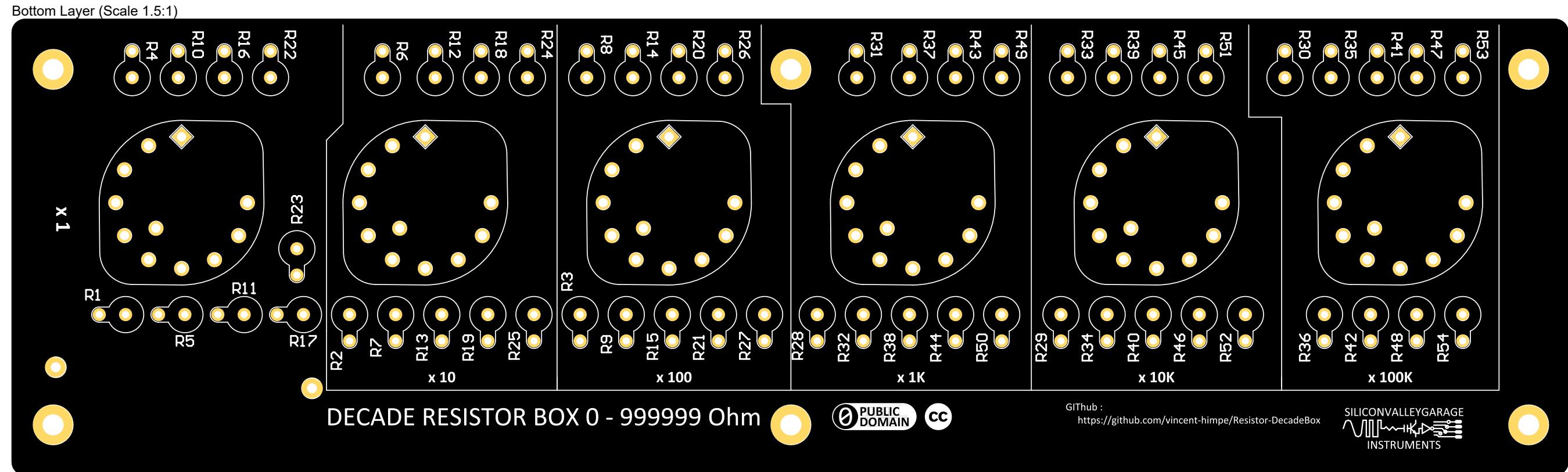
C

C

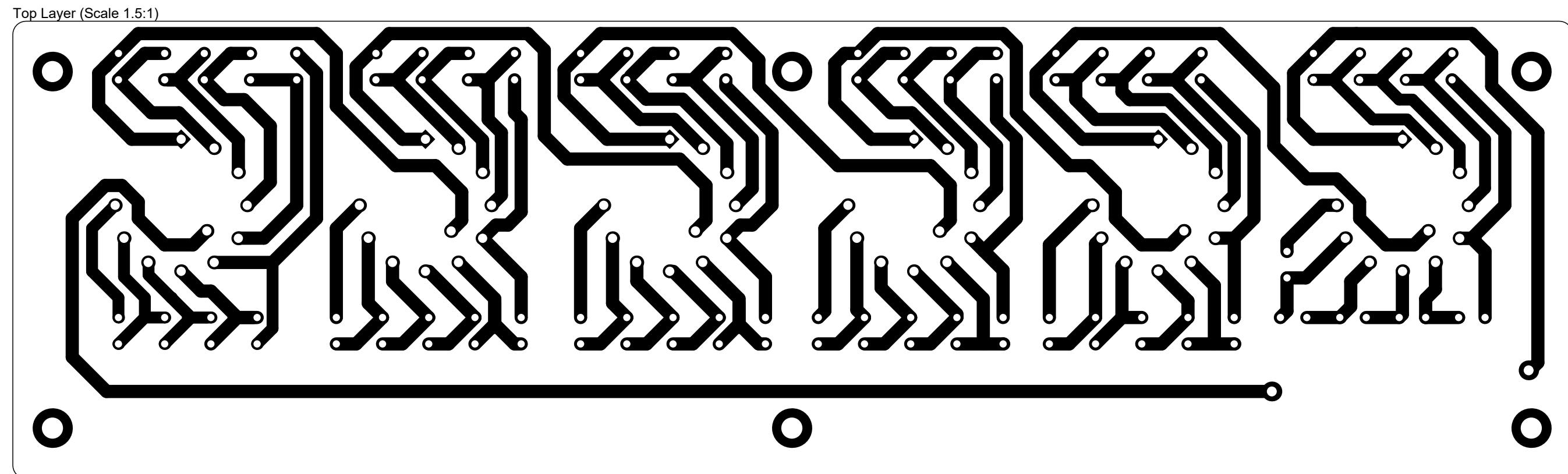
D

D

COMPOSITE VIEW BACK



LAYER VIEW : TOP LAYER



LAYER VIEW : BOTTOM LAYER

A

A

B

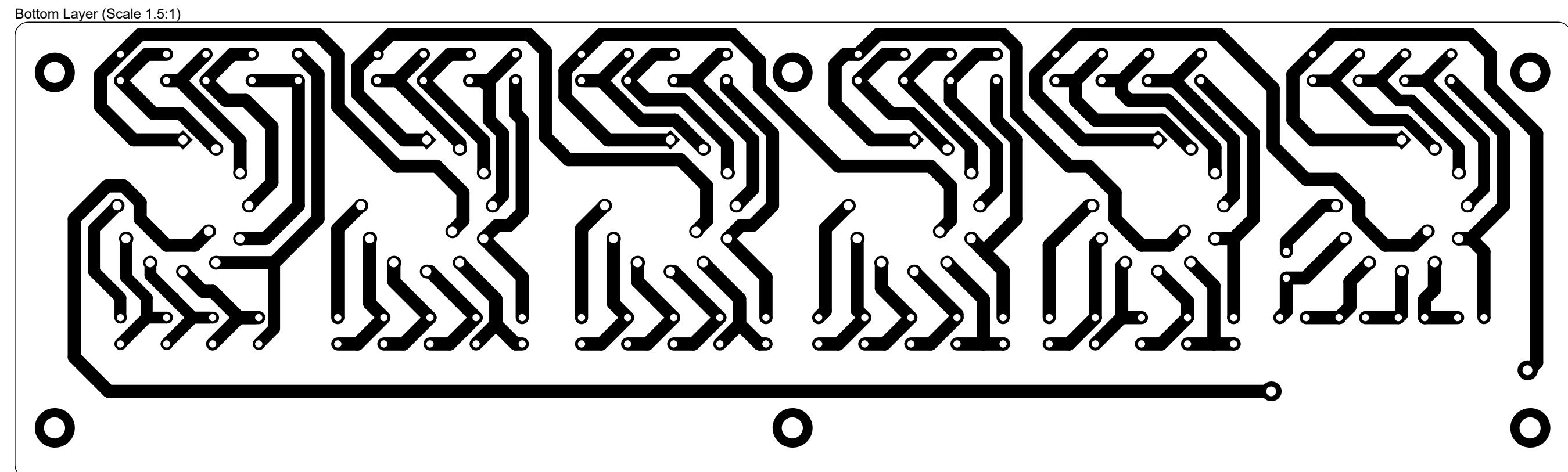
B

C

C

D

D

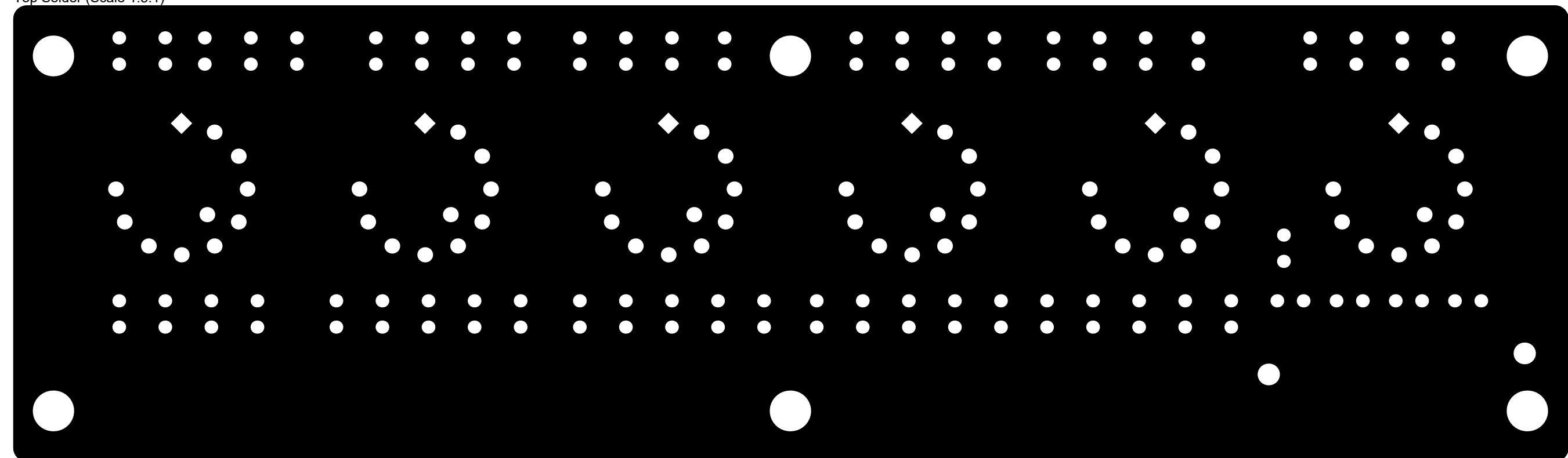


LAYER VIEW : TOP SOLDER MASK

A

A

Top Solder (Scale 1.5:1)



B

B

C

C

D

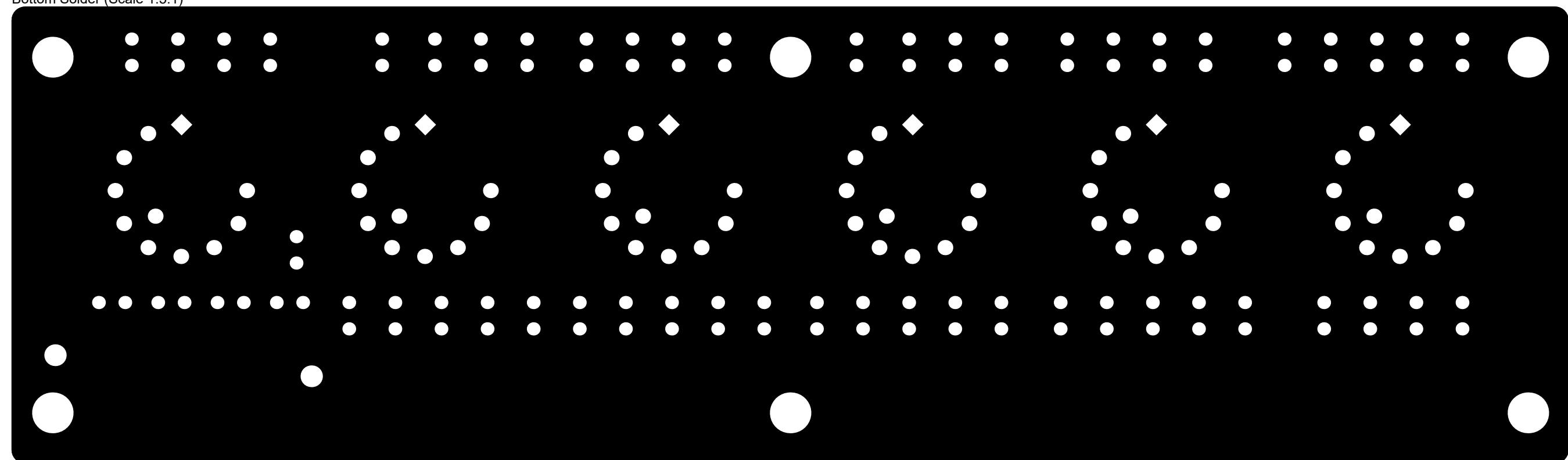
D

LAYER VIEW : BOTTOM SOLDER MASK

A

A

Bottom Solder (Scale 1.5:1)



B

B

C

C

D

D

LAYER VIEW : TOP SILKSCREEN (LEGEND)

A

A

B

B

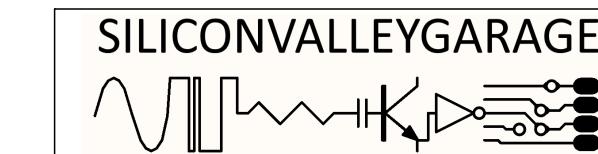
C

C

D

D

Top Overlay (Scale 1.5:1)



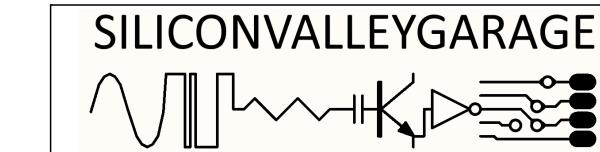
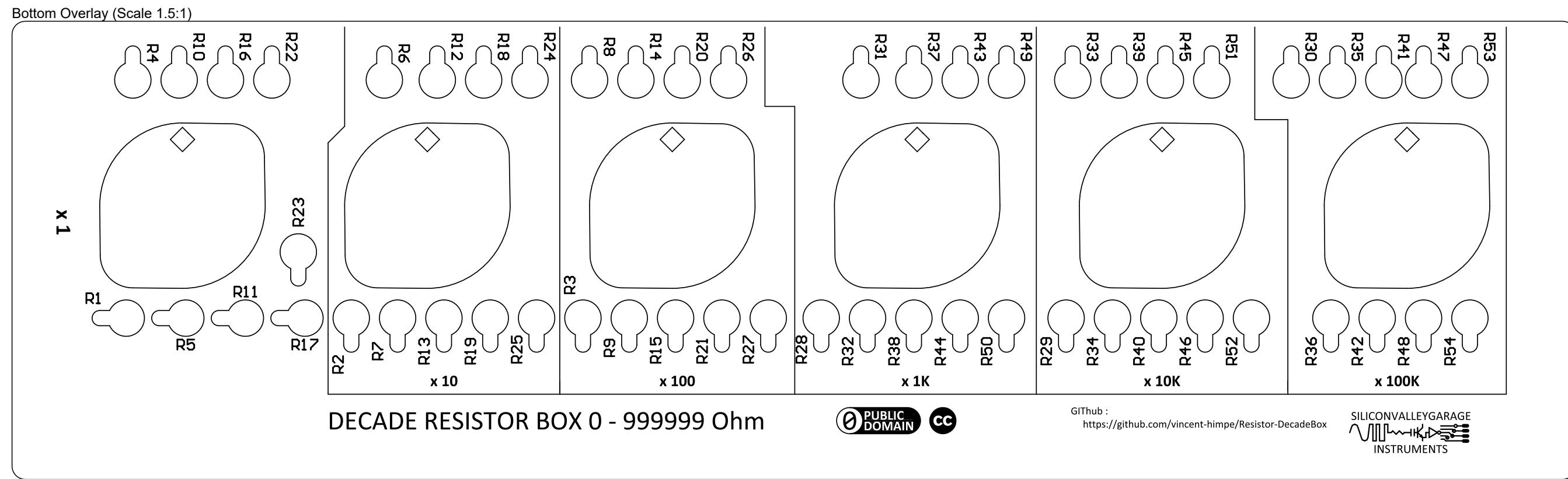
SILICONVALLEYGARAGE

Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)



Project ResistorDecadeBox.PnjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

GENERAL



A Unless otherwise specified the following rules apply:

1. DO NOT DEVIATE FROM ARTWORK OR BOM WITHOUT PRIOR AUTHORIZATION.
2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

B Bill of Materials and Material Handling

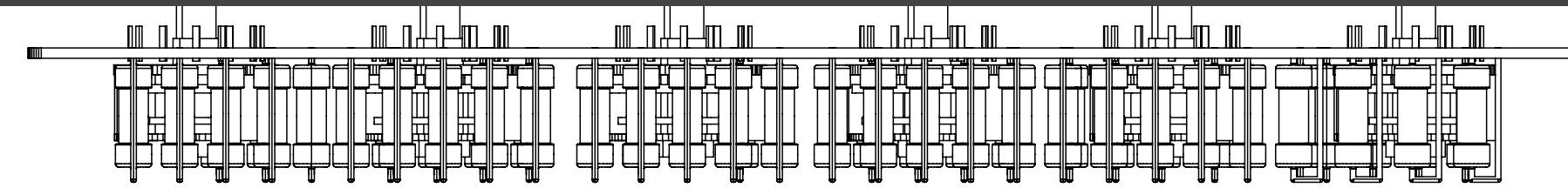
3. THE BOM CONTAINED IN THIS DOCUMENT IS AS-BUILT. NON-INSTALLED PARTS HAVE BEEN REMOVED. ADDITIONAL BOM FORMATS ARE AVAILABLE IN THE PROJECT FILES
4. ANY PART SUBSTITUTIONS MUST BE APPROVED IN WRITING BEFORE ASSEMBLY
5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
7. ESD CONTROL PER IPC RULES

B Soldering

8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
10. SOLDERING PREFERABLY TO BE DONE USING NITROGEN ATMOSPHERE
11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

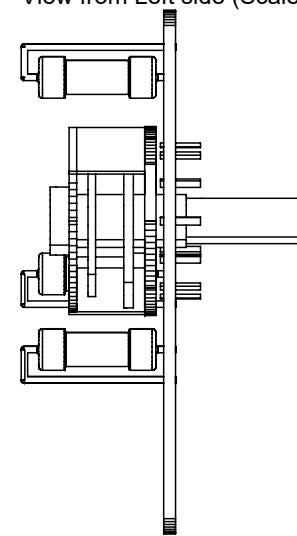
2D VIEW

A

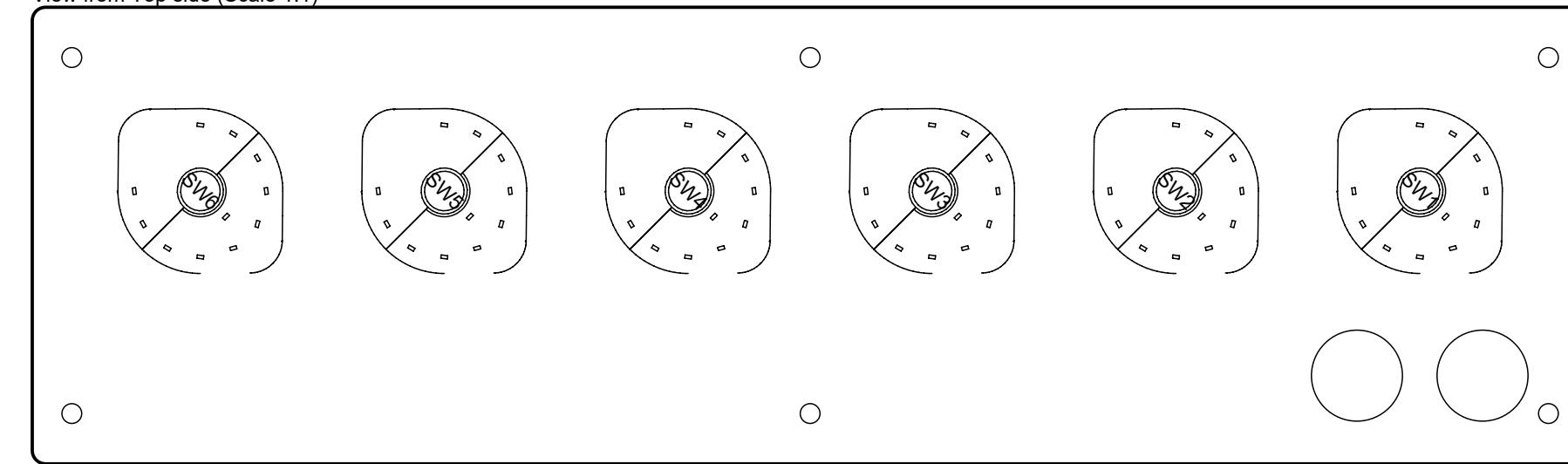


A

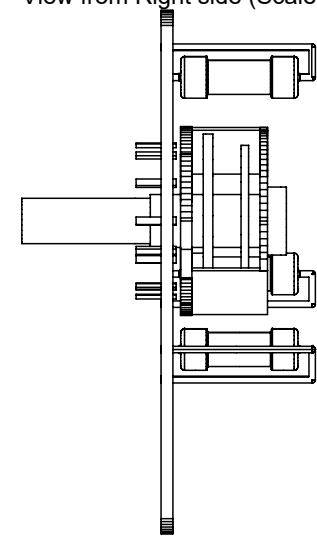
View from Left side (Scale 1:1)



View from Top side (Scale 1:1)

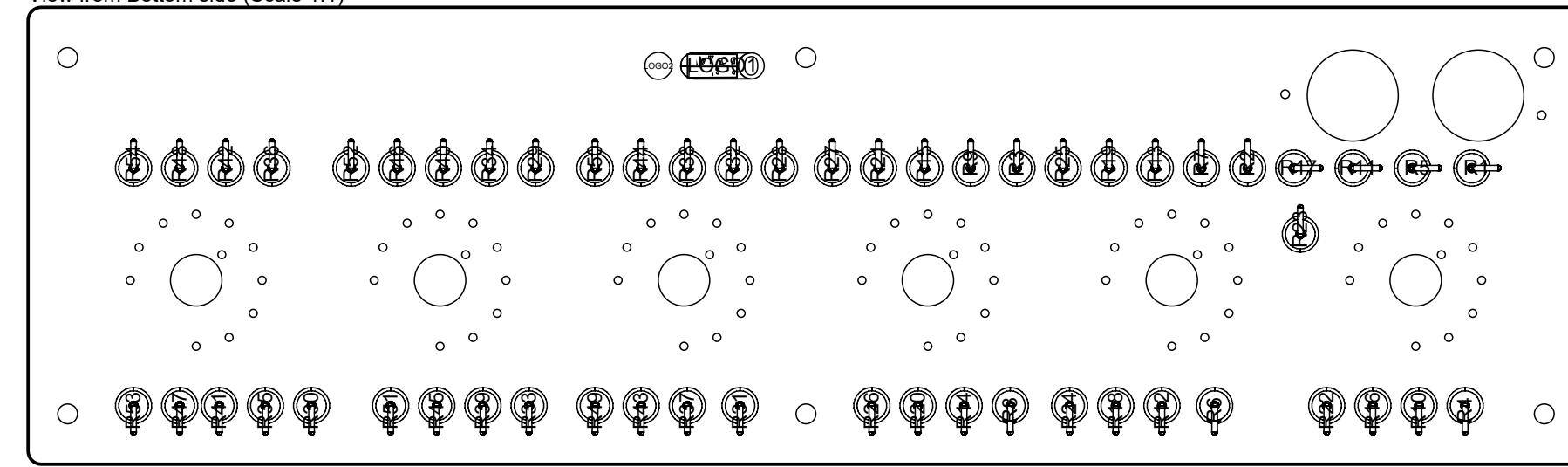


View from Right side (Scale 1:1)



B

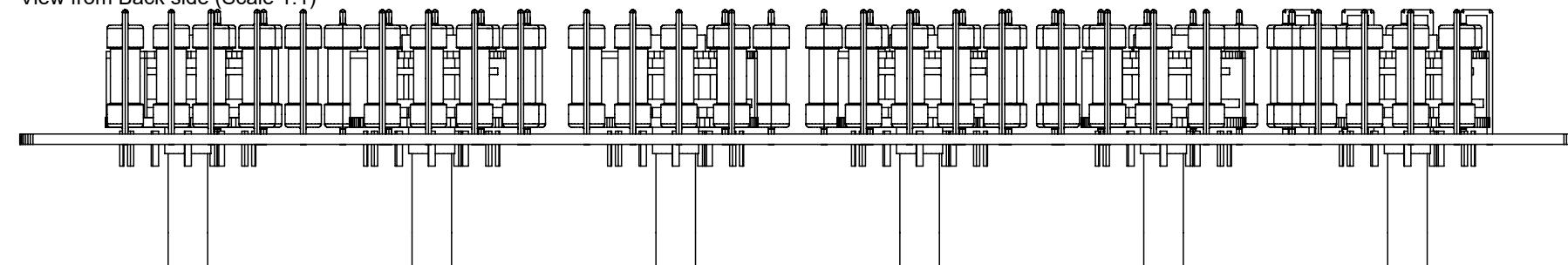
View from Bottom side (Scale 1:1)



B

C

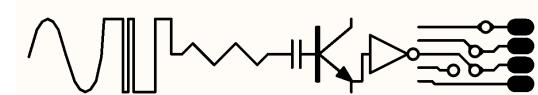
View from Back side (Scale 1:1)



C

D

SILICONVALLEYGARAGE



Project ResistorDecadeBox.PnjPcb

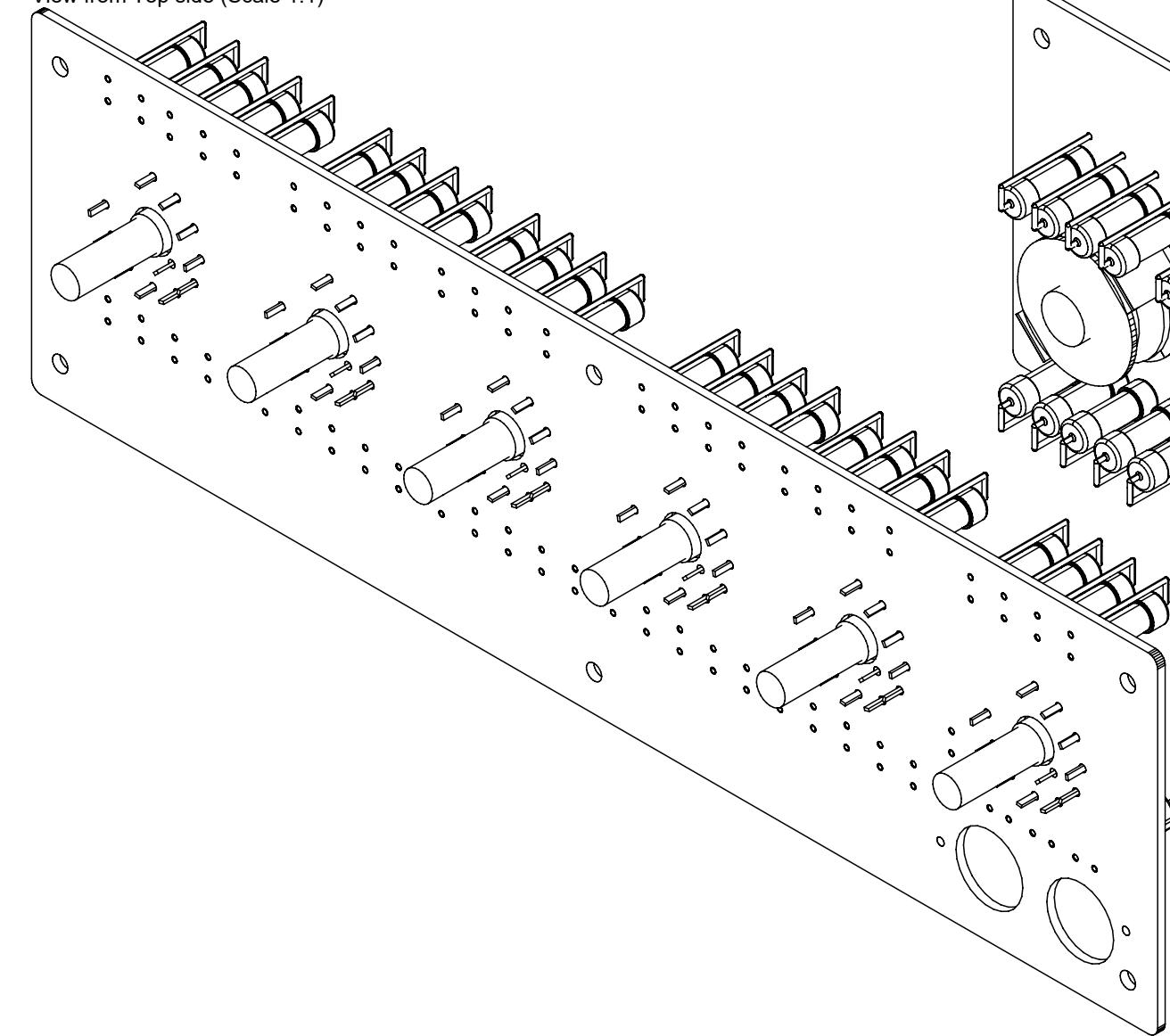
Version: | Variant [No Variations]

ASSEMBLY DRAWING

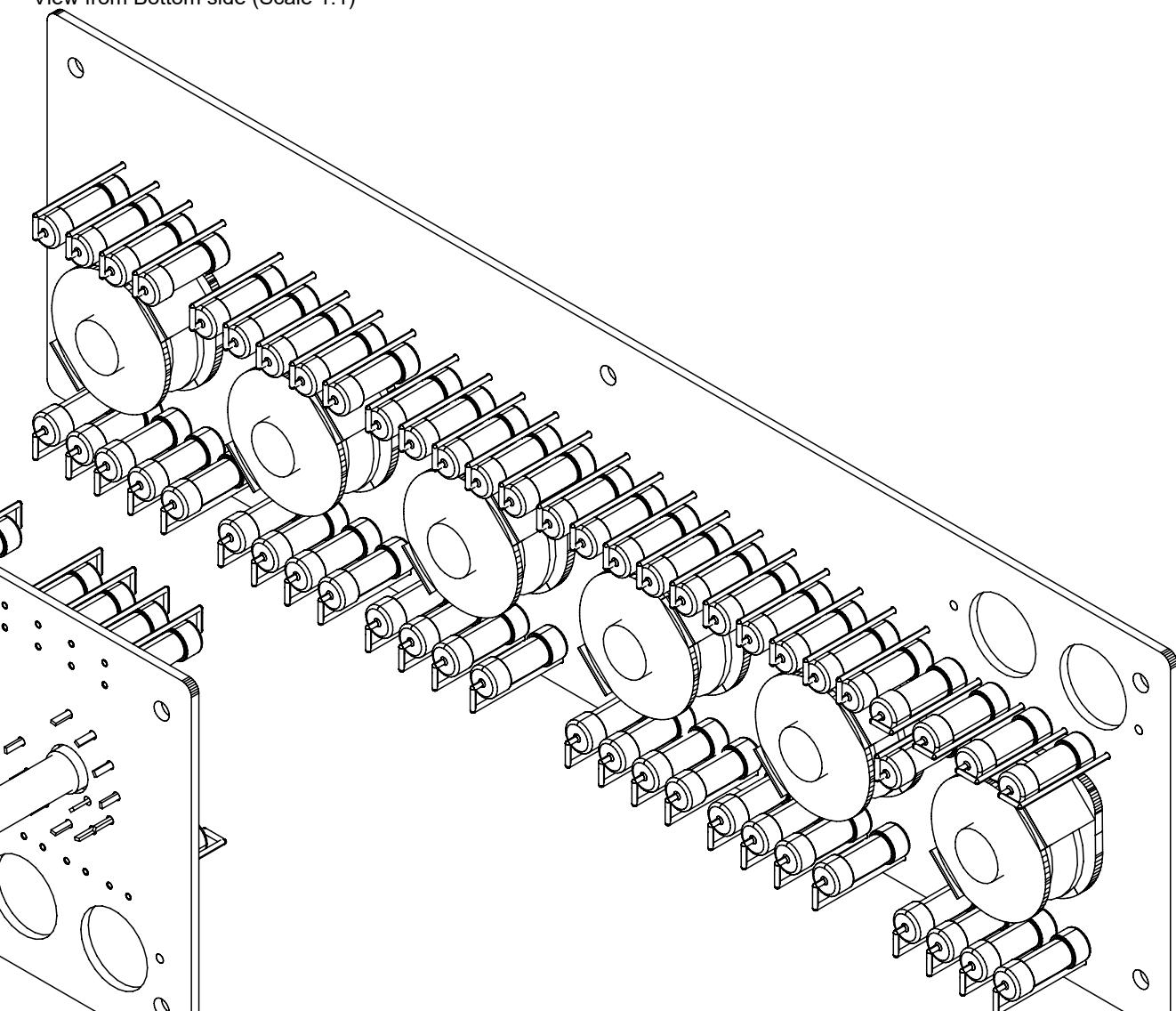
3D VIEW

A

View from Top side (Scale 1:1)



View from Bottom side (Scale 1:1)



B

C

D

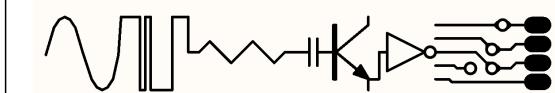
A

B

C

D

SILICONVALLEYGARAGE



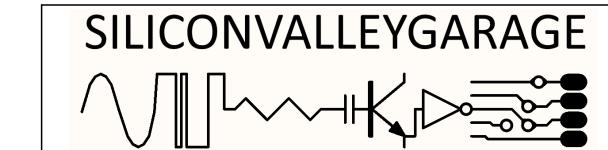
Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

Bill Of Materials

Quantity	Designator	Description	Manufacturer 1	Manufacturer Part Number 1	DIGIKEY
1	J1	CONNECTOR,BANANA BINDING POST,BLACK,CLIFF CL15XX	CLIFF ELECTRONICS	CL1505	4654-CL1505-ND
1	J2	CONNECTOR,BANANA BINDING POST,RED,CLIFF CL15XX	CLIFF ELECTRONICS	CL1506	4654-CL1506-ND
6	M13, M14, M15, M16, M17, M18	MECH,STANDOFF,M3.5.11mm,SMD,WURTH	WURTH	9775041360R	732-10919-1-ND
1	MECH1	ENCLOSURE,ABS,GRAY,HAMMOND, RM2095M	HAMMOND	RM2095M	HM1100-ND
9	R1, R4, R5, R10, R11, R16, R17, R22, R23	RESISTOR,TH,VERT,1R,1%,3W	YAGEO	FMP300FRF73-1R	13-FMP300FRF73-1RCT-ND
9	R2, R6, R7, R12, R13, R18, R19, R24, R25	RESISTOR,TH,VERT,10R,1%,2W	YAGEO	MFR200FRF52-10R	13-MFR200FRF52-10RCT-ND
9	R3, R8, R9, R14, R15, R20, R21, R26, R27	RESISTOR,TH,VERT,100R,1%,2W	YAGEO	FMP200FRF52-100R	100YCT-ND
9	R28, R31, R32, R37, R38, R43, R44, R49, R50	RESISTOR,TH,VERT,1K,1%,2W	YAGEO	MFR200FRF52-1K	13-MFR200FRF52-1KCT-ND
9	R29, R33, R34, R39, R40, R45, R46, R51, R52	RESISTOR,TH,VERT,10K,1%,2W	YAGEO	FMP200FRF52-10K	10KYCT-ND
9	R30, R35, R36, R41, R42, R47, R48, R53, R54	RESISTOR,TH,VERT,100K,1%,2W	YAGEO	MFR200FRF52-100K	13-MFR200FRF52-100KCT-ND
6	SW1, SW2, SW3, SW4, SW5, SW6	SWITCH,SP10T,ROTARY,TH,REAR MOUNT,ALPHA SR2512-XXX	TAIWAN ALPHA	SR2513-110NS	5942-SR2513-110NS-ND



Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

DESIGNATORS FRONT

A

A

B

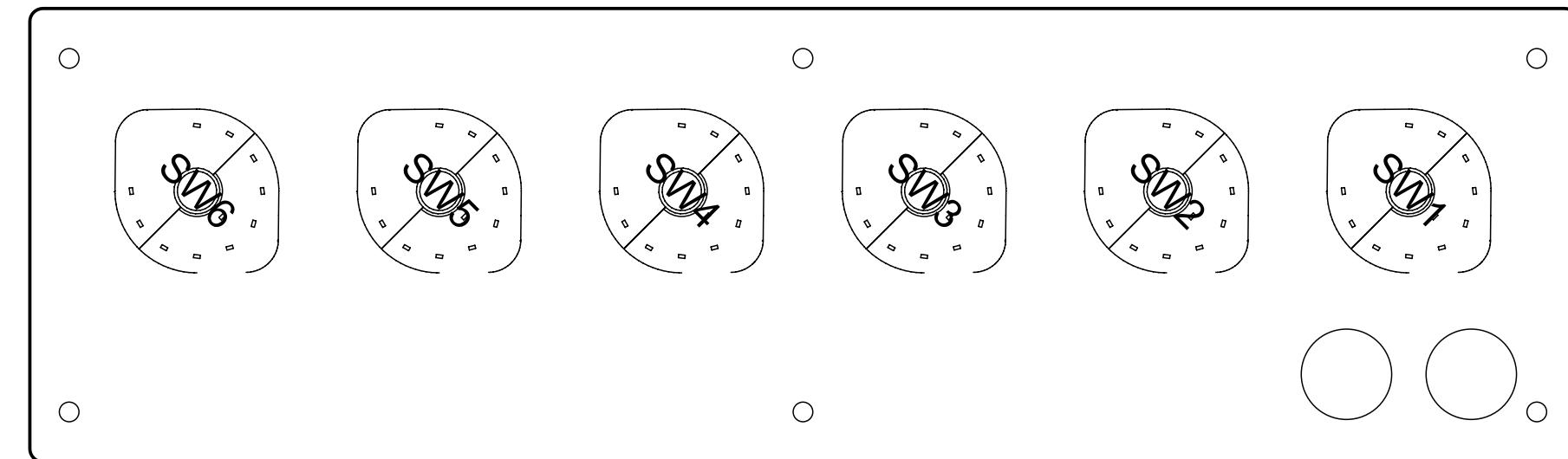
B

C

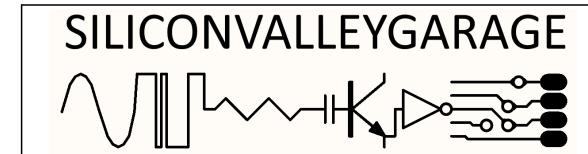
C

D

D



View from Top side (Scale 1:1)



Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

DESIGNATORS BACK

A

A

B

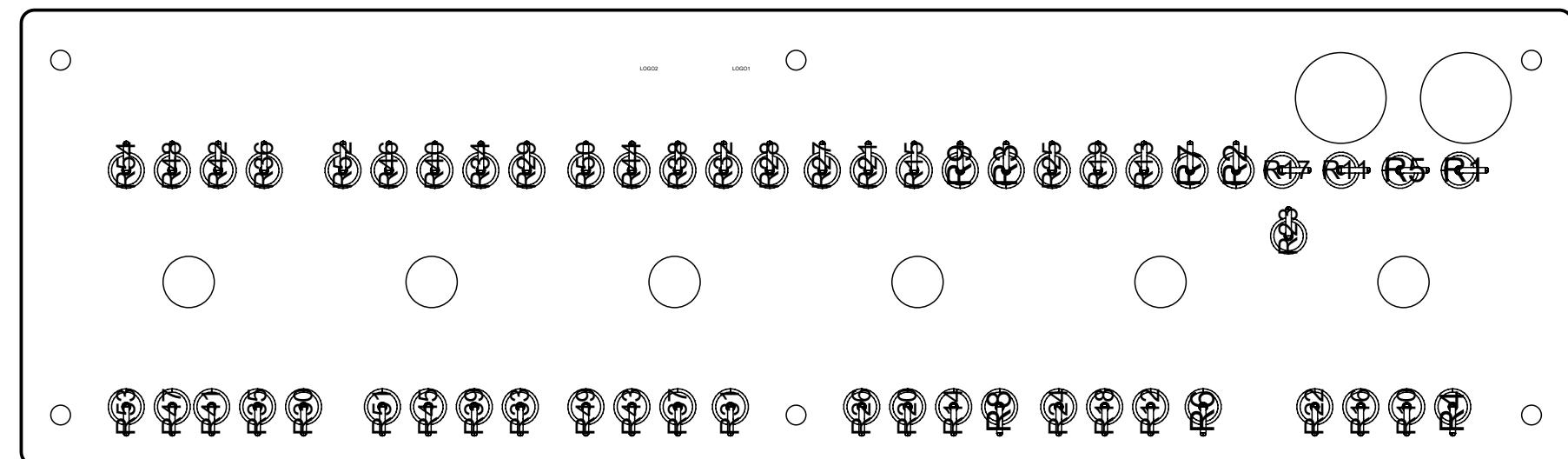
B

C

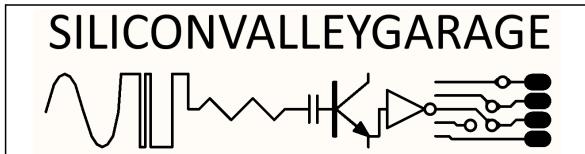
C

D

D



View from Bottom side (Scale 1:1)



Project ResistorDecadeBox.PnjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

GENERAL

GENERAL

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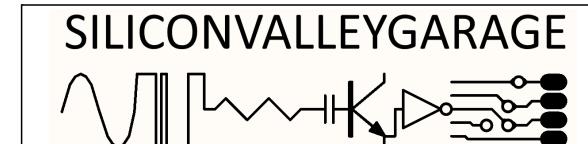
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10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
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QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY



Project ResistorDecadeBox.PnjPcb

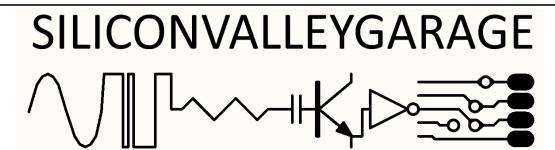
Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER STACK

Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material Type	Gerber Dk	Weight	Constructions	Df Resin
A	Top Overlay	Top Overlay		Legend	GTO			
B	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5	
C	Copper	Top Layer	0.036mm(1.400mil)		Signal	GTL	1oz	
D				0.320mm(12.600mil) FR-4	Dielectric		4.8	
E								
F	Copper	Bottom Layer	0.036mm(1.400mil)		Signal	GBL	1oz	
G	Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5	
H		Bottom Overlay			Legend	GBO		
	Total thickness: 0.411mm(16.200mil)							



Project ResistorDecadeBox.PnjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

CONTROLLED IMPEDANCE

A

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Substack	Clearance	Target Tolerance
--------------	-------------------	------------------	----------------------	-------------	------------------	--------------------	------------------	----------	-----------	------------------

B

A

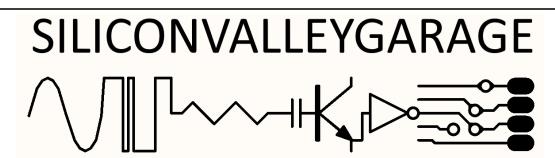
C

B

D

C

D



Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
□	6	0.800mm(31.496mil)	Plated	Round	Top Layer - Bottom Layer	Via					
+	6	8.000mm(314.961mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
	12 Total										

A

A

B

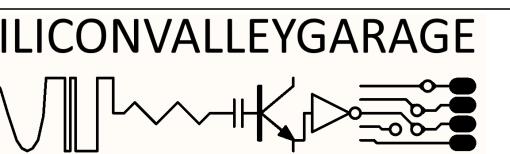
B

C

C

D

D



Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL DRAWING

A

A

B

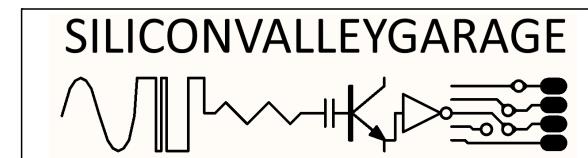
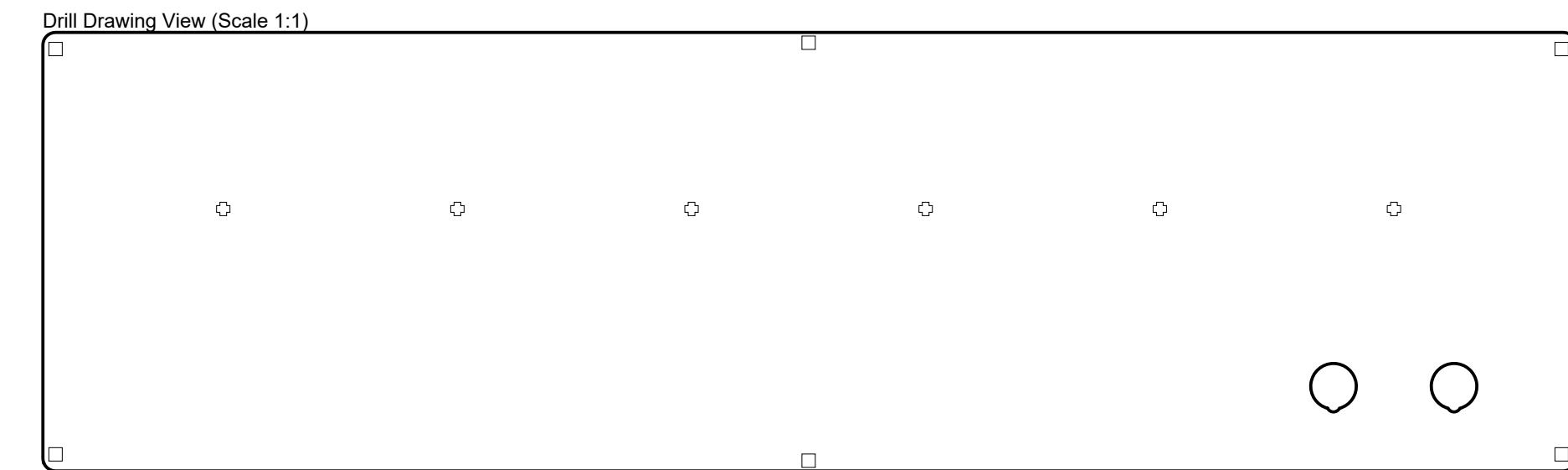
B

C

C

D

D



Project ResistorDecadeBox.PnjPcb
Version: | Variant [No Variations]
FABRICATION DRAWING

COMPOSITE VIEW FRONT

A

A

B

B

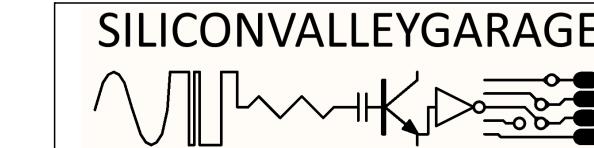
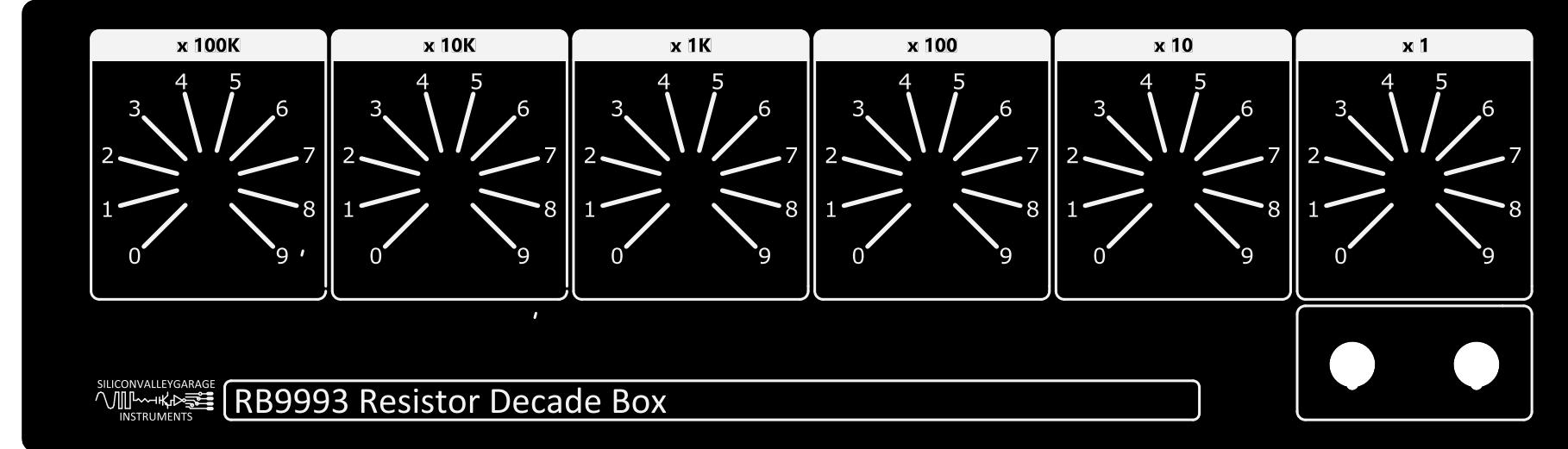
C

C

D

D

Top Layer (Scale 1:1)



Project ResistorDecadeBox.PnjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

COMPOSITE VIEW BACK

A

A

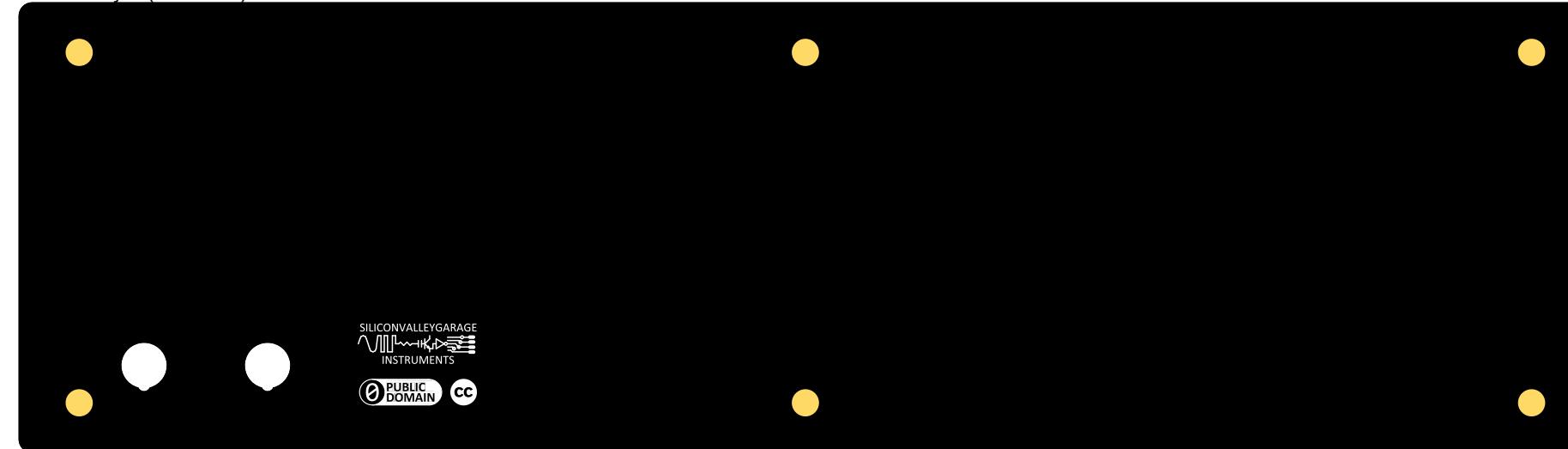
B

B

C

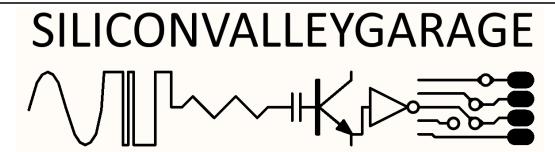
C

Bottom Layer (Scale 1:1)



D

D

**Project ResistorDecadeBox.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP LAYER

A

A

B

B

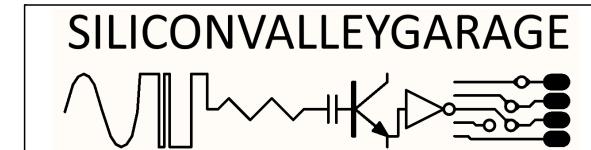
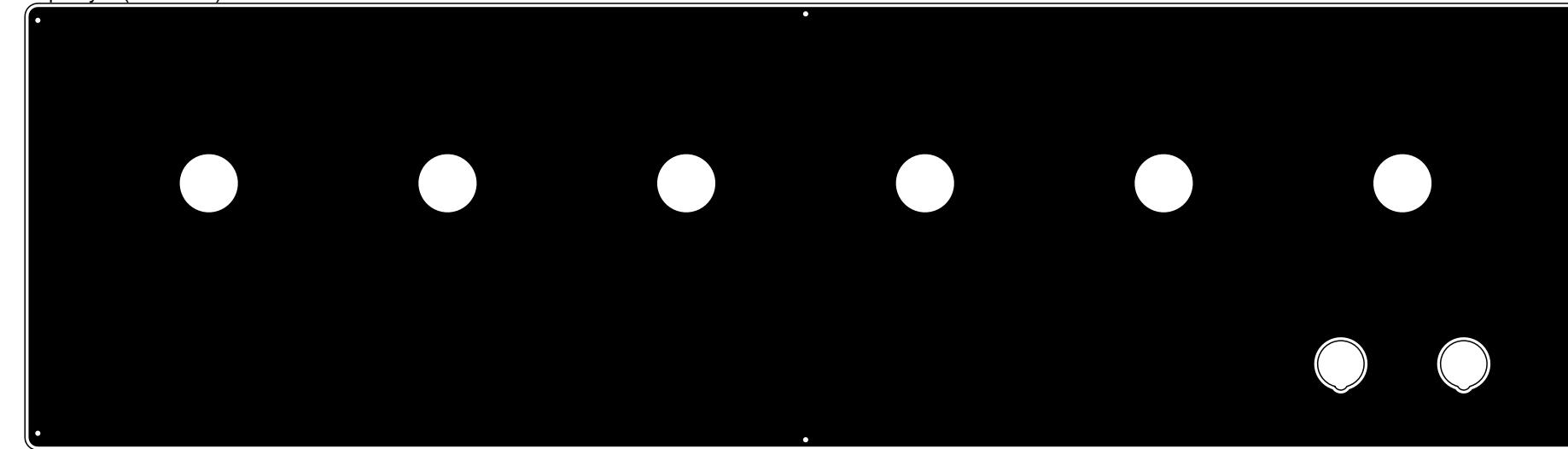
C

C

D

D

Top Layer (Scale 1:1)

**Project ResistorDecadeBox.PrjPcb**

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM LAYER

A

A

B

B

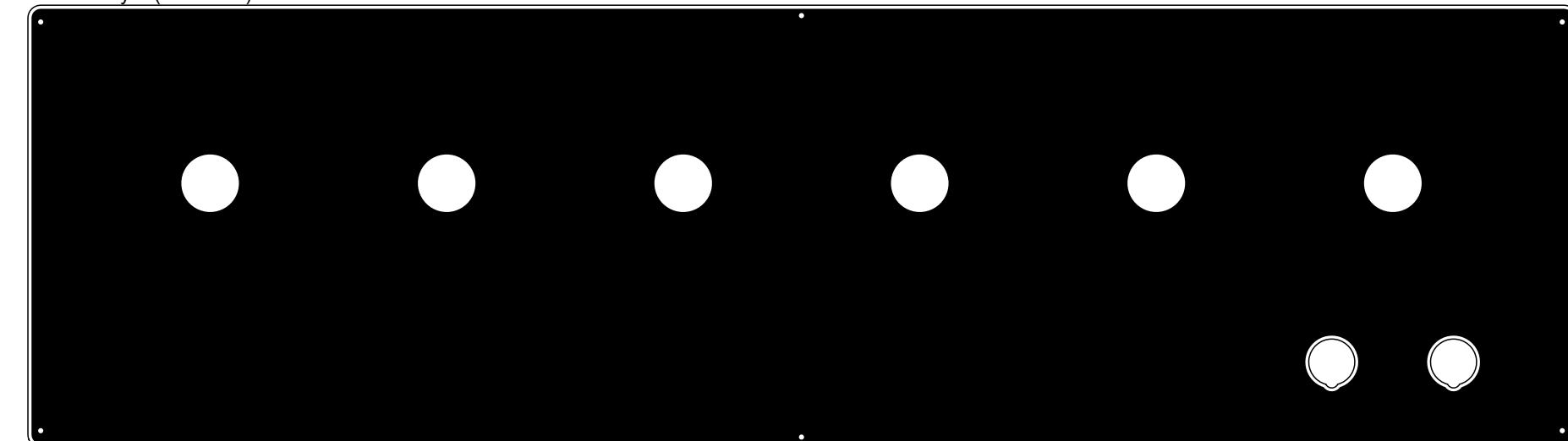
C

C

D

D

Bottom Layer (Scale 1:1)



LAYER VIEW : TOP SOLDER MASK

A

A

B

B

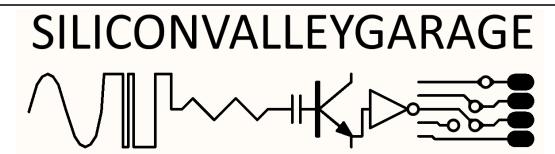
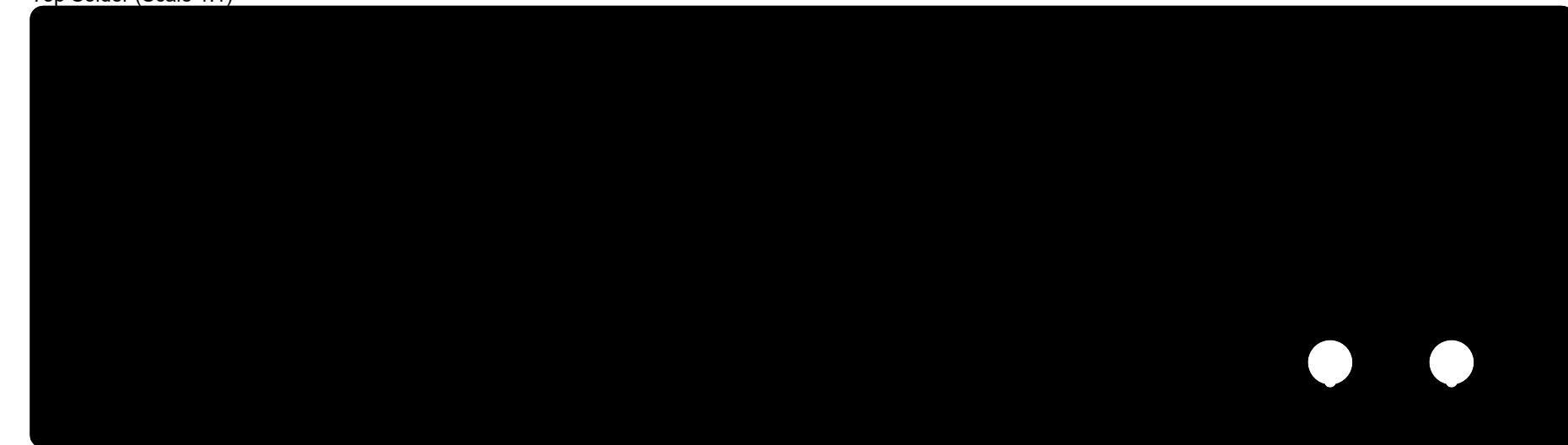
C

C

D

D

Top Solder (Scale 1:1)

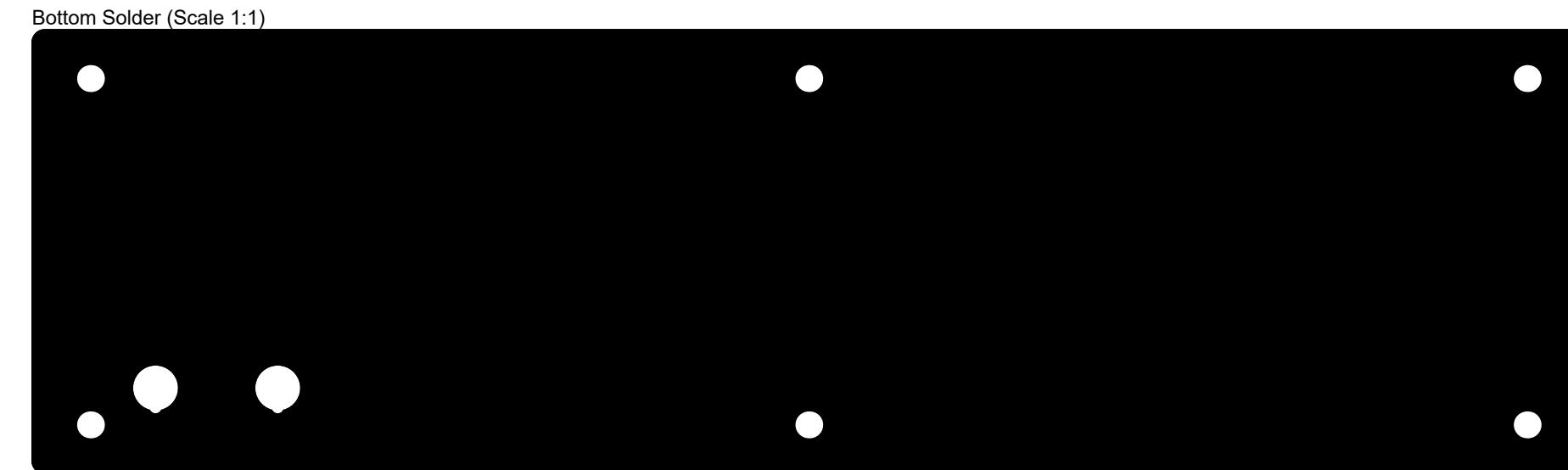


Project ResistorDecadeBox.PrjPcb

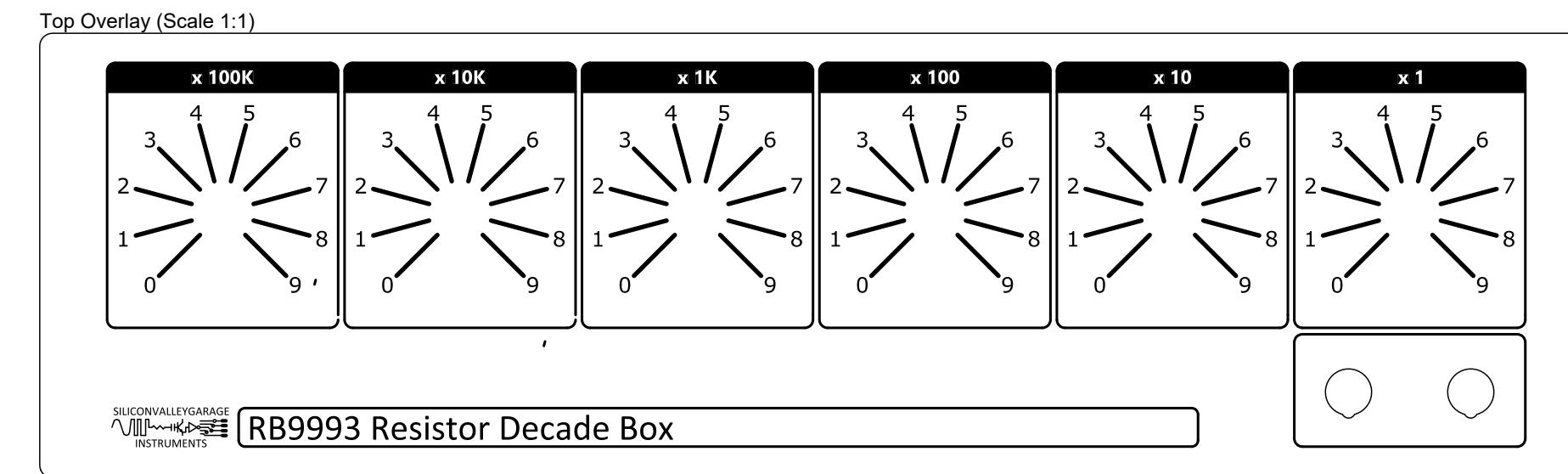
Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SOLDER MASK



LAYER VIEW : TOP SILKSCREEN (LEGEND)



LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

A

A

B

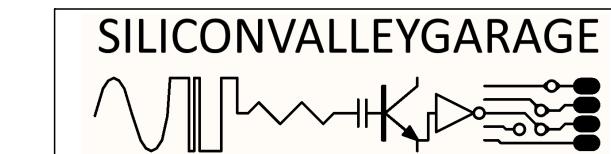
B

C

C

D

D

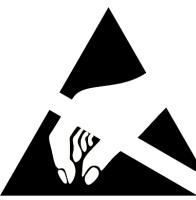


Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

GENERAL



A Unless otherwise specified the following rules apply:

1. DO NOT DEVIATE FROM ARTWORK OR BOM WITHOUT PRIOR AUTHORIZATION.
2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

B Bill of Materials and Material Handling

3. THE BOM CONTAINED IN THIS DOCUMENT IS AS-BUILT. NON-INSTALLED PARTS HAVE BEEN REMOVED. ADDITIONAL BOM FORMATS ARE AVAILABLE IN THE PROJECT FILES
4. ANY PART SUBSTITUTIONS MUST BE APPROVED IN WRITING BEFORE ASSEMBLY
5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
7. ESD CONTROL PER IPC RULES

B Soldering

8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
10. SOLDERING PREFERABLY TO BE DONE USING NITROGEN ATMOSPHERE
11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

3D VIEW

A

A

B

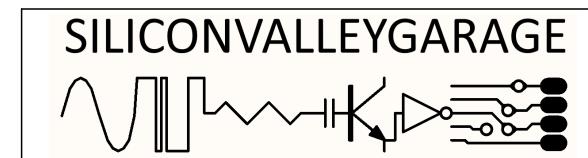
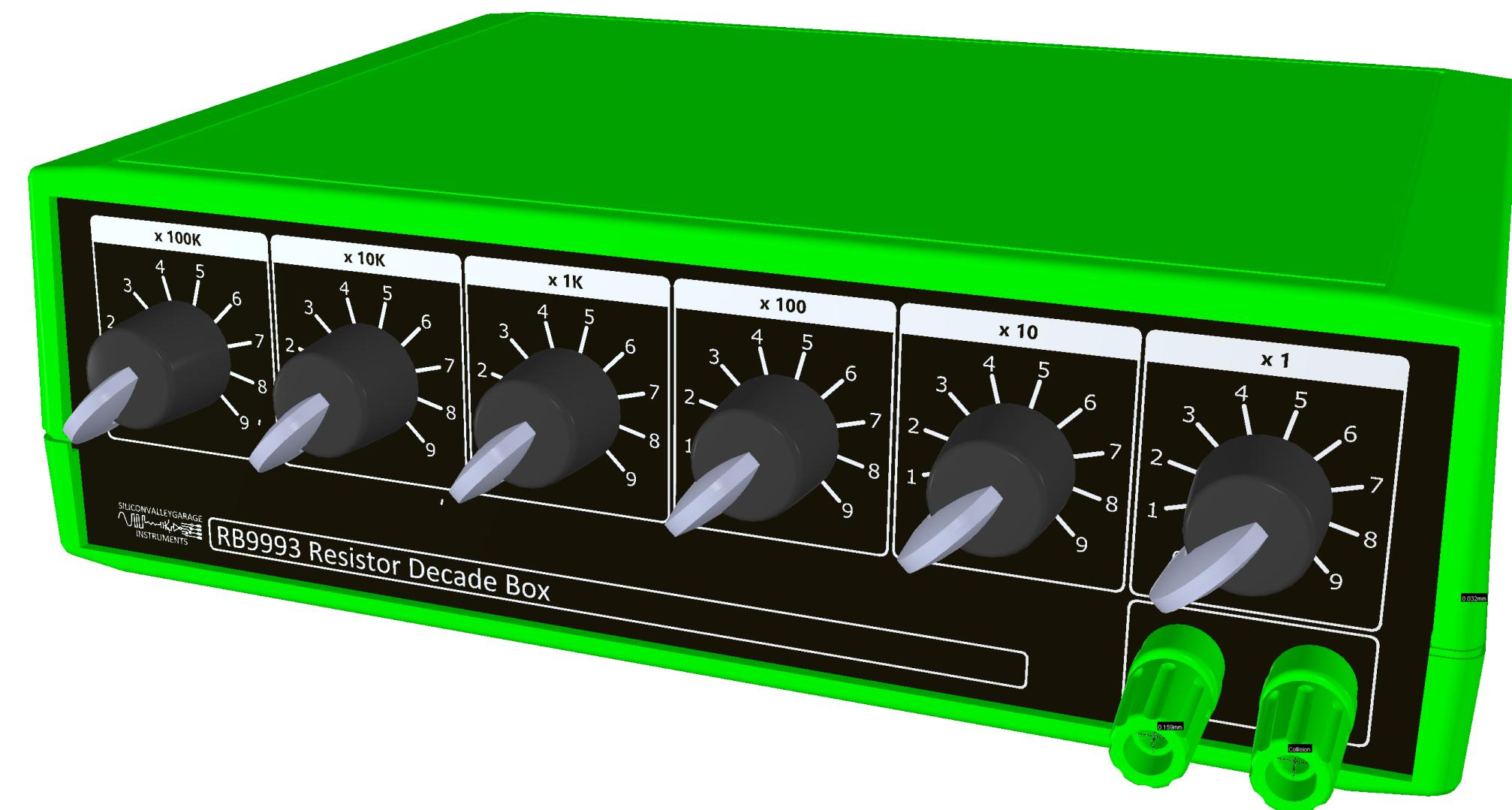
B

C

C

D

D



Project ResistorDecadeBox.PnjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING