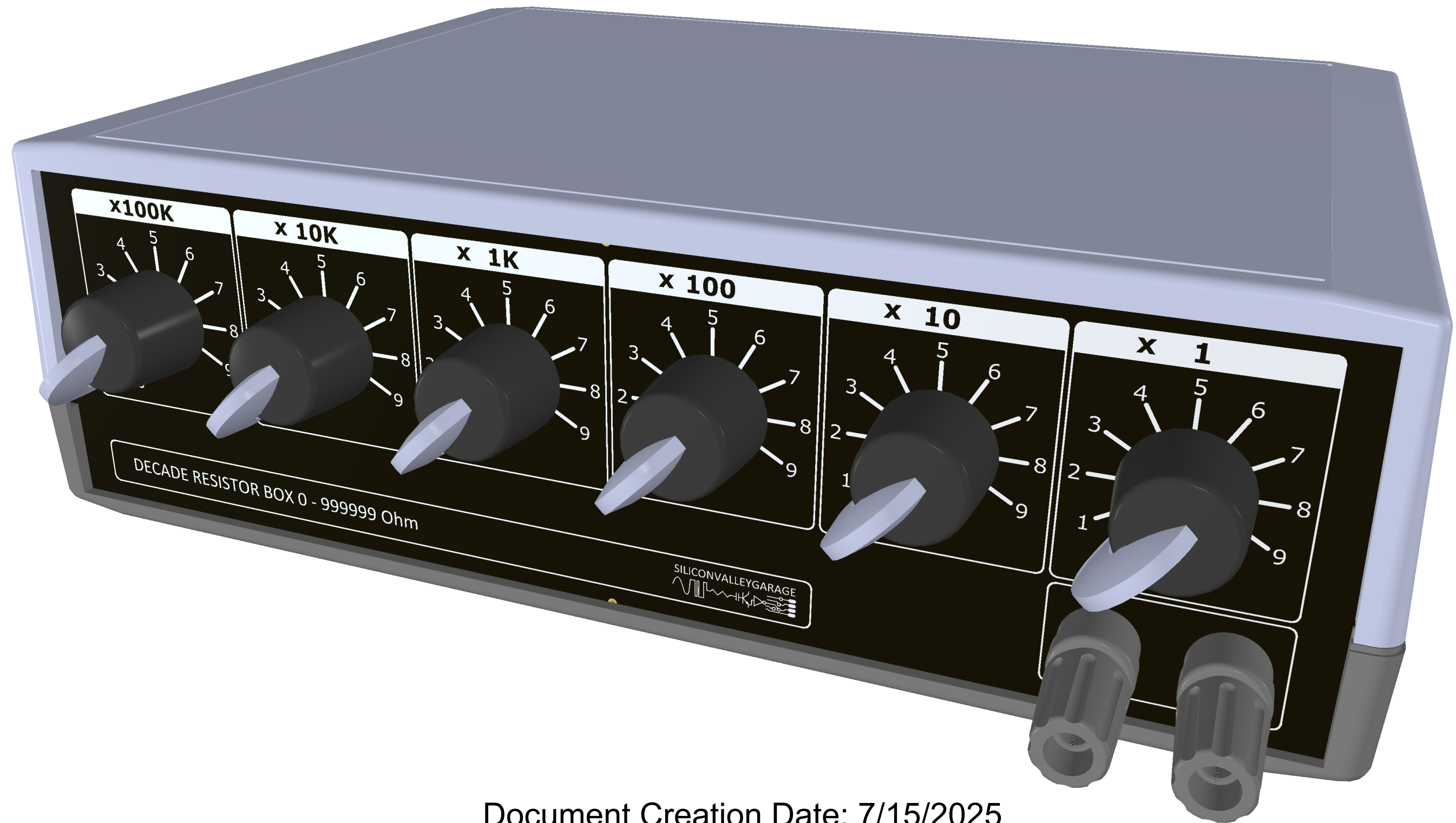


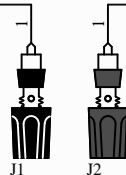
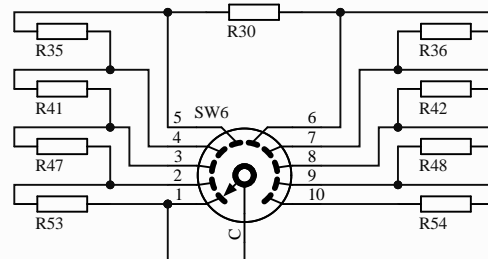
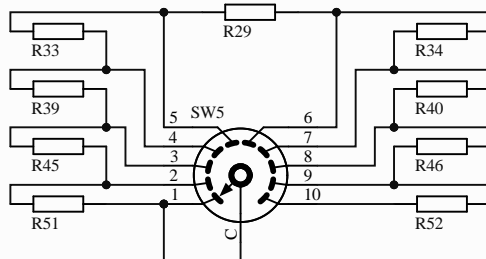
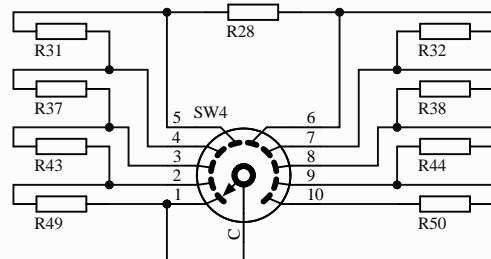
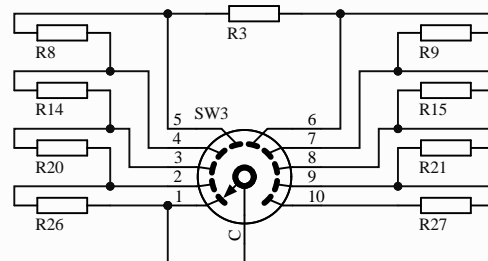
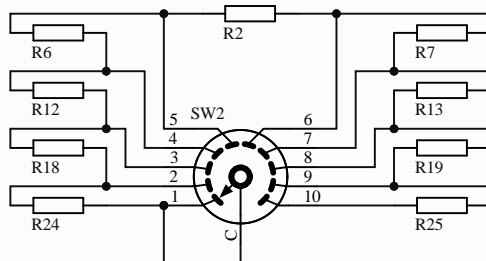
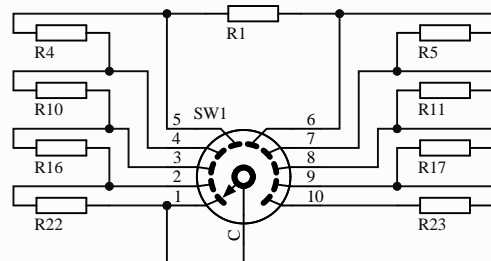
# ResistorDecadeBox.PrjPcb



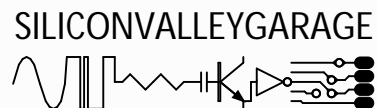
Document Creation Date: 7/15/2025

Design : Vincent Himpe

Fullyrouted



GitHub :  
<https://github.com/vincent-himpe/Resistor-DecadeBox>



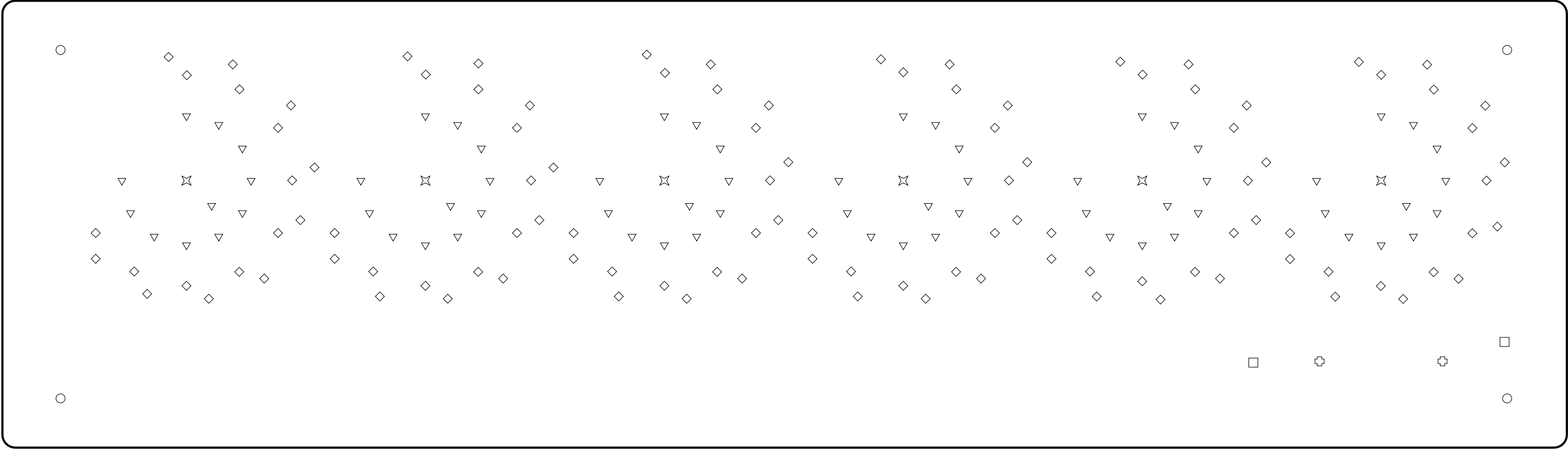
1	2	3	4	5	6
GENERAL					
A	<b>GENERAL</b>				
	1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA				
	2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.				
	3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER				
	4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2				
	5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED				
B	6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.				
	<b>MATERIALS</b>				
	7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.				
	8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER				
	9. SURFACE FINISH : HASL				
	10. SOLDER MASK COLOR : BLACK				
C	11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm				
	12. SILKSCREEN COLOR : WHITE				
	<b>STACKUP / IMPEDANCE CONTROL</b>				
	13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG				
	14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%				
	<b>QA, ELECTRICAL TEST AND MARKINGS</b>				
D	15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY				
			<div><div>Fullyrouted</div><div>Project ResistorDecadeBox.PrjPcb</div><div>Version:   Variant [No Variations]</div><div>FABRICATION DRAWING</div></div>		
1	2	3	4	5	6





DRILL DRAWING

Drill Drawing View (Scale 1.5:1)

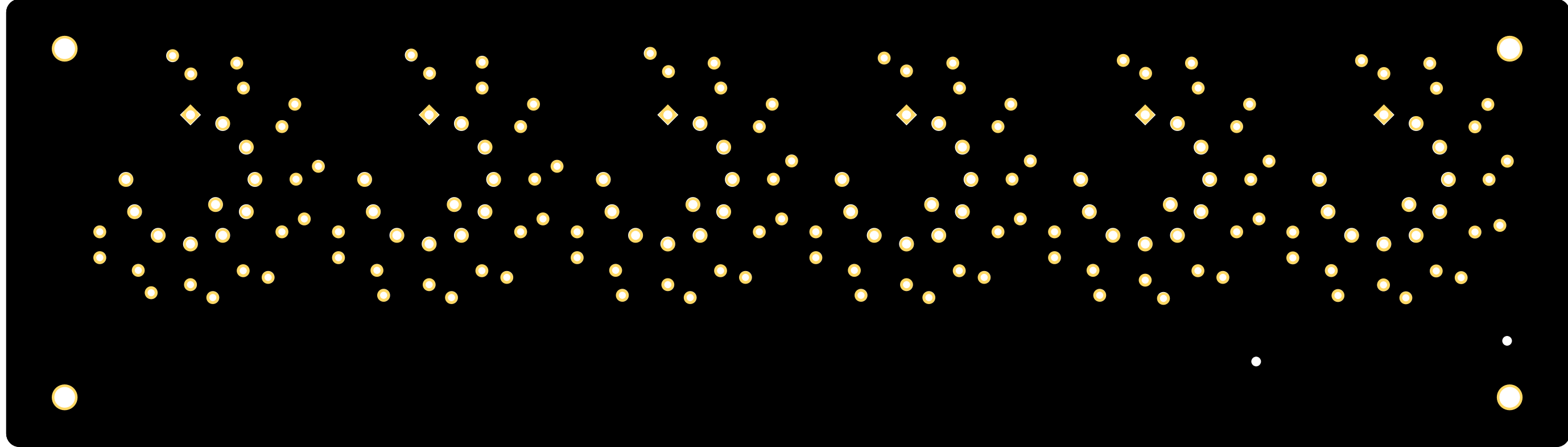


COMPOSITE VIEW FRONT

A

A

Top Layer (Scale 1.5:1)



B

B

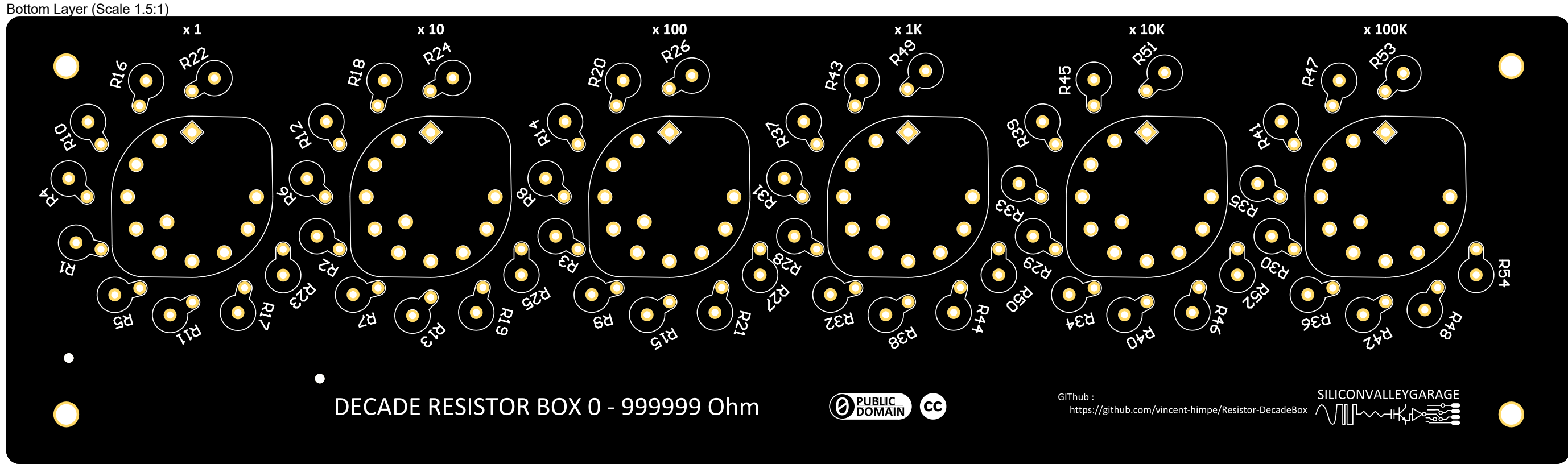
C

C

D

D

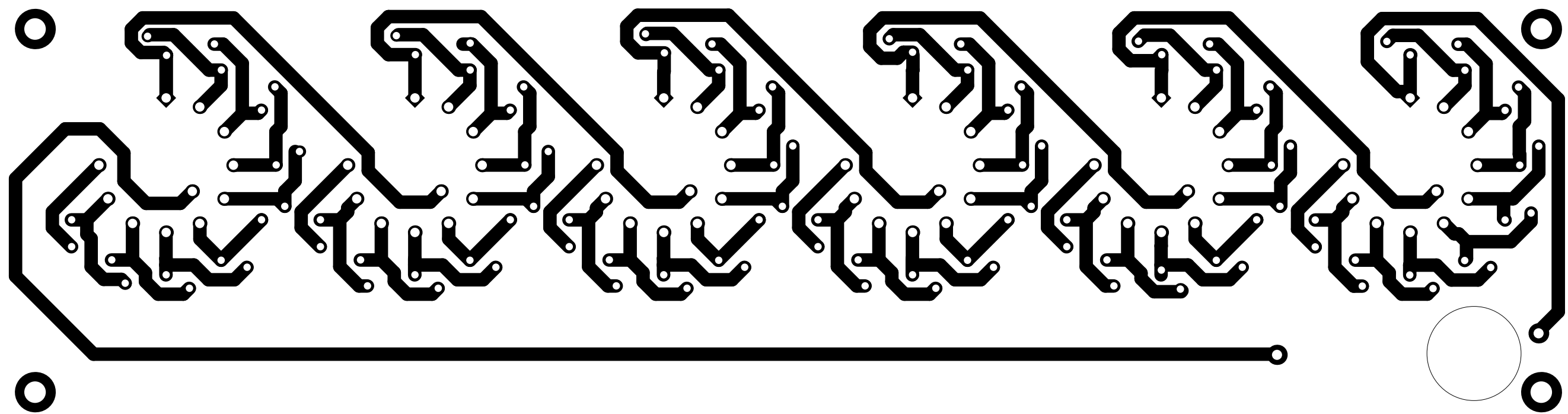
COMPOSITE VIEW BACK





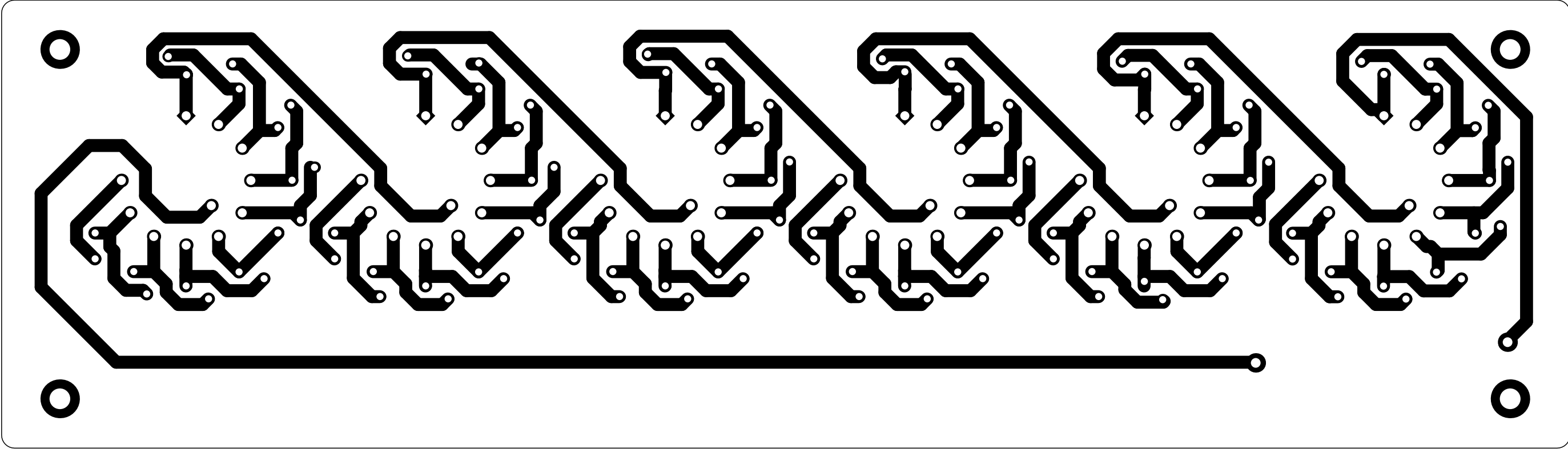
LAYER VIEW : TOP LAYER

Top Layer (Scale 1.5:1)



LAYER VIEW : BOTTOM LAYER

Bottom Layer (Scale 1.5:1)



Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP SOLDER MASK

A

A

B

B

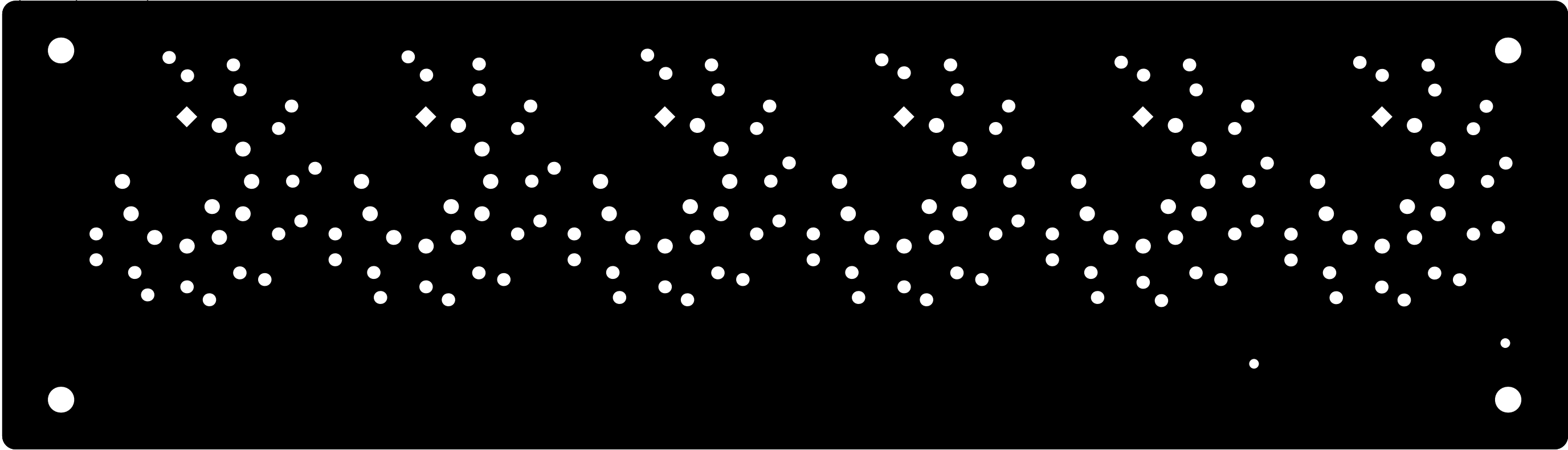
C

C

D

D

Top Solder (Scale 1.5:1)



LAYER VIEW : BOTTOM SOLDER MASK

A

A

B

B

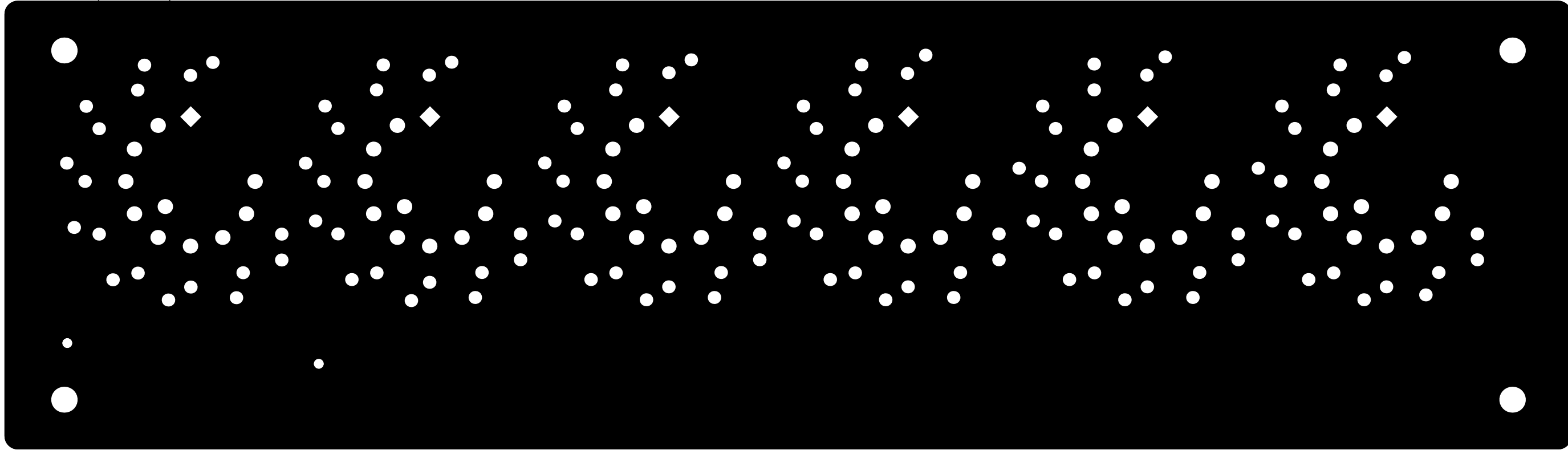
C

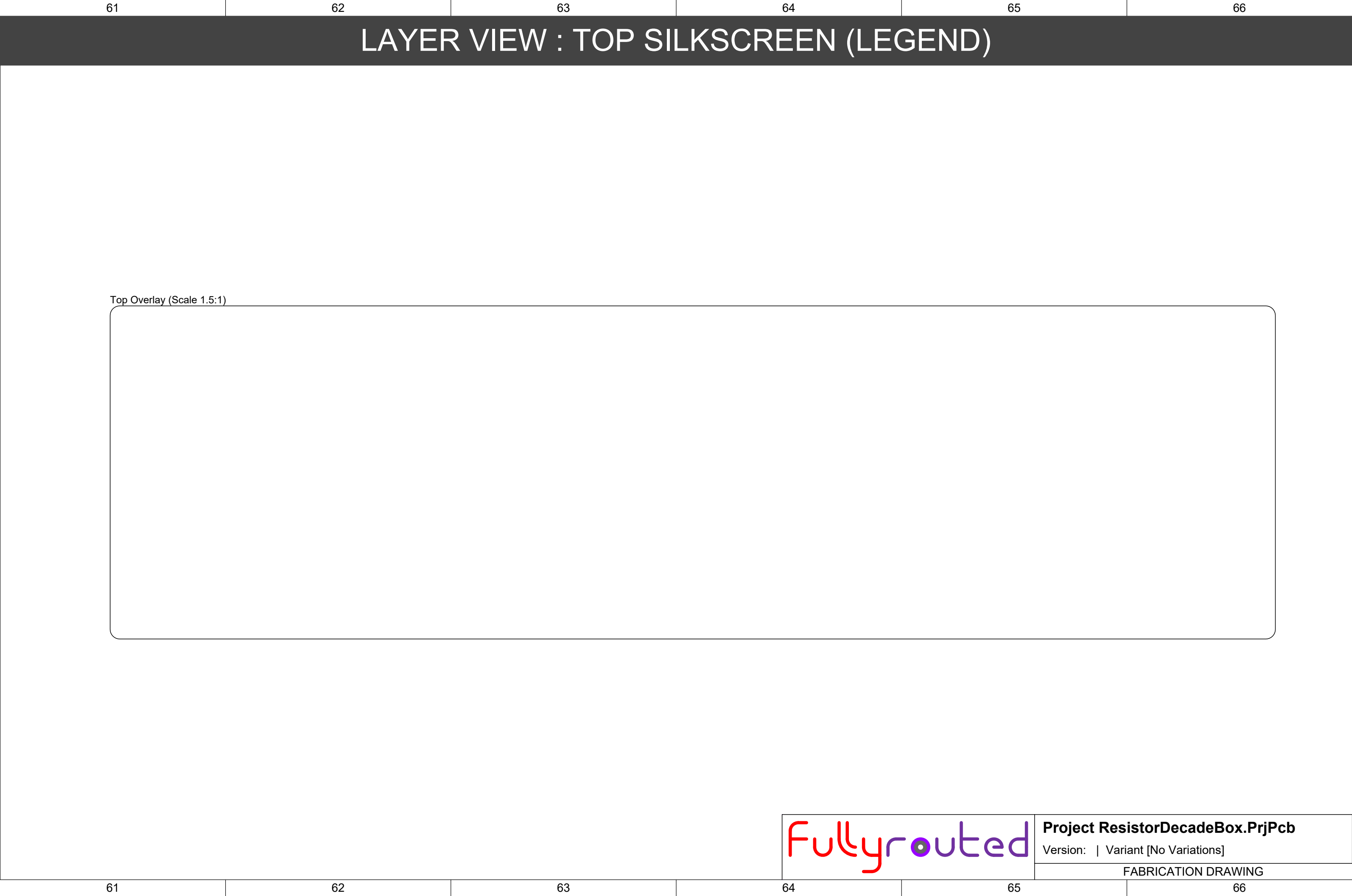
C

D

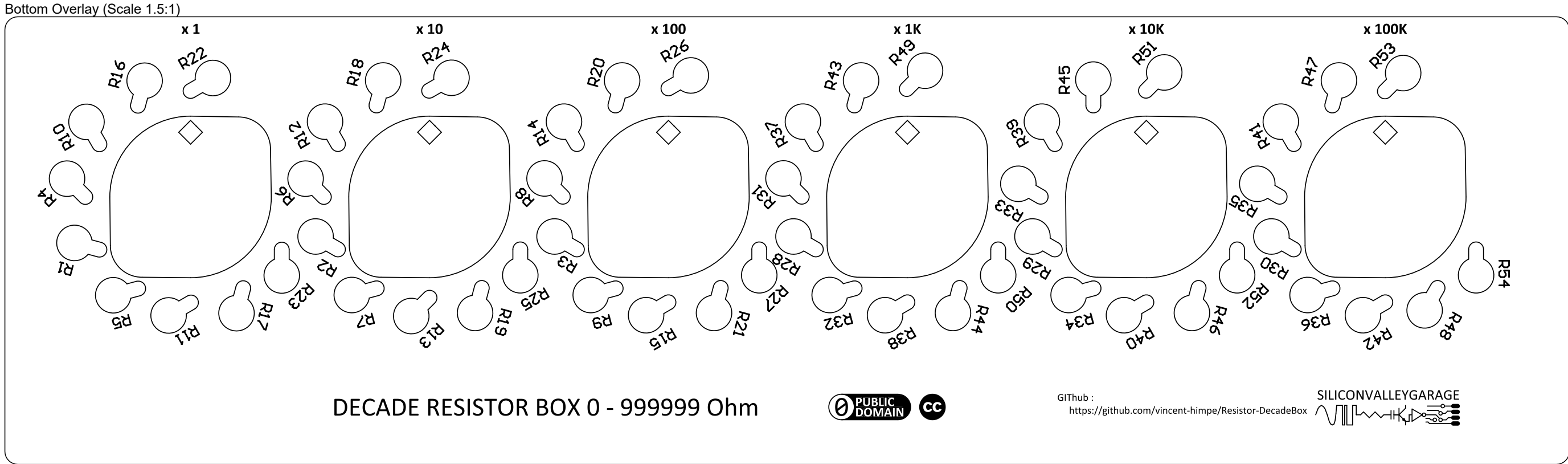
D

Bottom Solder (Scale 1.5:1)

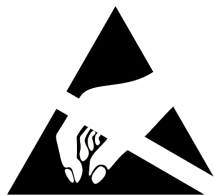




LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)



GENERAL



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- 2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

Bill of Materials and Material Handling

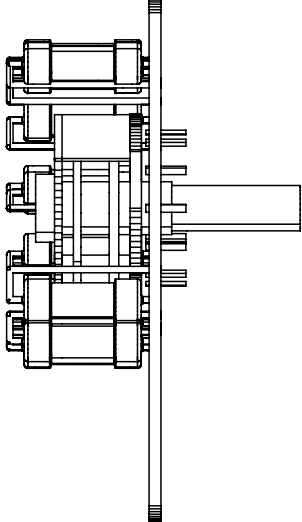
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- 7. ESD CONTROL PER IPC RULES

Soldering

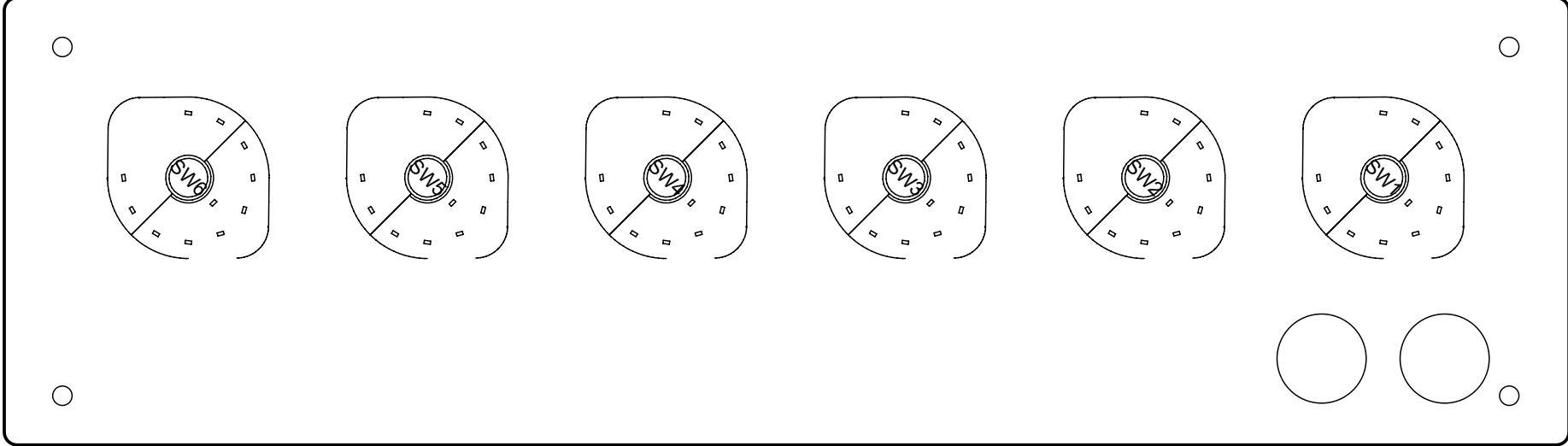
- 8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
- 9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
- 10. SOLDERING PREFERRABLY TO BE DONE USING NITROGEN ATMOSPHERE
- 11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
- 12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
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2D VIEW

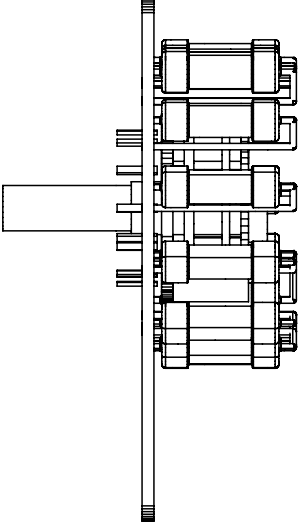
View from Left side (Scale 1:1)



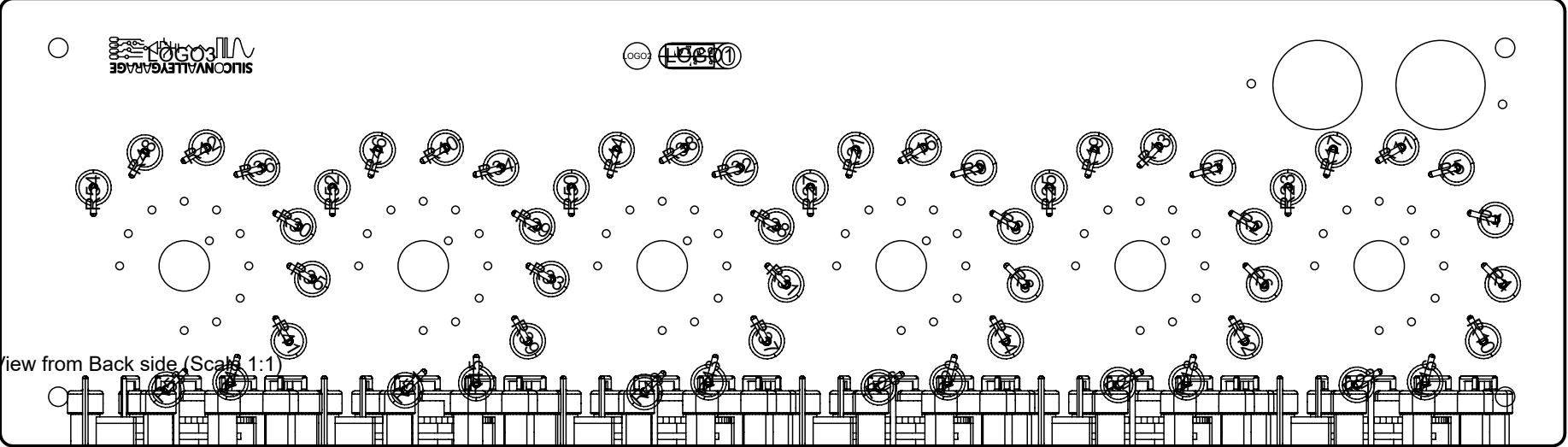
View from Top side (Scale 1:1)



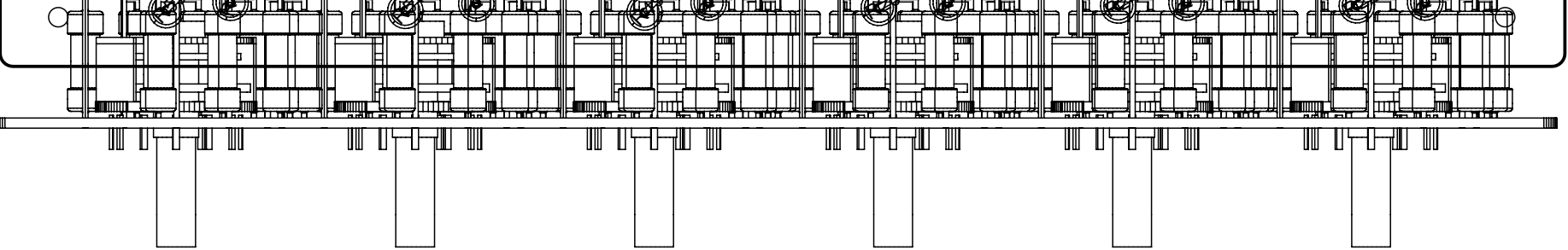
View from Right side (Scale 1:1)



View from Bottom side (Scale 1:1)

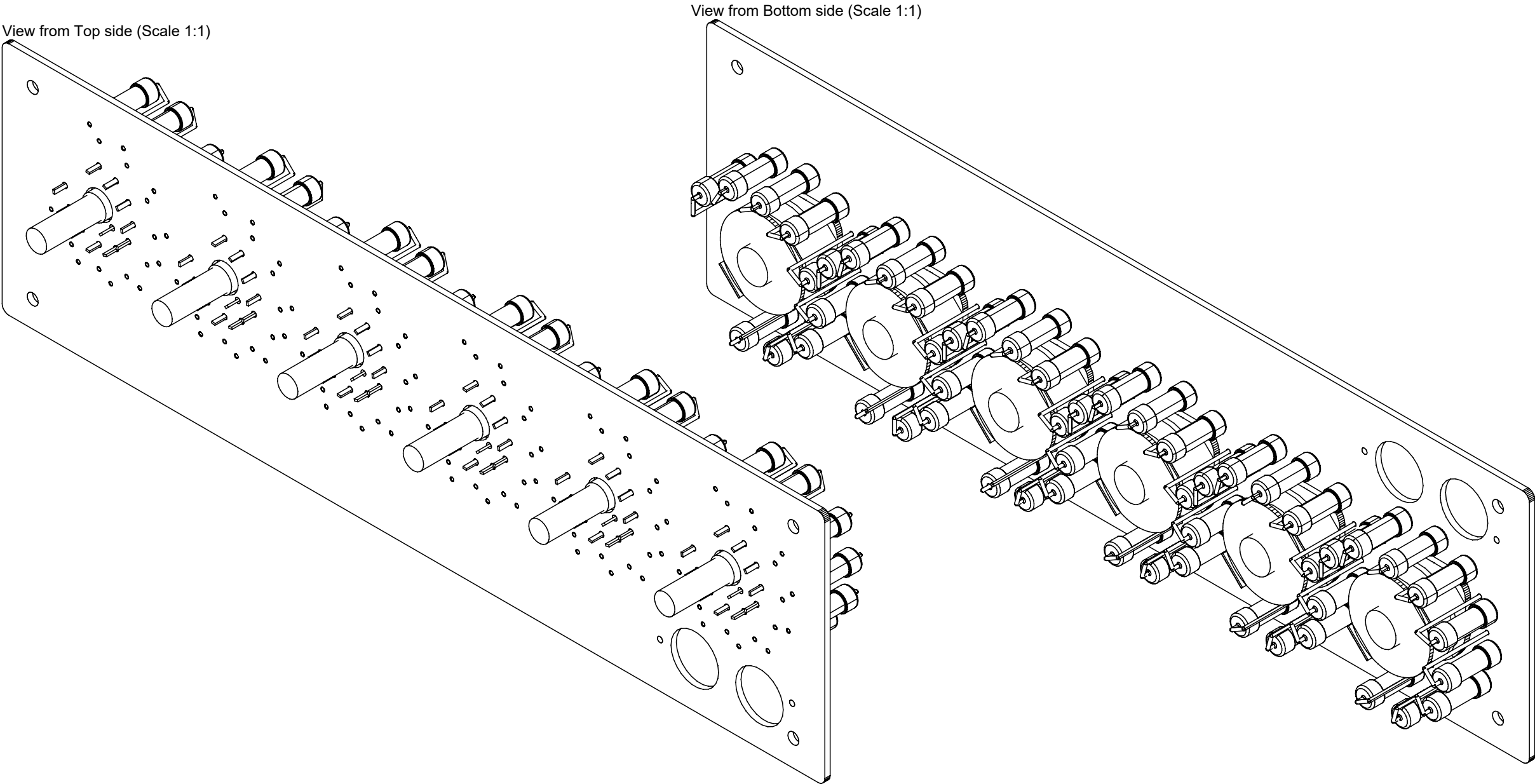


View from Back side (Scale 1:1)



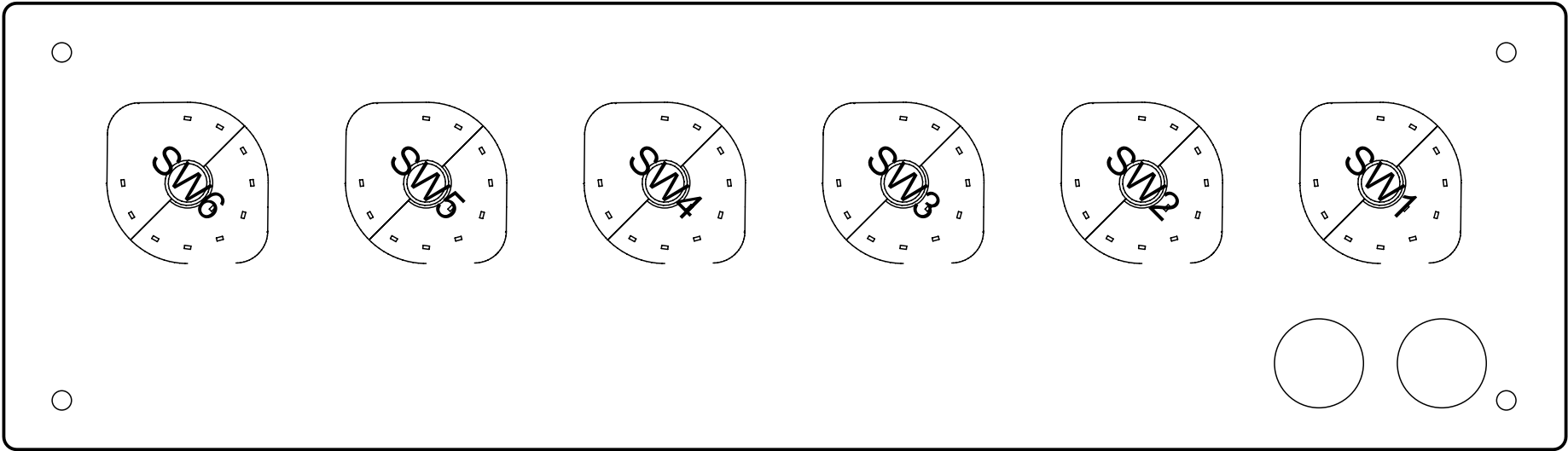


3D VIEW



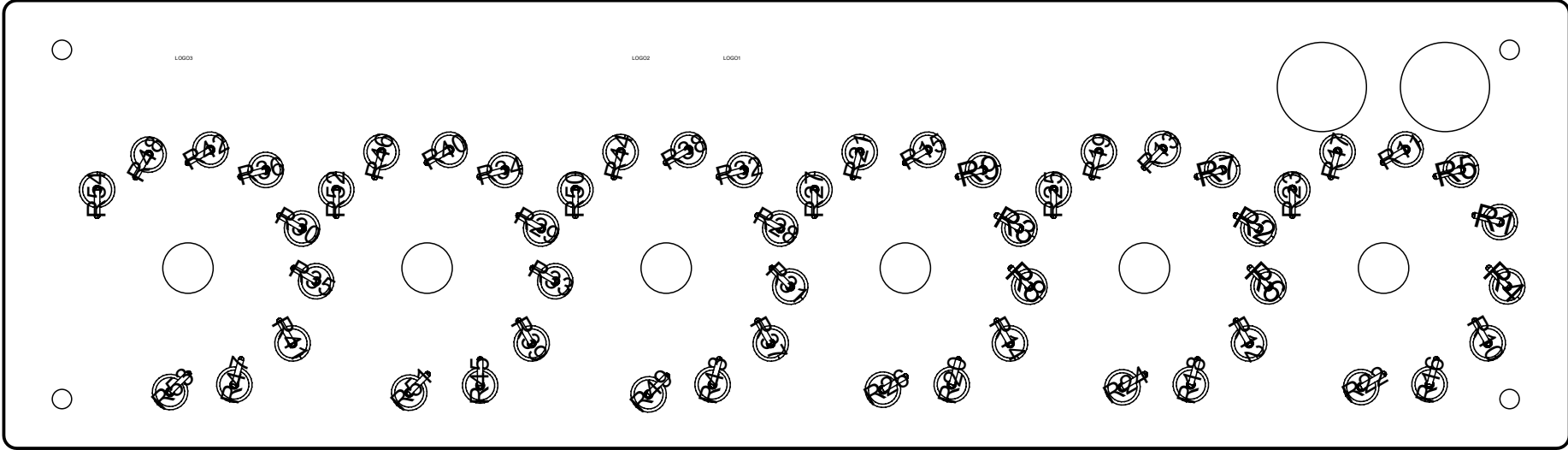


DESIGNATORS FRONT



View from Top side (Scale 1:1)

DESIGNATORS BACK



View from Bottom side (Scale 1:1)

1	2	3	4	5	6
GENERAL					
A	<b>GENERAL</b>				
	1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA				
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	<b>MATERIALS</b>				
	7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.				
	8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER				
	9. SURFACE FINISH : HASL				
	10. SOLDER MASK COLOR : BLACK				
C	11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm				
	12. SILKSCREEN COLOR : WHITE				
	<b>STACKUP / IMPEDANCE CONTROL</b>				
	13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG				
	14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%				
	<b>QA, ELECTRICAL TEST AND MARKINGS</b>				
D	15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY				
			<div><div>Fullyrouted</div><div>Project ResistorDecadeBox.PrjPcb</div><div>Version:   Variant [No Variations]</div><div>FABRICATION DRAWING</div></div>		
1	2	3	4	5	6









# DRILL DRAWING

A

A

B

B

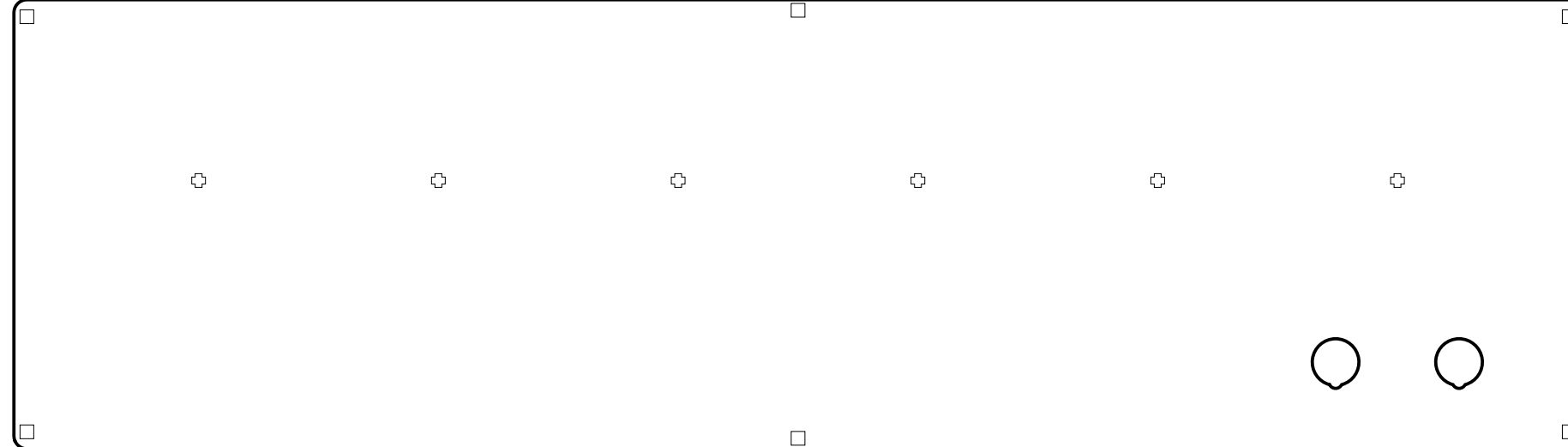
C

C

D

D

### Drill Drawing View (Scale 1:1)



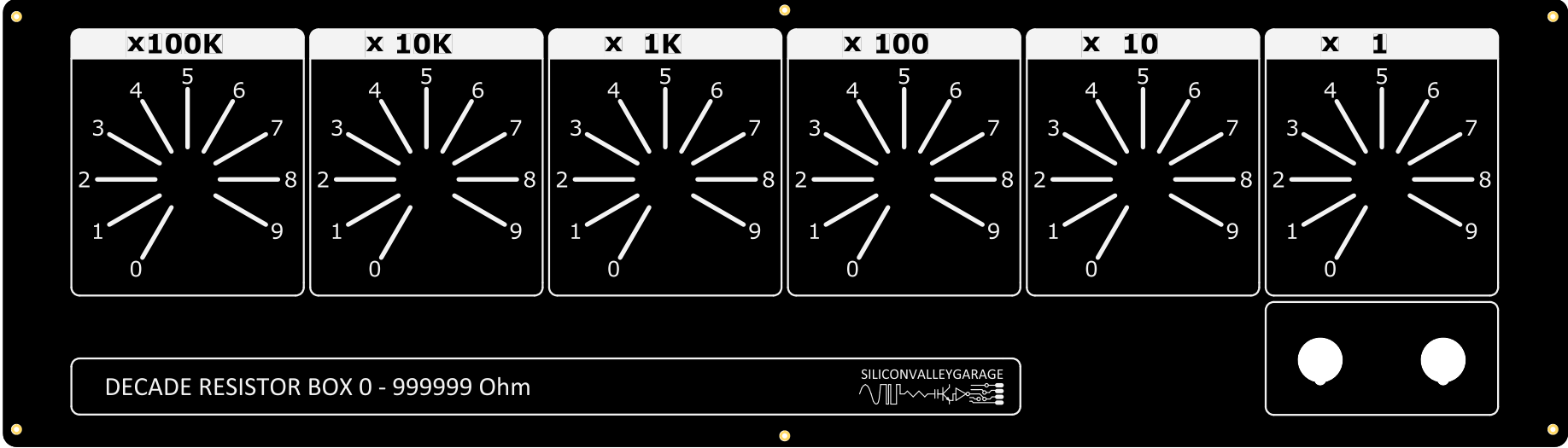
Project ResistorDecadeBox.PrjPcb

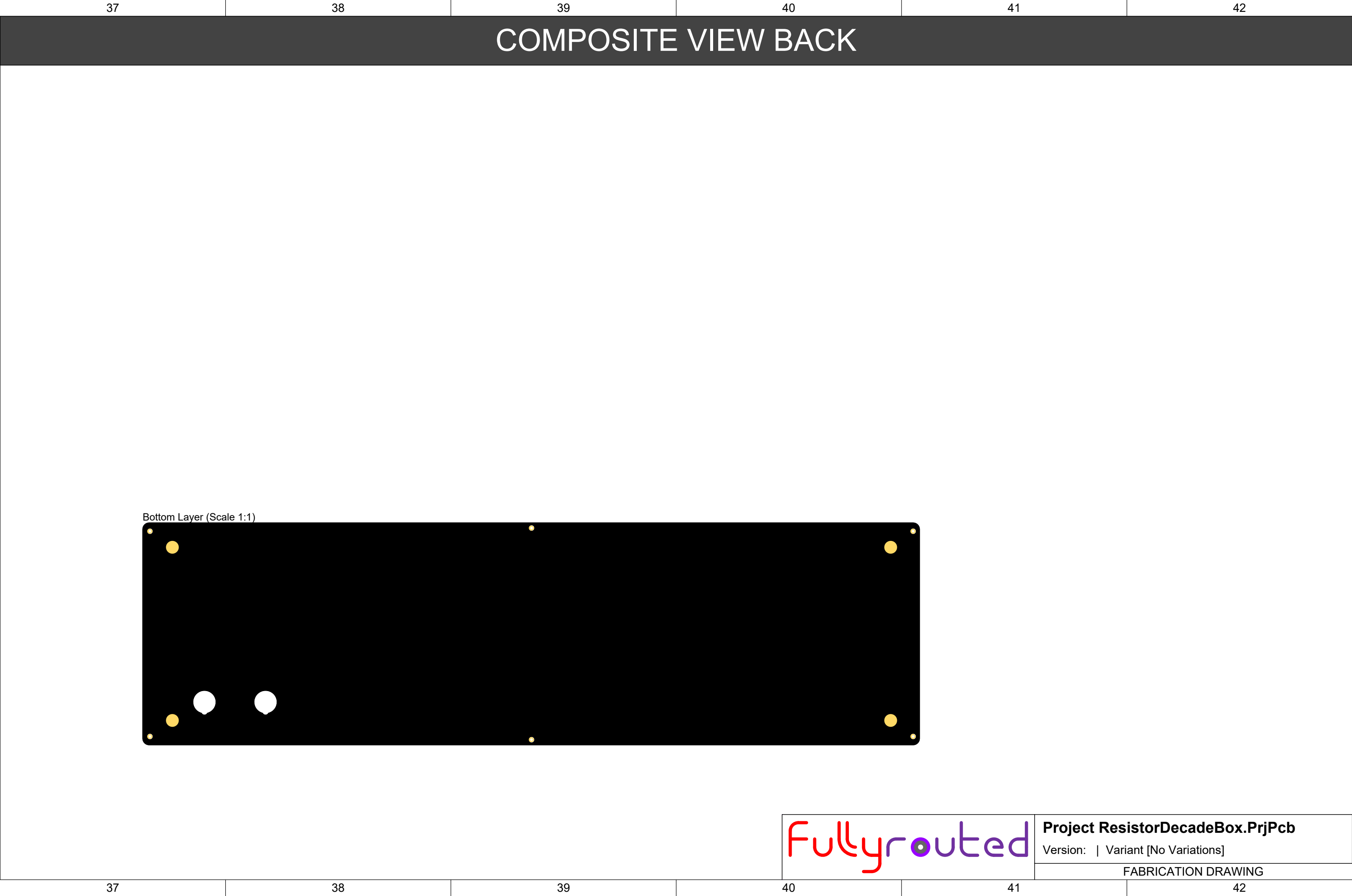
Version:	Variant [No Variations]
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### FABRICATION DRAWING

COMPOSITE VIEW FRONT

Top Layer (Scale 1:1)





LAYER VIEW : TOP LAYER

A

A

B

B

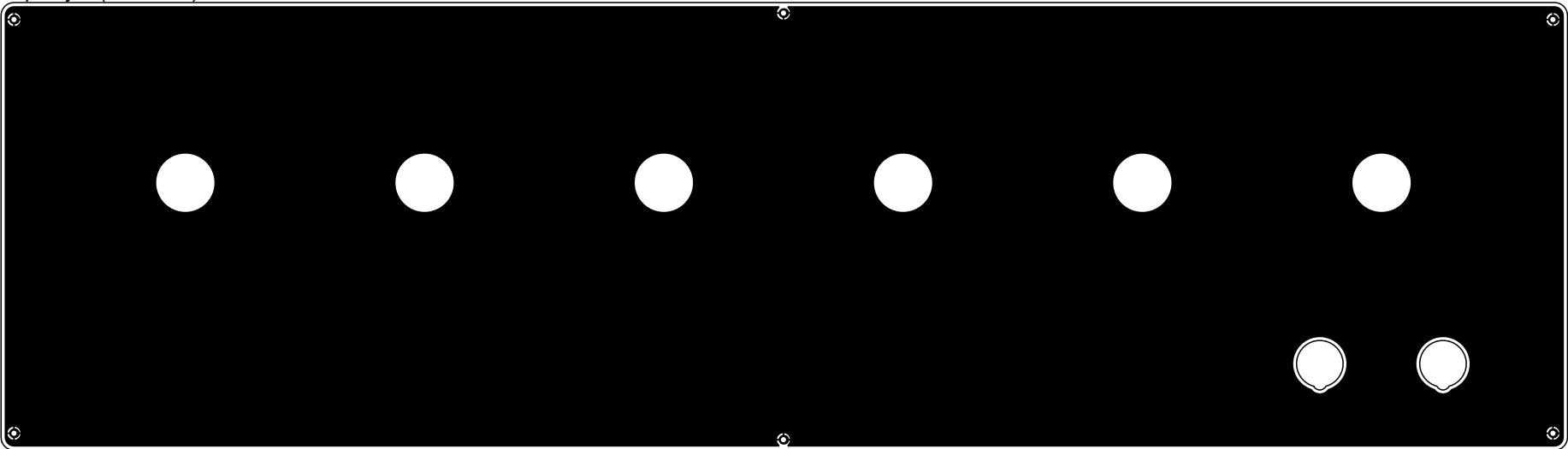
C

C

D

D

Top Layer (Scale 1:1)



Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

# LAYER VIEW : BOTTOM LAYER

A

A

B

B

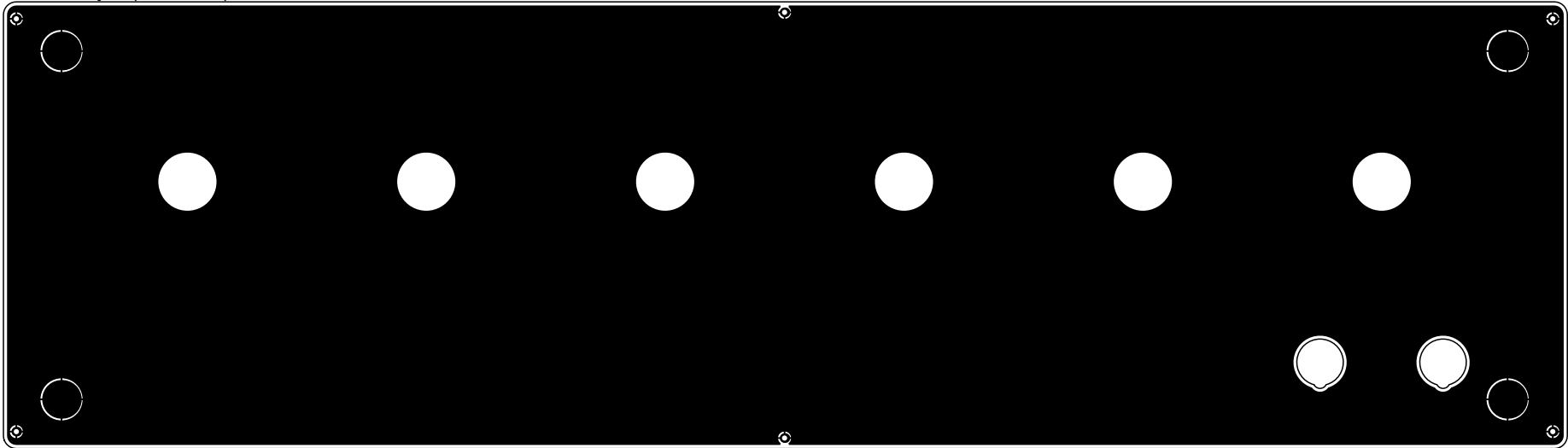
C

C

D

D

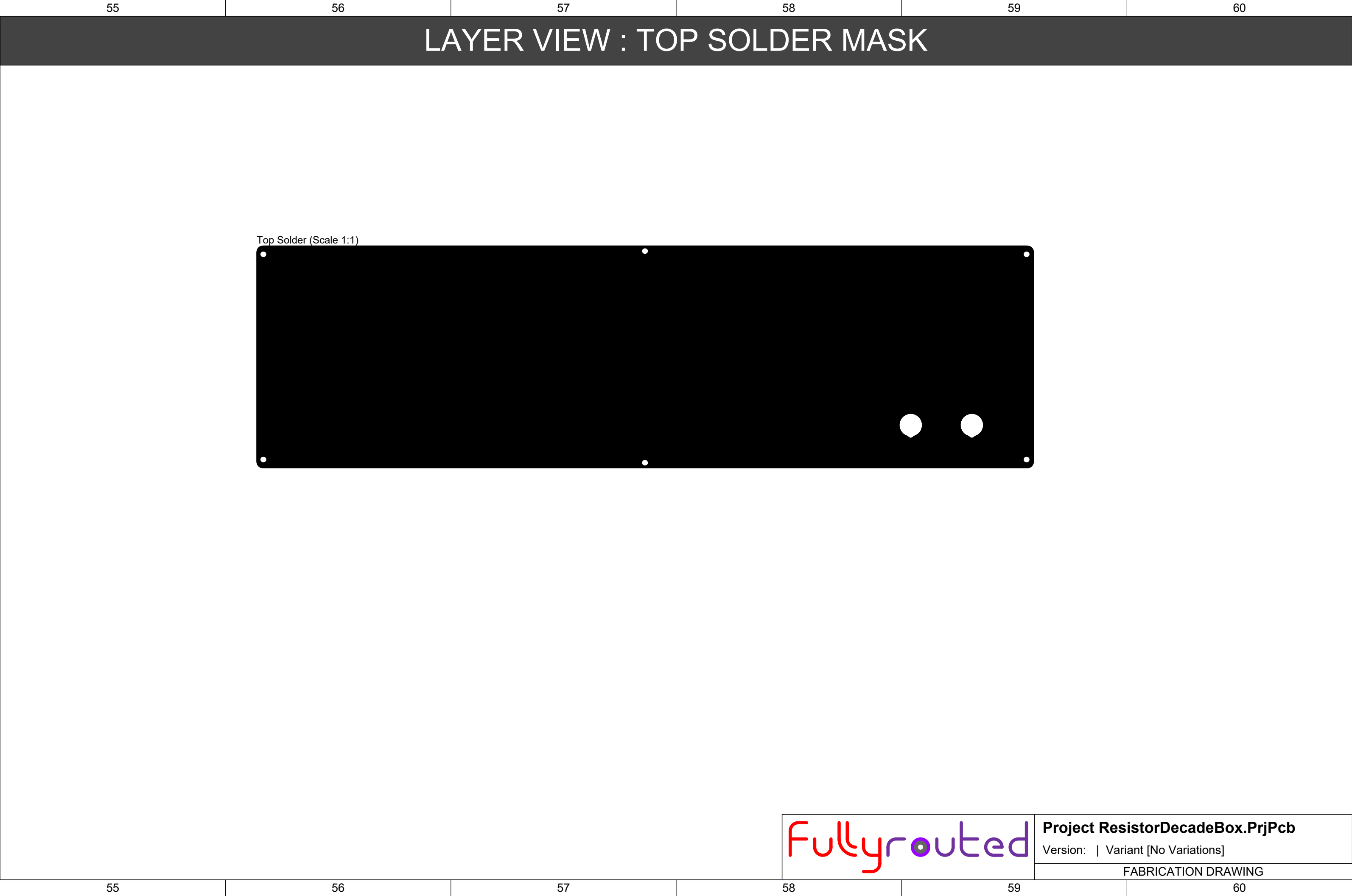
Bottom Layer (Scale 1:1)

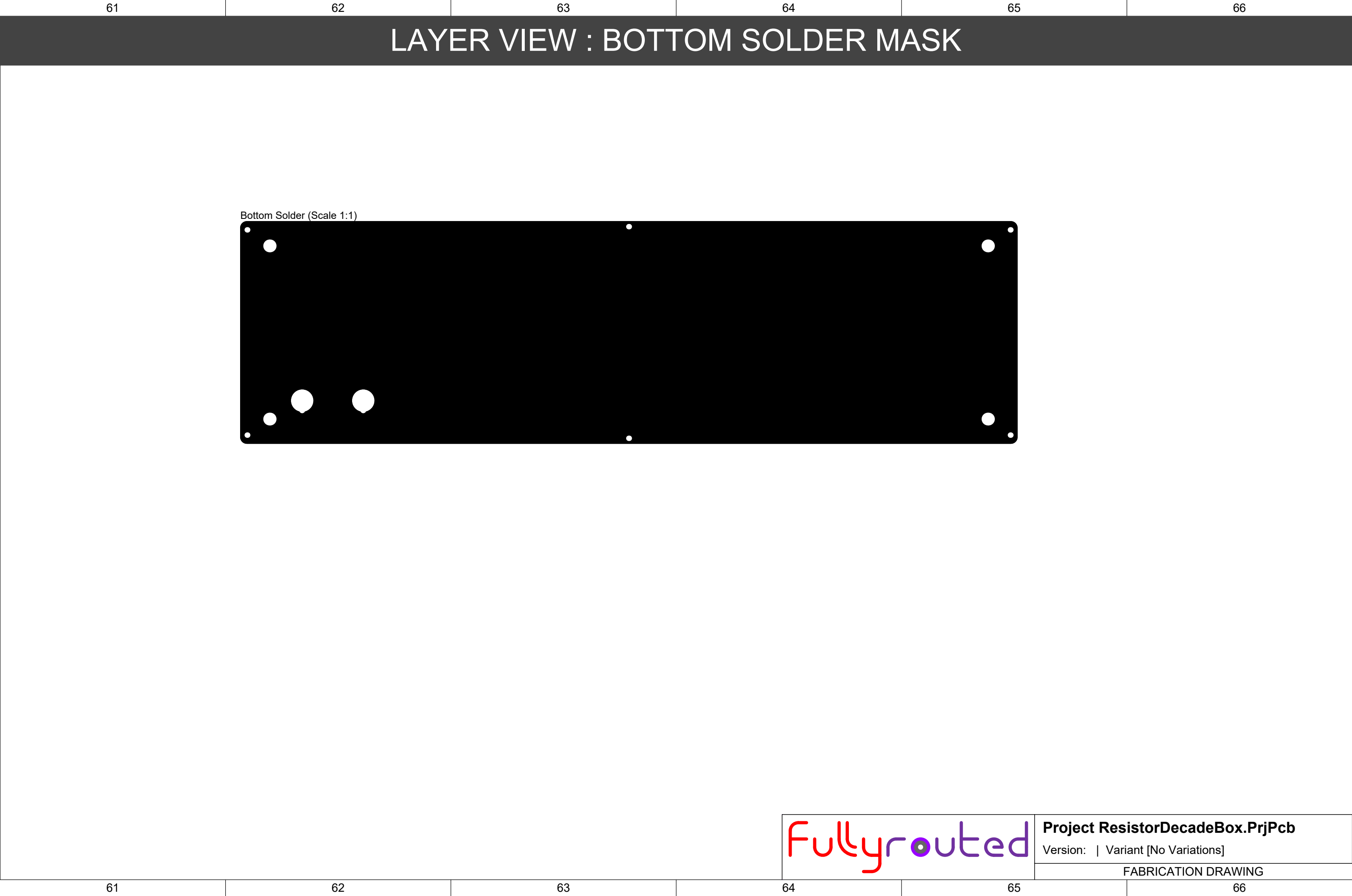


Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING





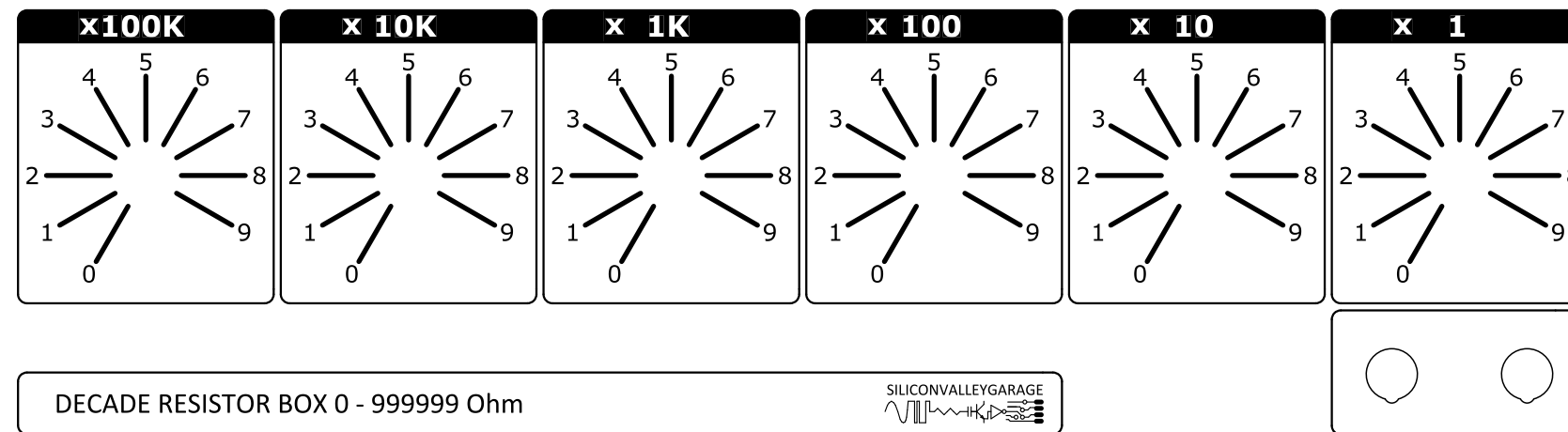
Project ResistorDecadeBox.PrjPcb

Version: | Variant [No Variations]

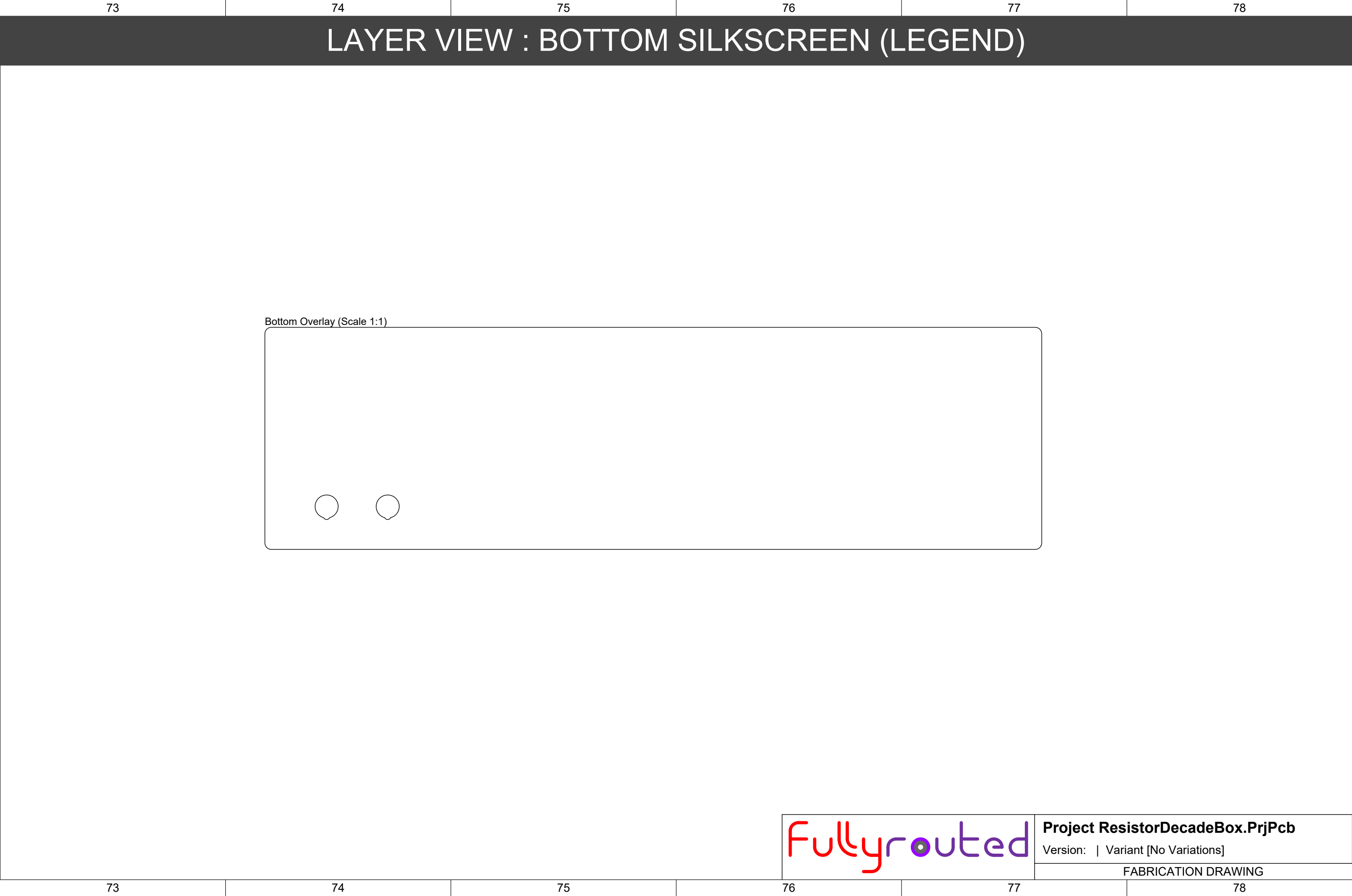
FABRICATION DRAWING

## LAYER VIEW : TOP SILKSCREEN (LEGEND)

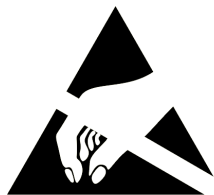
Top Overlay (Scale 1:1)







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Soldering

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3D VIEW

