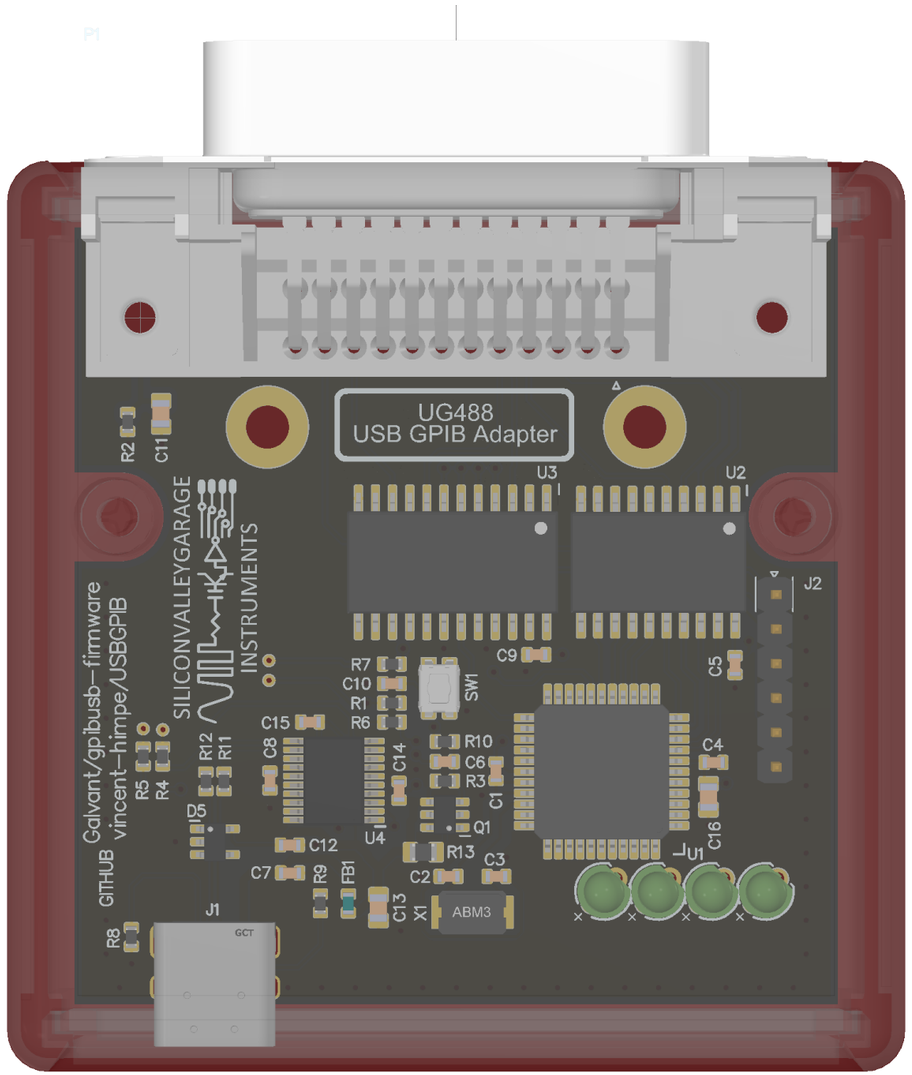
USB-GPIB.PrjPcb



Document Creation Date: 9/25/2025

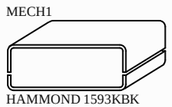
Design : Vincent Himpe

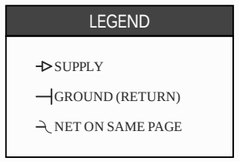
SILICONVALLEYGARAGE

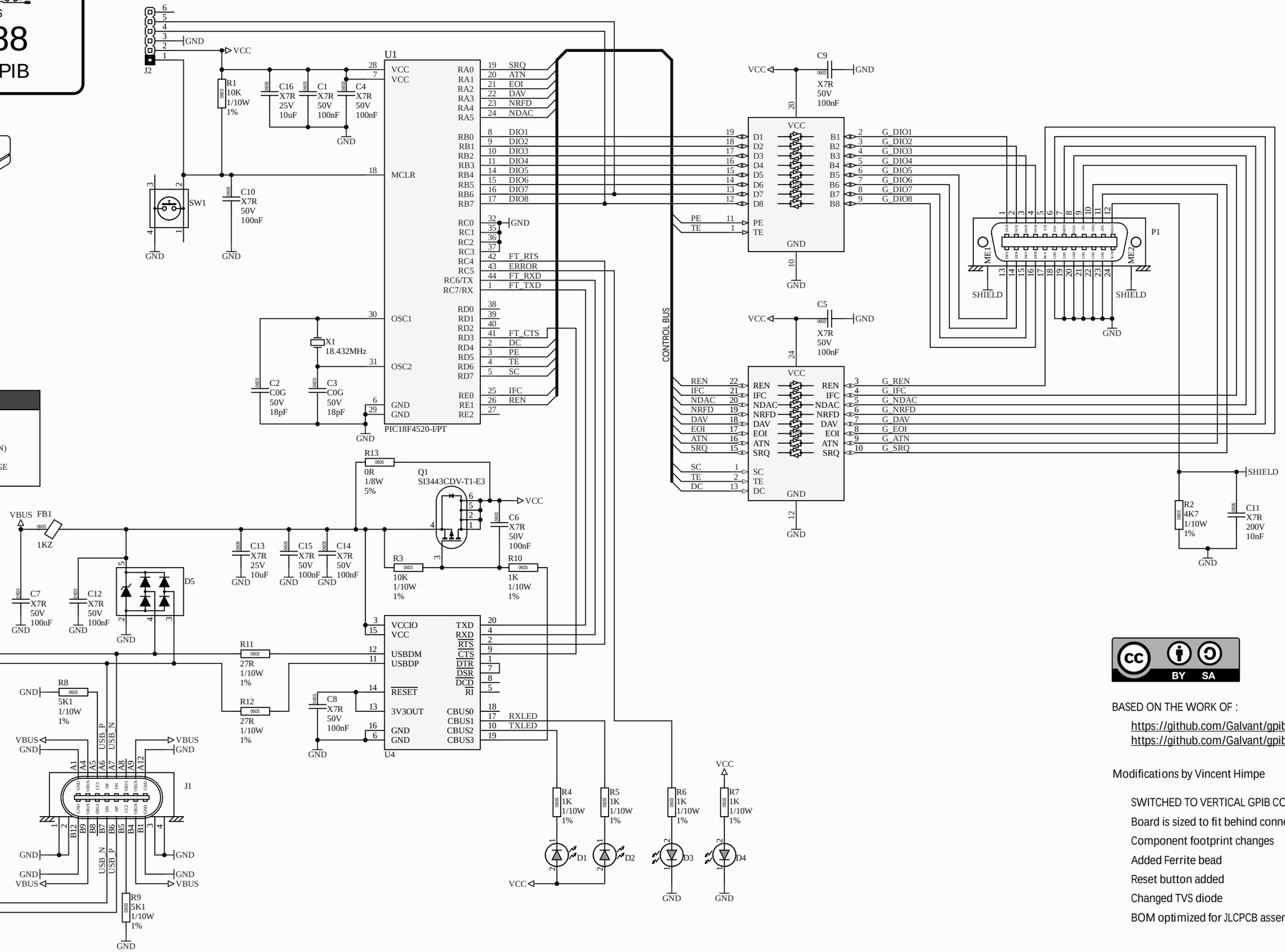
SILICONVALLEYGARAGE Instruments

UG488

USB< > GPIB







BASED ON THE WORK OF :

https://github.com/Galvant/gpibusb-pcb
https://github.com/Galvant/gpibusb-firmware

Modifications by Vincent Himpe

- SWITCHED TO VERTICAL GPIB CONNECTOR
- Board is sized to fit behind connector
- Component footprint changes
- Added Ferrite bead
- Reset button added
- Changed TVS diode
- BOM optimized for JLCPCB assembly service (LCSC parts)

GENERAL

GENERAL

1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA
2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.
3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER
4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2
5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED
6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.

MATERIALS

7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.
8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER
9. SURFACE FINISH : HASL
10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%

QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY

SILICONVALLEYGARAGE

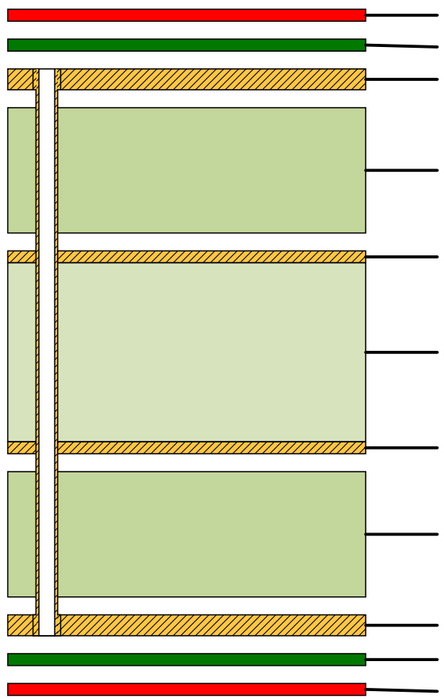
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER STACK

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber	Dk	Weight	Constructions	Df	Resin
	Top Overlay			Legend	GTO					
Surface Material	Top Solder	0.010mm(0.394mil)	Solder Resist	Solder Mask	GTS	3.5				
Copper	**Top Layer**	**0.035mm(1.378mil)**		**Signal**	**GTL**		**1oz**			
Prepreg		*0.210mm(8.268mil)*	*7628 X 1*	*Dielectric*		*4.1*		*1080*	*0.02*	*62%*
CF-004	**Layer 1**	**0.015mm(0.591mil)**		**Signal**	**G1**		**0.5oz**			
Core		*1.065mm(41.929mil)*	*FR-4*	*Dielectric*		*4.8*				
CF-004	**Layer 2**	**0.015mm(0.591mil)**		**Signal**	**G2**		**0.5oz**			
Prepreg		*0.210mm(8.268mil)*	*7628 X 1*	*Dielectric*		*4.1*		*1080*	*0.02*	*62%*
Copper	**Bottom Layer**	**0.035mm(1.378mil)**		**Signal**	**GBL**		**1oz**			
Surface Material	Board Layer Stack Bottom Solder	0.010mm(0.394mil)	Solder Resist	Solder Mask	GBS	3.5				
	Board Layer Stack Bottom Overlay			Legend	GBO					

Total thickness: 1.605mm(63.189mil)

SILICONVALLEYGARAGE

Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

CONTROLLED IMPEDANCE

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Substack	Clearance	Target Tolerance

SILICONVALLEYGARAGE

Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description Hole Tolerance	Via Type	Via Feature
⛝	147	0.400mm(15.748mil)	Plated	Round	Top Layer - Bottom Layer	(Mixed)	(Mixed)		(Mixed)	(Mixed)
○	32	1.000mm(39.370mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded			
⯐	6	1.100mm(43.307mil)	Plated	Round	Top Layer - Bottom Layer	Pad	(Mixed)			
▽	2	1.400mm(55.118mil)	Plated	Slot	Top Layer - Bottom Layer	Pad	Rounded Rectangular			
⛝	2	2.100mm(82.677mil)	Plated	Slot	Top Layer - Bottom Layer	Pad	Rounded Rectangular			
◇	2	3.200mm(125.984mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded			
□	2	3.200mm(125.984mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded			
	193 Total									

SILICONVALLEYGARAGE

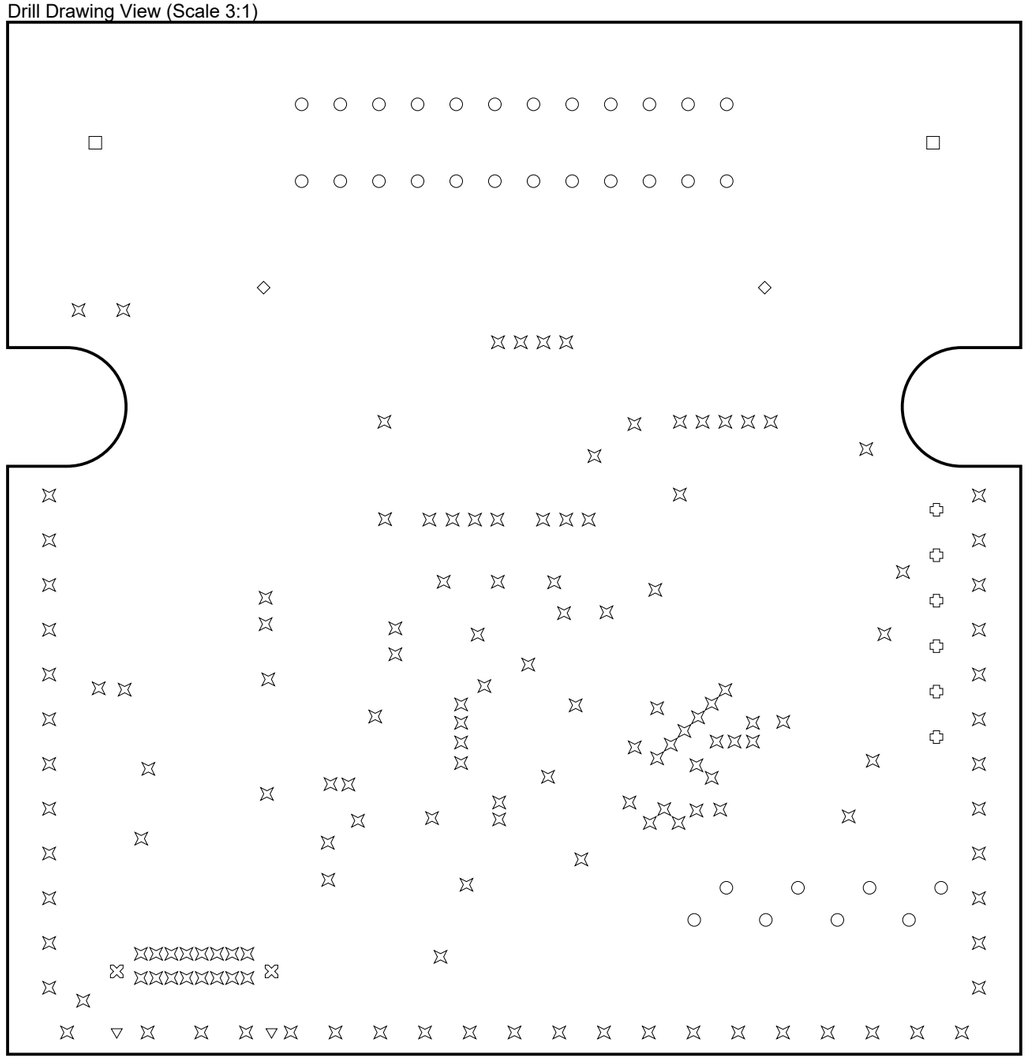
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

DRILL DRAWING

Drill Drawing View (Scale 3:1)



SILICONVALLEYGARAGE

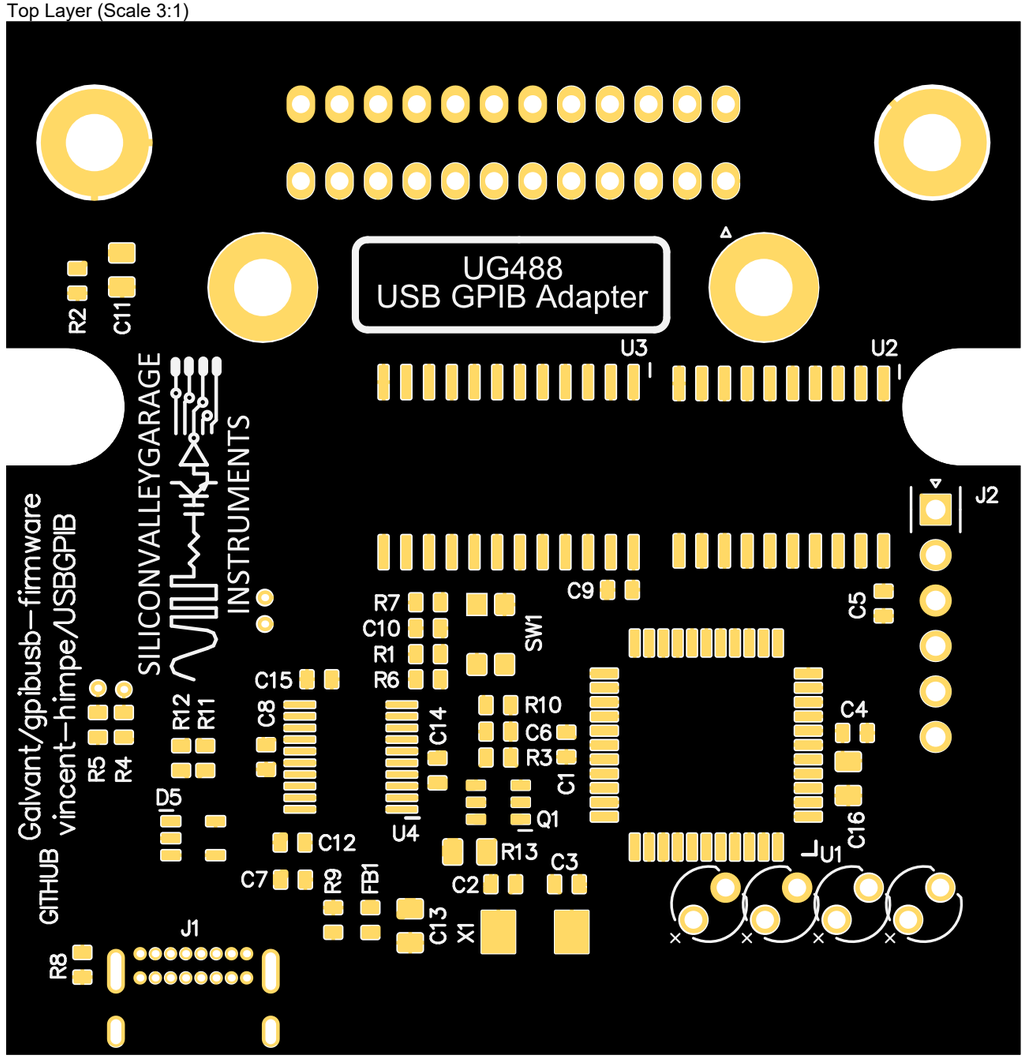
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

COMPOSITE VIEW FRONT

Top Layer (Scale 3:1)



SILICONVALLEYGARAGE

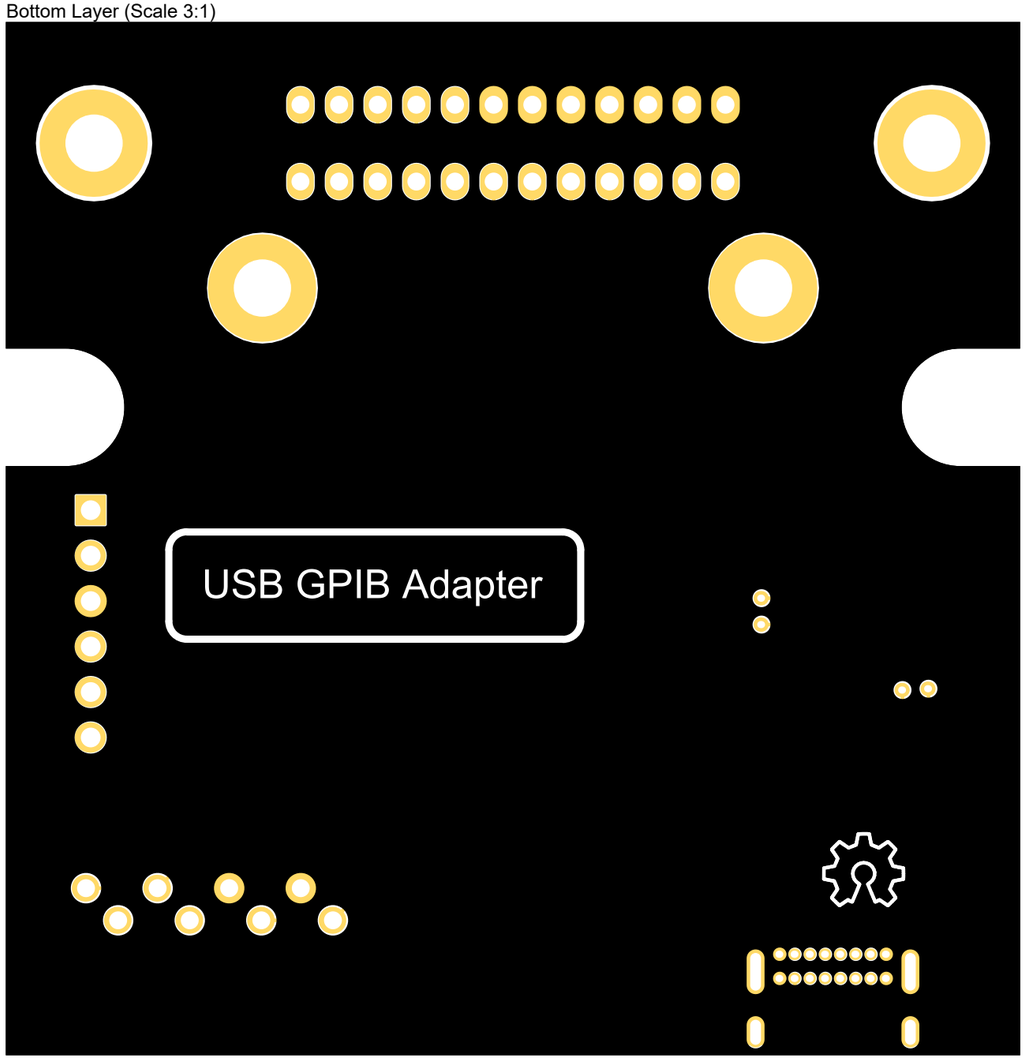
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

COMPOSITE VIEW BACK

Bottom Layer (Scale 3:1)



SILICONVALLEYGARAGE

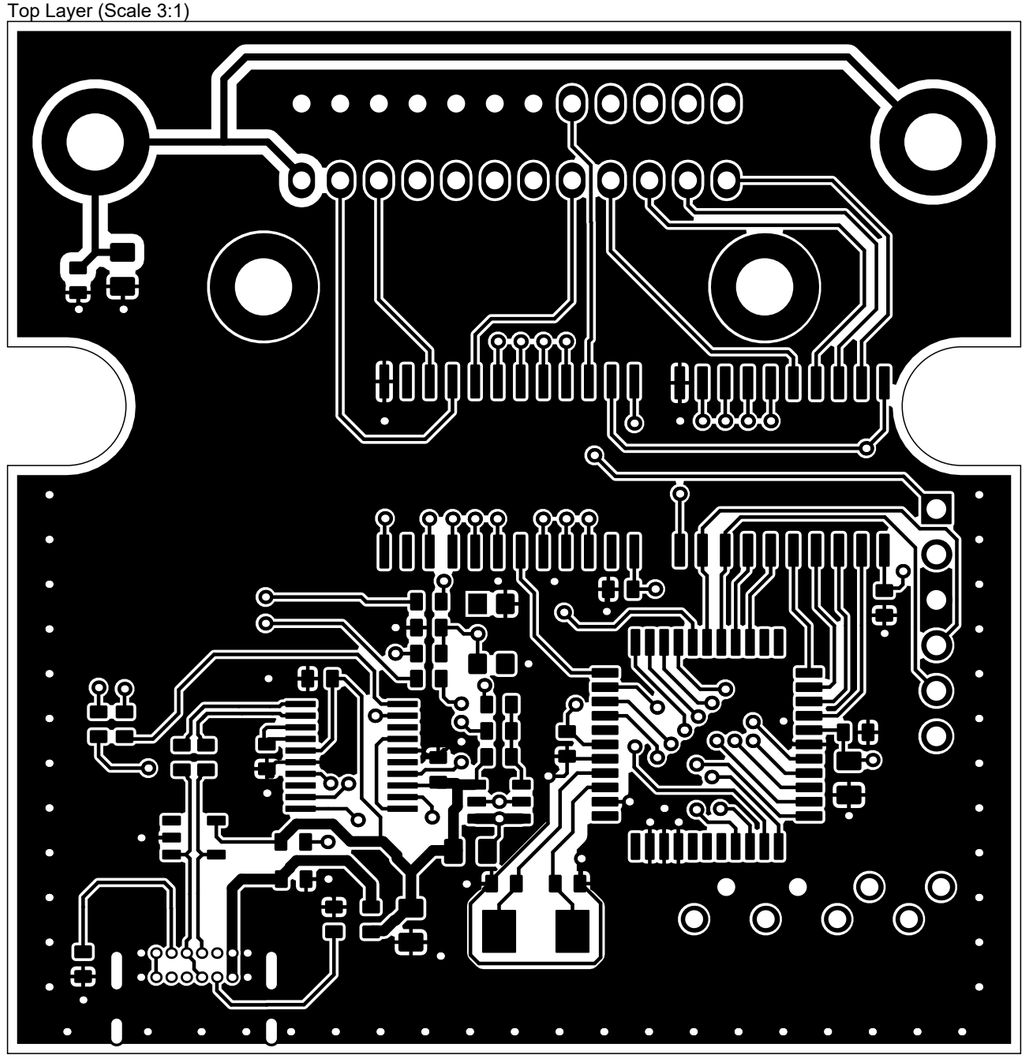
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP LAYER

Top Layer (Scale 3:1)



SILICONVALLEYGARAGE

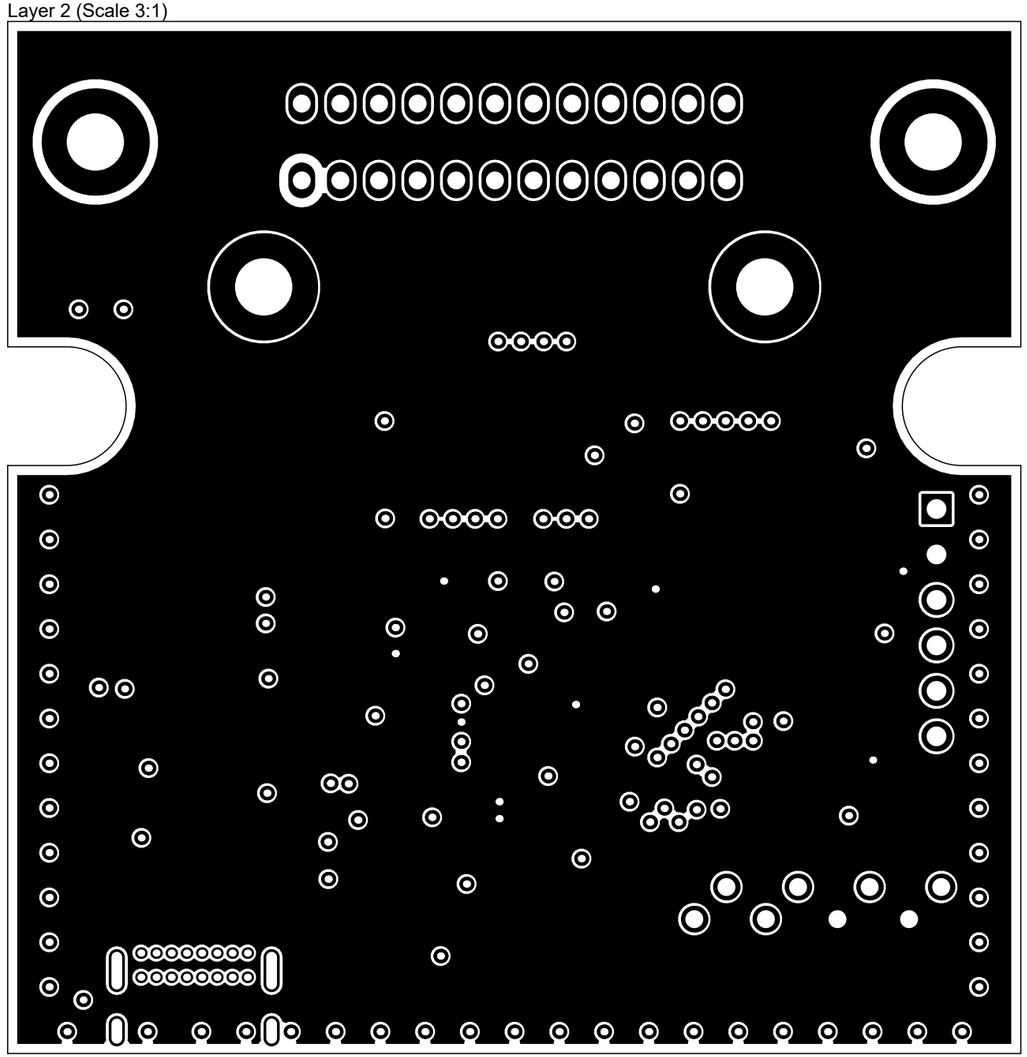
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : MID LAYER 1

Layer 2 (Scale 3:1)



SILICONVALLEYGARAGE

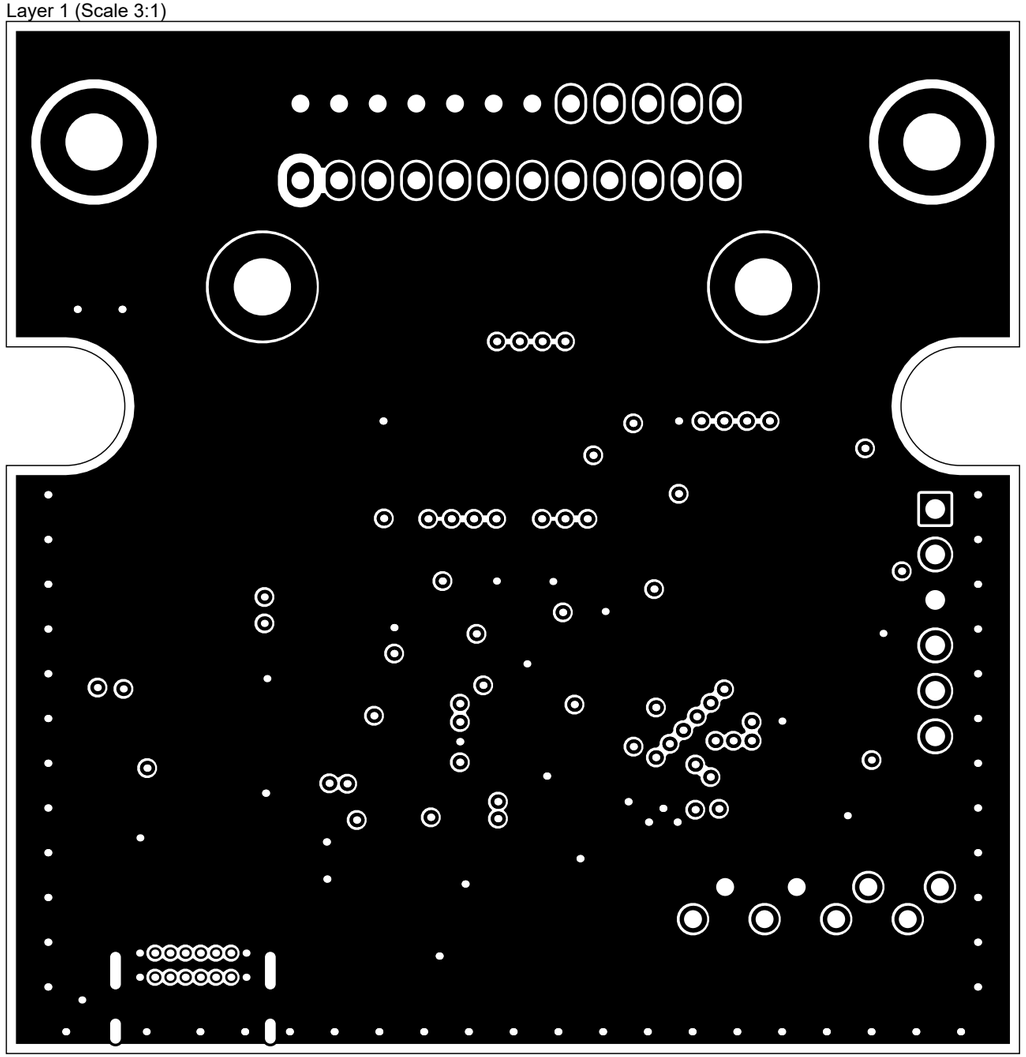
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : MID LAYER 2

Layer 1 (Scale 3:1)



SILICONVALLEYGARAGE

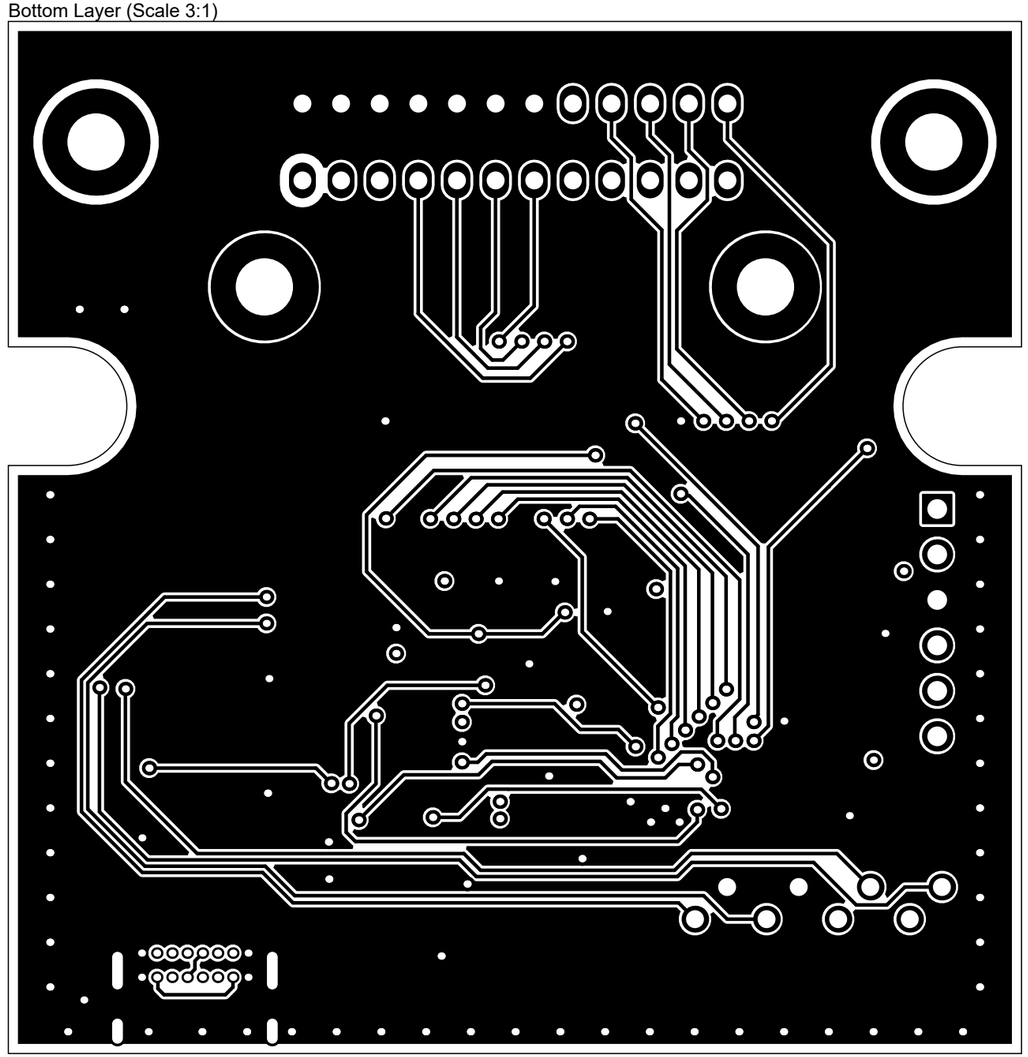
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM LAYER

Bottom Layer (Scale 3:1)



SILICONVALLEYGARAGE

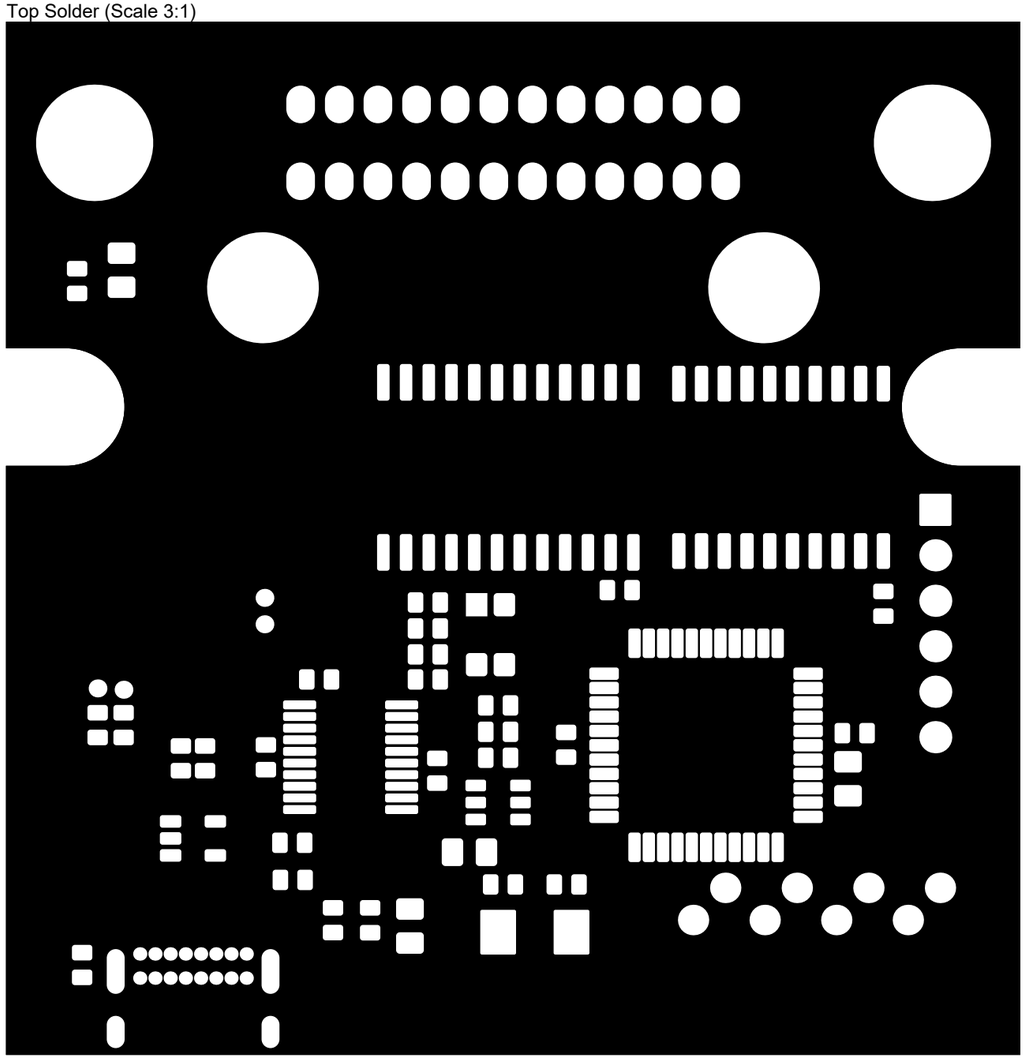
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP SOLDER MASK

Top Solder (Scale 3:1)



SILICONVALLEYGARAGE

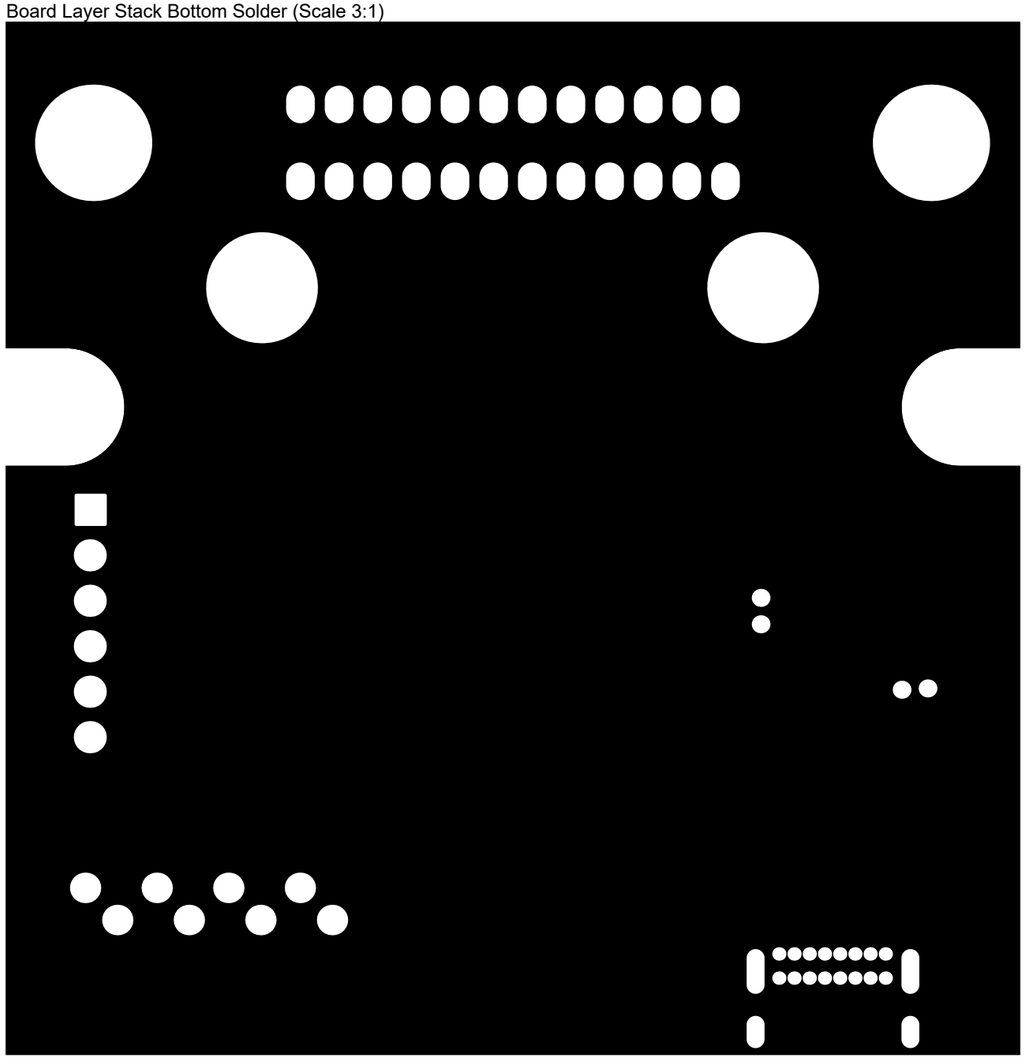
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SOLDER MASK

Board Layer Stack Bottom Solder (Scale 3:1)



SILICONVALLEYGARAGE

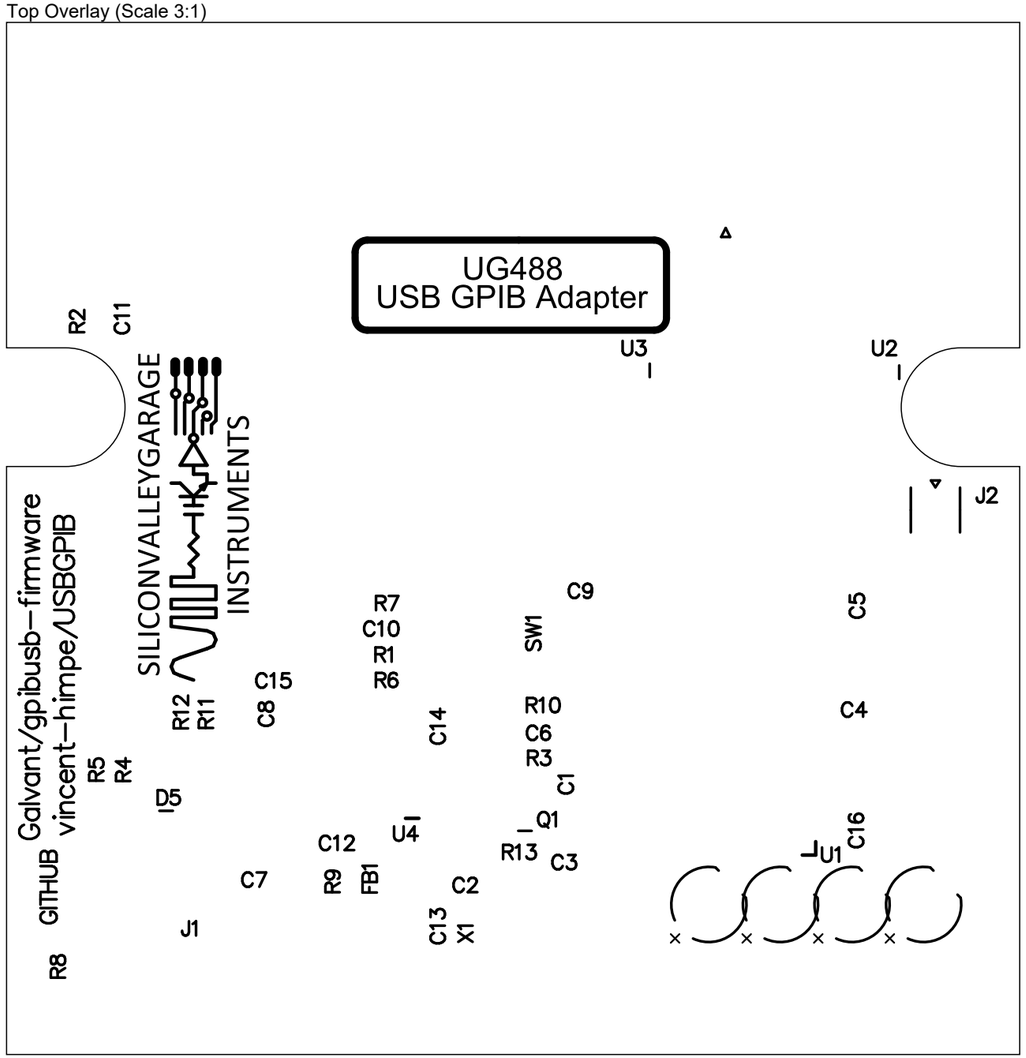
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP SILKSCREEN (LEGEND)

Top Overlay (Scale 3:1)



SILICONVALLEYGARAGE

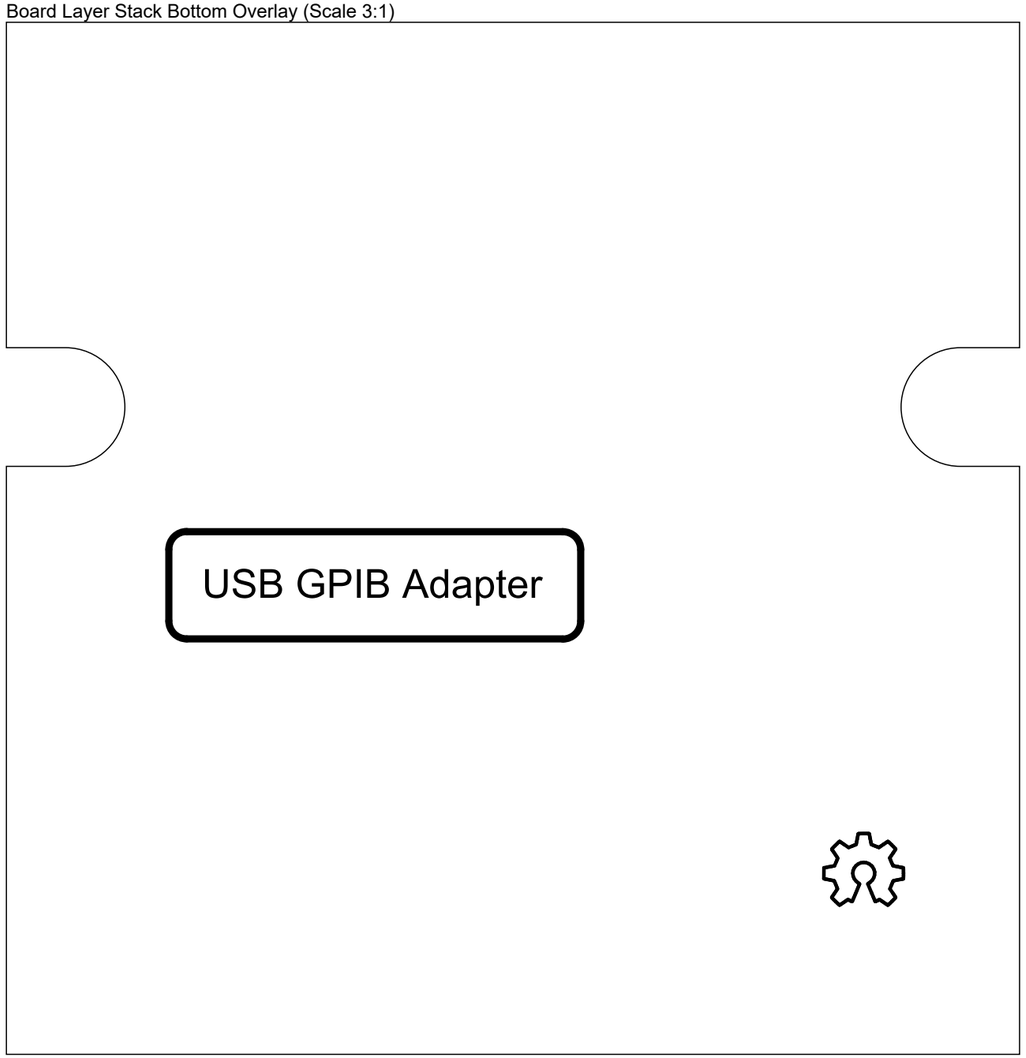
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

Board Layer Stack Bottom Overlay (Scale 3:1)



SILICONVALLEYGARAGE

Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

GENERAL

Unless otherwise specified the following rules apply:

1. DO NOT DEVIATE FROM ARTWORK OR BOM WITHOUT PRIOR AUTHORIZATION.
2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

Bill of Materials and Material Handling

3. THE BOM CONTAINED IN THIS DOCUMENT IS AS-BUILT. NON-INSTALLED PARTS HAVE BEEN REMOVED. ADDITIONAL BOM FORMATS ARE AVAILABLE IN THE PROJECT FILES
4. ANY PART SUBSTITUTIONS MUST BE APPROVED IN WRITING BEFORE ASSEMBLY
5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
7. ESD CONTROL PER IPC RULES

Soldering

8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
10. SOLDERING PREFERRABLY TO BE DONE USING NITROGEN ATMOSPHERE
11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

SILICONVALLEYGARAGE

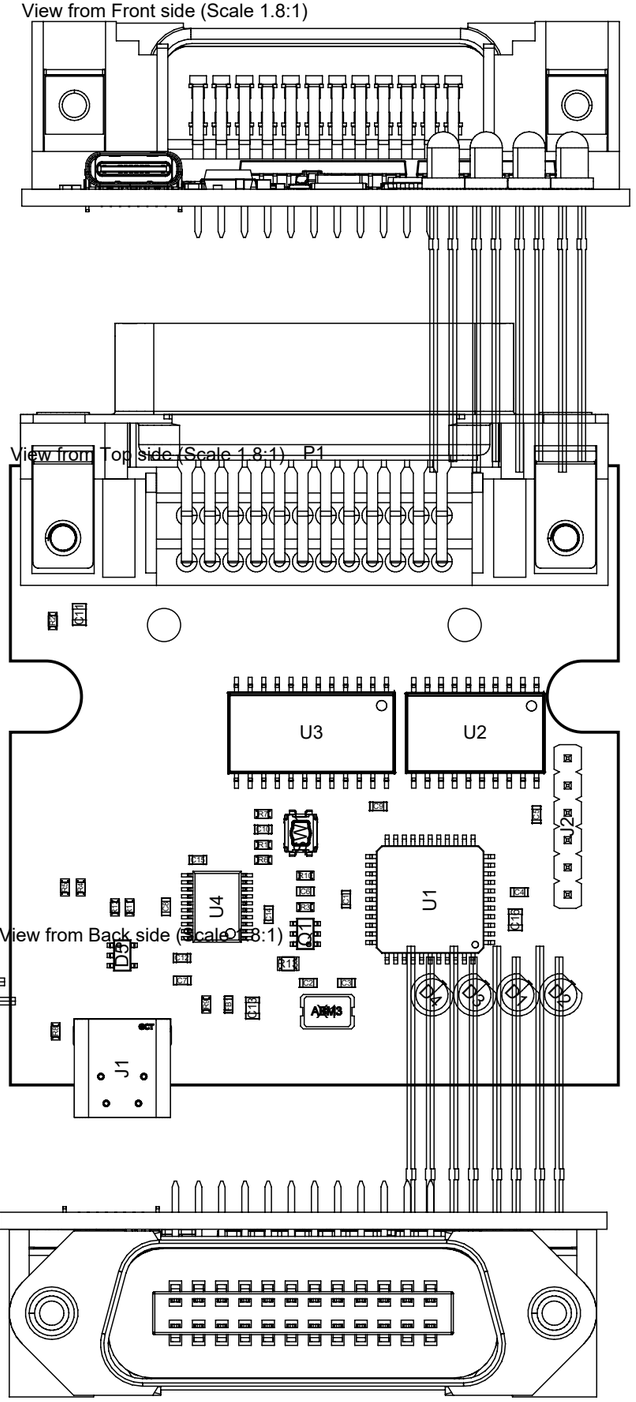
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

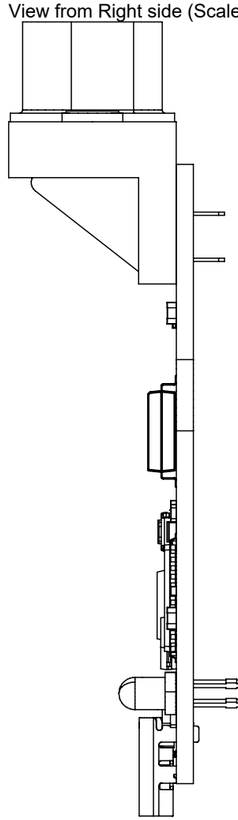
ASSEMBLY DRAWING

2D VIEW

View from Front side (Scale 1.8:1)



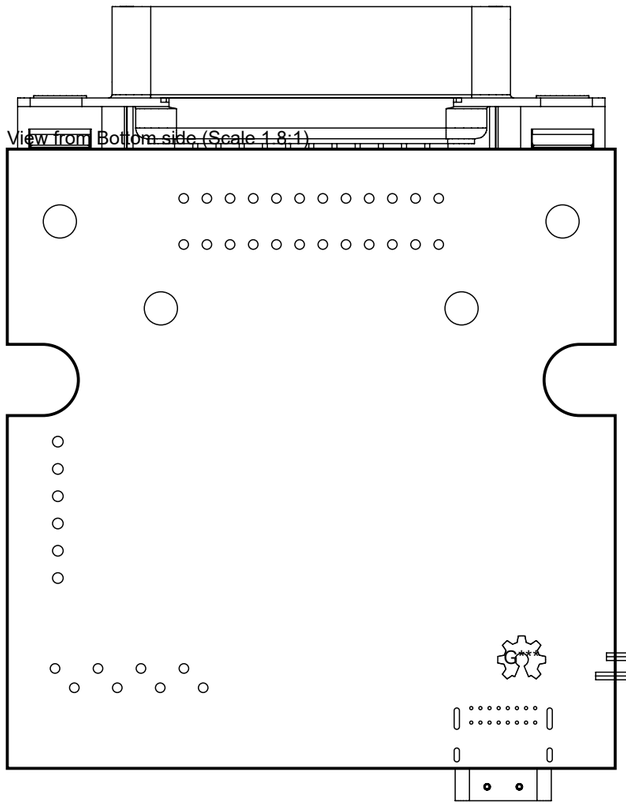
View from Right side (Scale 1.8:1)



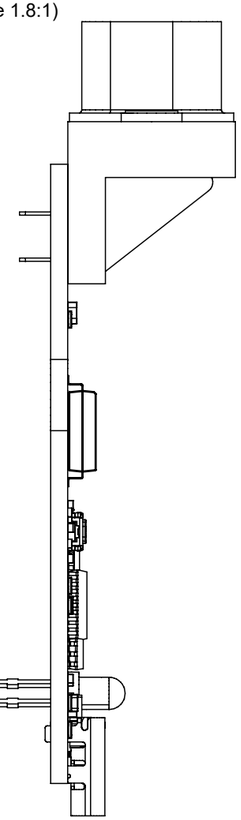
View from Top side (Scale 1.8:1) P1

View from Back side (Scale 1.8:1)

View from Bottom side (Scale 1.8:1)



View from Left side (Scale 1.8:1)



SILICONVALLEYGARAGE

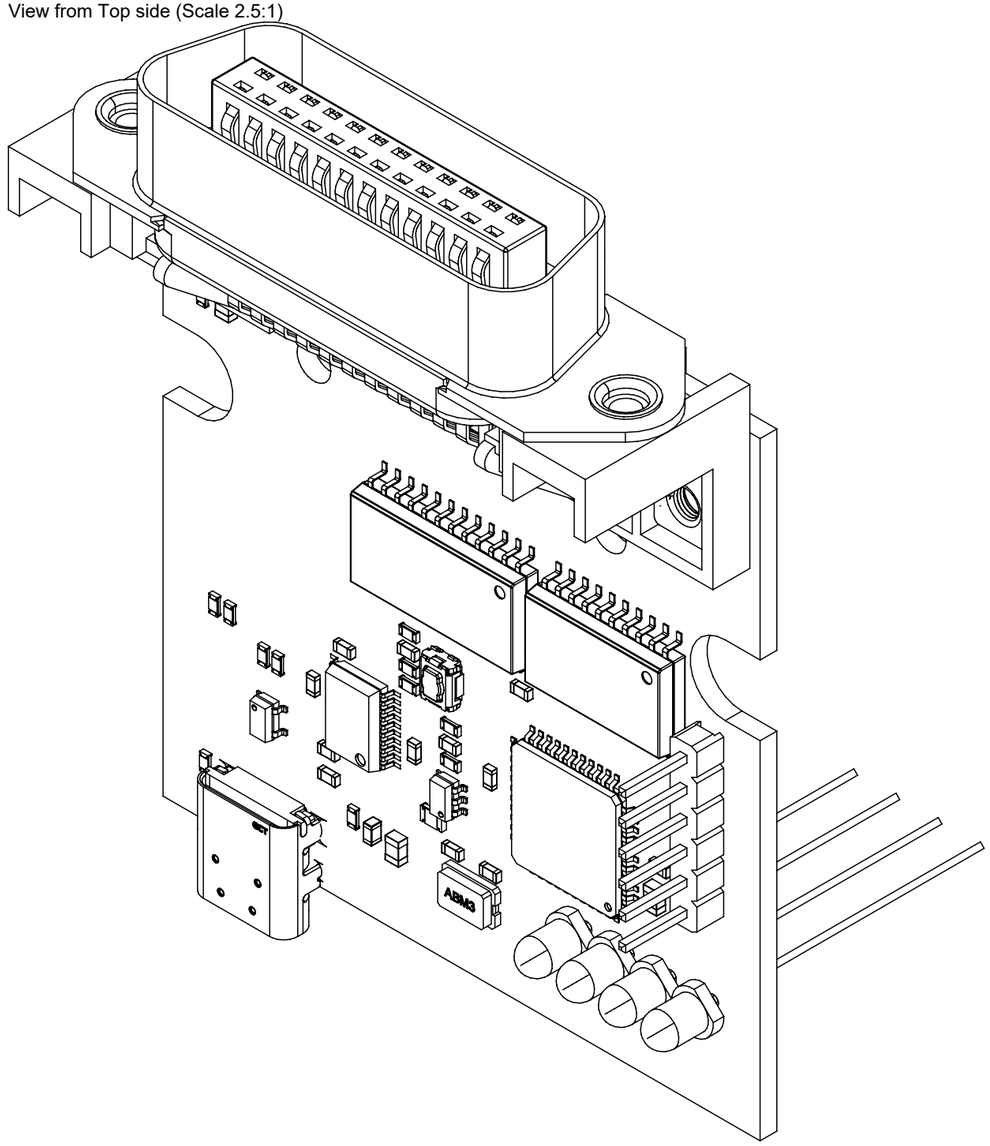
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

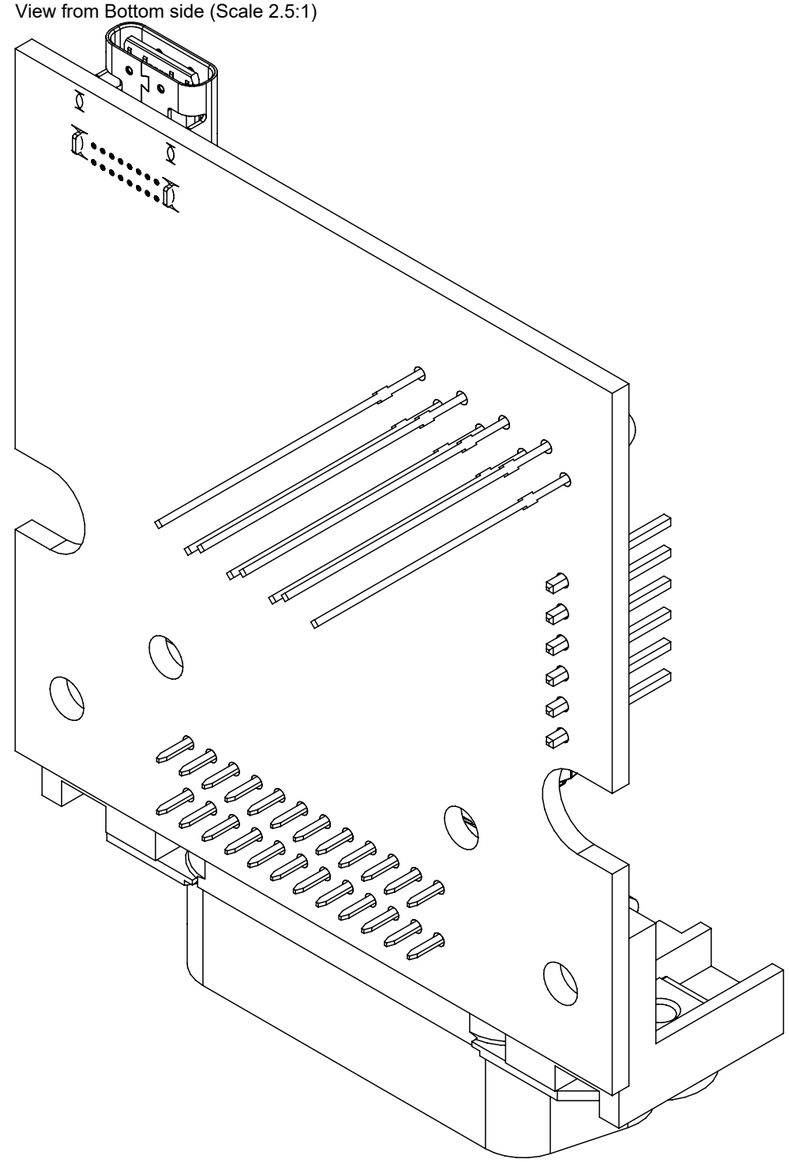
ASSEMBLY DRAWING

3D VIEW

View from Top side (Scale 2.5:1)



View from Bottom side (Scale 2.5:1)



SILICONVALLEYGARAGE

Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

Bill Of Materials

Quantity	Designator	Description	LCSC	MOUSER
11	C1, C4, C5, C6, C7, C8, C9, C10, C12, C14, C15	CAPACITOR,CERAMIC,100nF,50V,X7R,0603	C127833	80-C0603C104K5R
2	C2, C3	CAPACITOR,CERAMIC,18pF,50V,C0G,0603	C2169518	80-C0603C180K5G
1	C11	CAPACITOR,CERAMIC,10nF,200V,X7R,0805,ESD	C36911368	80-C0805C103K2RECAUT
2	C13, C16	CAPACITOR,CERAMIC,10uF,25V,X5R,0805	C3039694	187-CL21B106KAYQNNE
4	D1, D2, D3, D4	LED,TH,GREEN,42mCd,3MM		78-VLMPG33N1P2
1	D5	DIODE,TVS,DUAL,UNIDIRECTIONAL,USB	C22358704	710-824011
1	FB1	FERRITE,1KZ@100MHz,0R2DC,0603	C160982	81-BLM18KG102SN1D
1	J1	CONN,USB-C,16P,RA,TH,8.94X9.17	C7095263	640-USB4085-GF-A
1	J2			
1	MECH1	ENCLOSURE,ABS,GRAY,HAMMOND, 1593KBK		546-1593KBK
1	P1	CONN,GPIB,24P,RIGHT ANGLE,TH		636-112-024-113R001
1	Q1	XSTR,PMOS,20V,5.97A,VISHAY,SI3443,SOT26	C727385	781-SI3443CDV-GE3
2	R1, R3	RESISTOR,10K,1%,100mW,0603 (1608)	C98220	603-RC0603FR-0710KL
1	R2	RESISTOR,4K7,1%,100mW,0603 (1608)	C99782	603-RC0603FR-074K7L
5	R4, R5, R6, R7, R10	RESISTOR,1K,1%,100mW,0603 (1608)	C22548	603-RC0603FR-071KL
2	R8, R9	RESISTOR,5K1,1%,100mW,0603 (1608)	C105580	603-RC0603FR-075K1
2	R11, R12	RESISTOR,27R,1%,100mW,0603 (1608)	C137753	603-RC0603FR-0727RL
1	R13	RESISTOR,0R,JUMPER	C96345	603-RC0805JR-070RL
1	SW1	SW,SMD,TACT,4PIN,2.9X3.5,4PIN	C483888	667-EVP-AA202K
1	U1	IC,CPU,MICROCHIP,PIC18F4520,TQFP44	C9734	579-PIC18F4520-I/PT
1	U2	IC,XCVR,GPIB,DATA.TI,SN75160DW,SO20W	C882412	595-SN75160BDW
1	U3	IC,XCVR,GPIB,CONTROL,TI,SN75162DW,SO24W	C2863933	595-SN75162BDWR
1	U4	IC,XCVR,USB UART,FTDI,FT231XS-R,TSSOP20	C132160	895-FT231XS-R
1	X1	XTAL,18.432MHz,ABRACON ABM3,SMD5032	C1985331	815-ABM3-18.43-D2Y-T

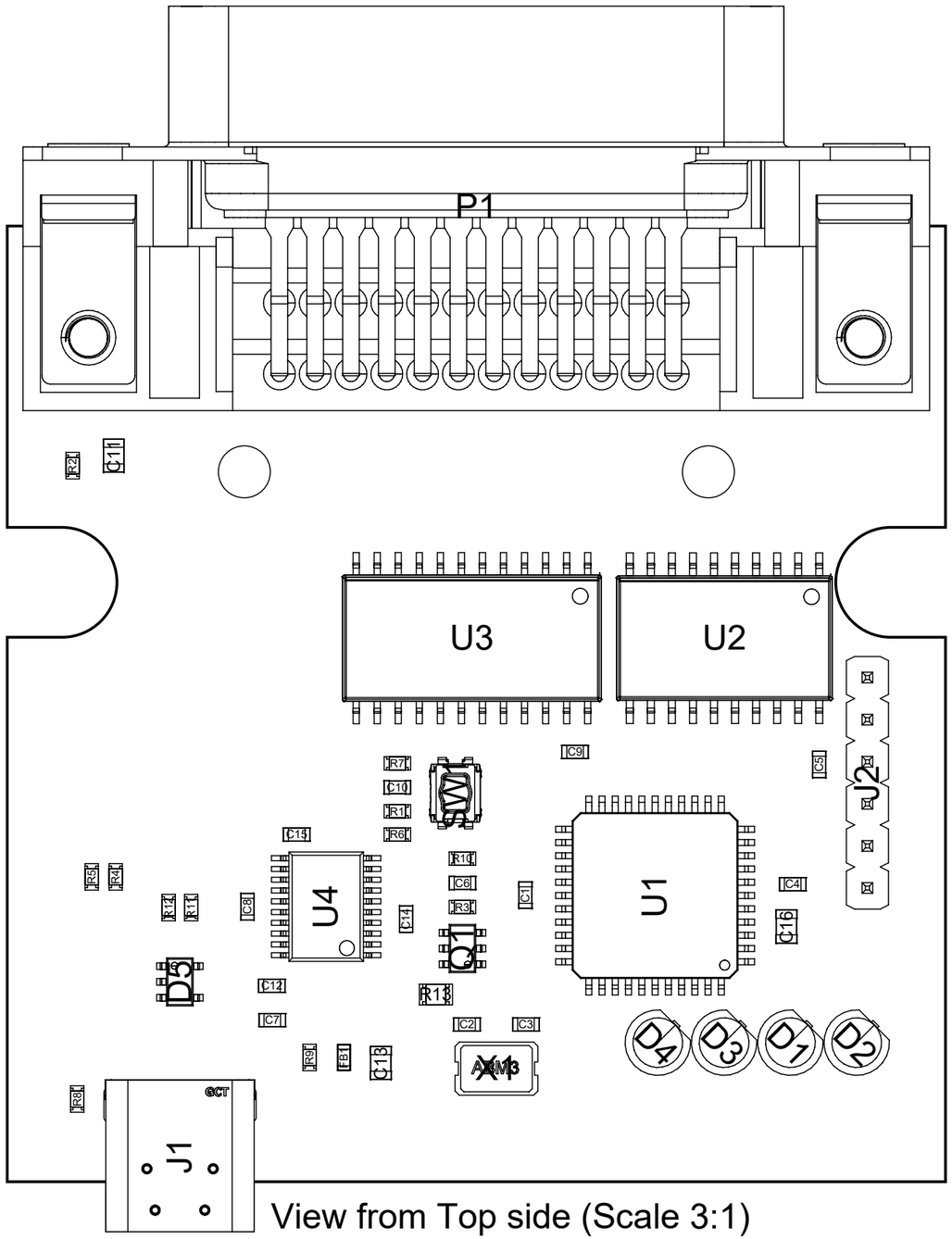
SILICONVALLEYGARAGE

Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

DESIGNATORS FRONT



View from Top side (Scale 3:1)

SILICONVALLEYGARAGE

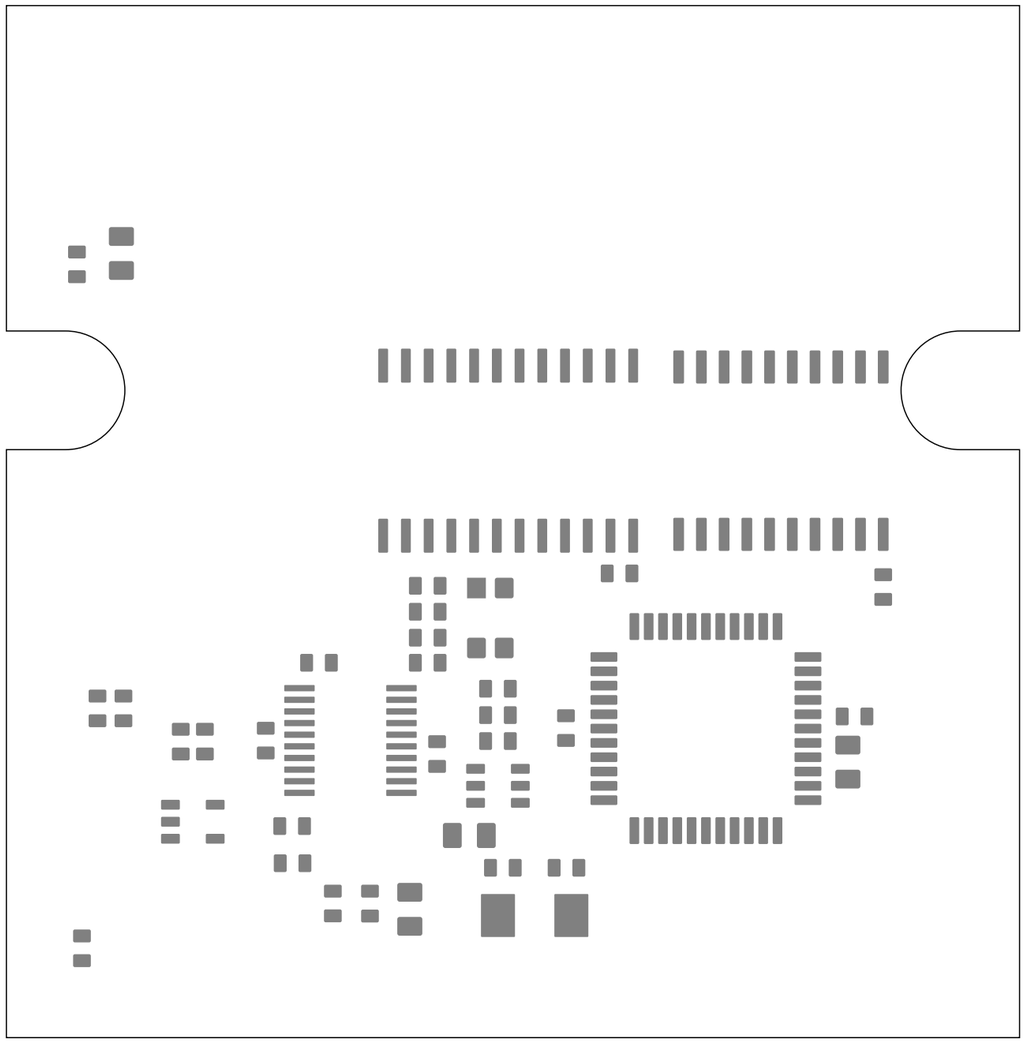
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

PASTE MASK TOP

Top Paste (Scale 3:1)



SILICONVALLEYGARAGE

Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

ASSEMBLY DRAWING

GENERAL

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10. SOLDER MASK COLOR : BLACK
11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm
12. SILKSCREEN COLOR : WHITE

STACKUP / IMPEDANCE CONTROL

13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG
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QA, ELECTRICAL TEST AND MARKINGS

15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY

SILICONVALLEYGARAGE

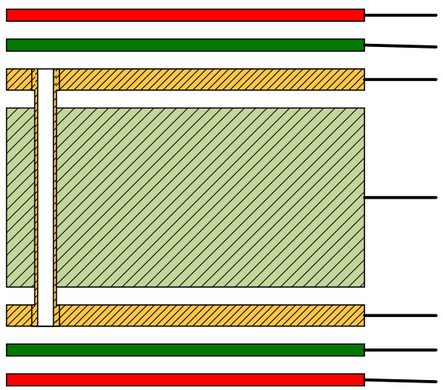
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER STACK

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber	Dk	Weight	Constructions	Df	Resin
	Top Overlay			Legend	GTO					
Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5				
Copper	**Top Layer**	**0.036mm(1.400mil)**		**Signal**	**GTL**		**1oz**			
		1.500mm(59.055mil)	*FR-4*	*Dielectric*		*4.8*				
Copper	**Bottom Layer**	**0.036mm(1.400mil)**		**Signal**	**GBL**		**1oz**			
Surface Material	Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5				
	Bottom Overlay			Legend	GBO					

Total thickness: 1.591mm(62.655mil)

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FABRICATION DRAWING

DRILL LEGEND

Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Description	Hole Tolerance	Via Type	Via Feature
▽	2	0.500mm(19.685mil)	Plated	Round	Top Layer - Bottom Layer	Via				Type 1B	Tenting Both
□	4	3.100mm(122.047mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded				
	6 Total										

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FABRICATION DRAWING

DRILL DRAWING

Drill Drawing View (Scale 4:1)

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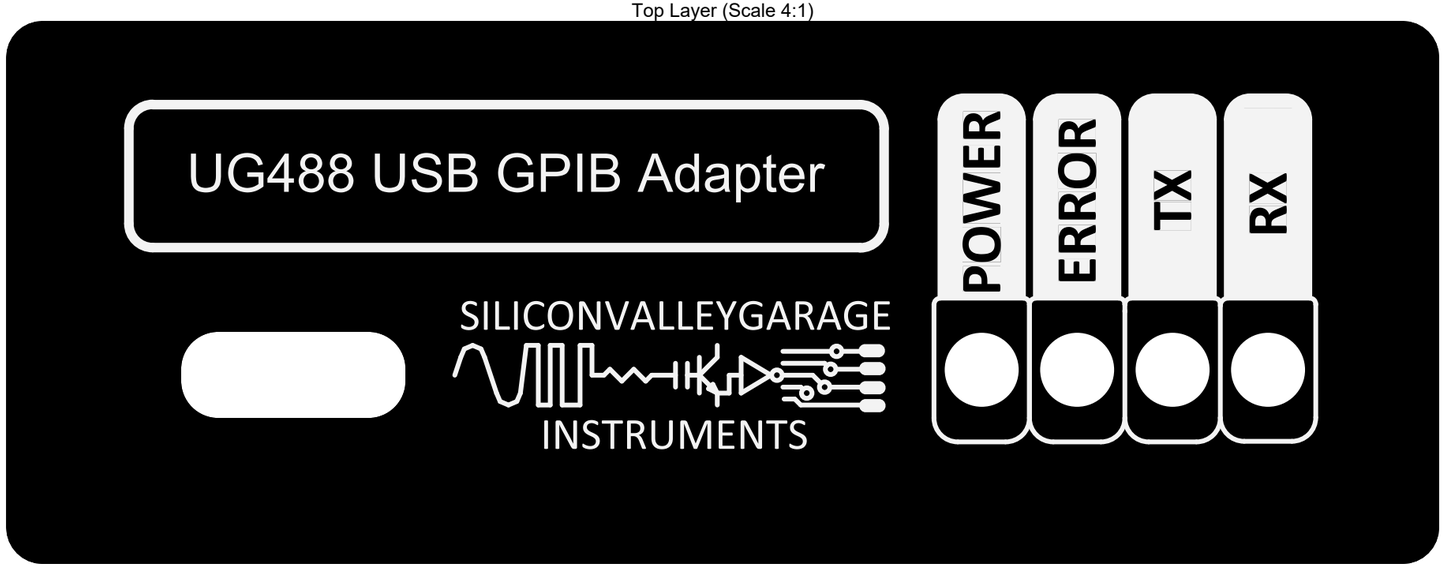
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

COMPOSITE VIEW FRONT

Top Layer (Scale 4:1)



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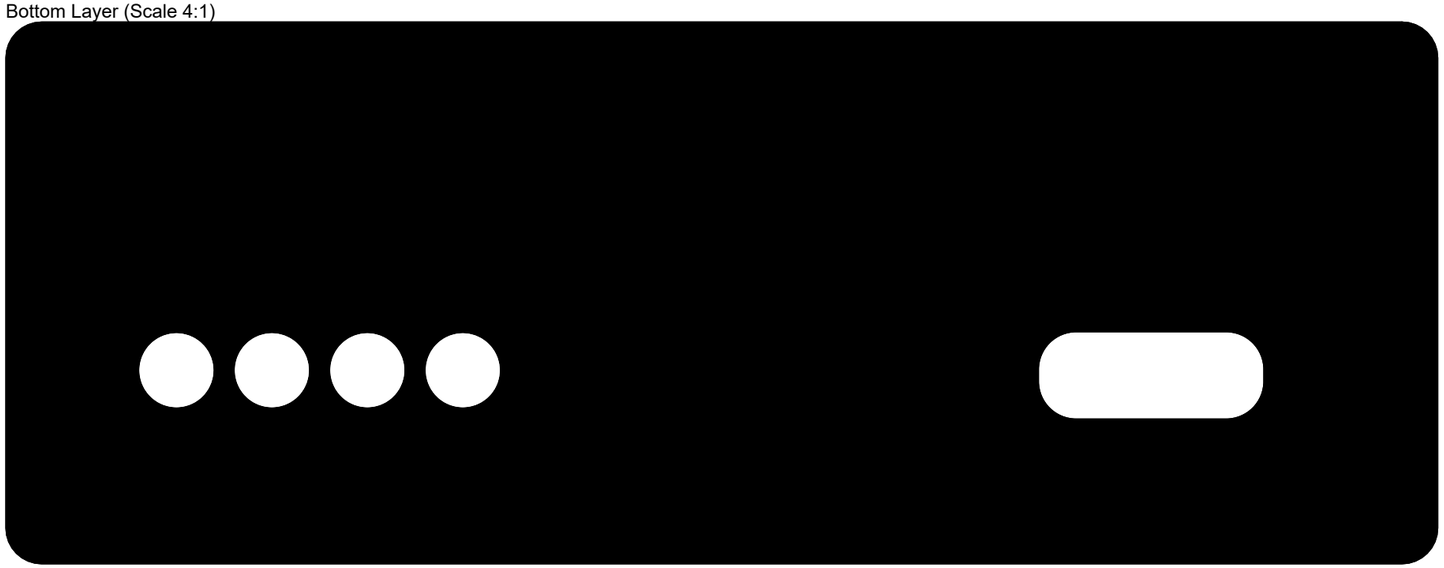
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

COMPOSITE VIEW BACK

Bottom Layer (Scale 4:1)



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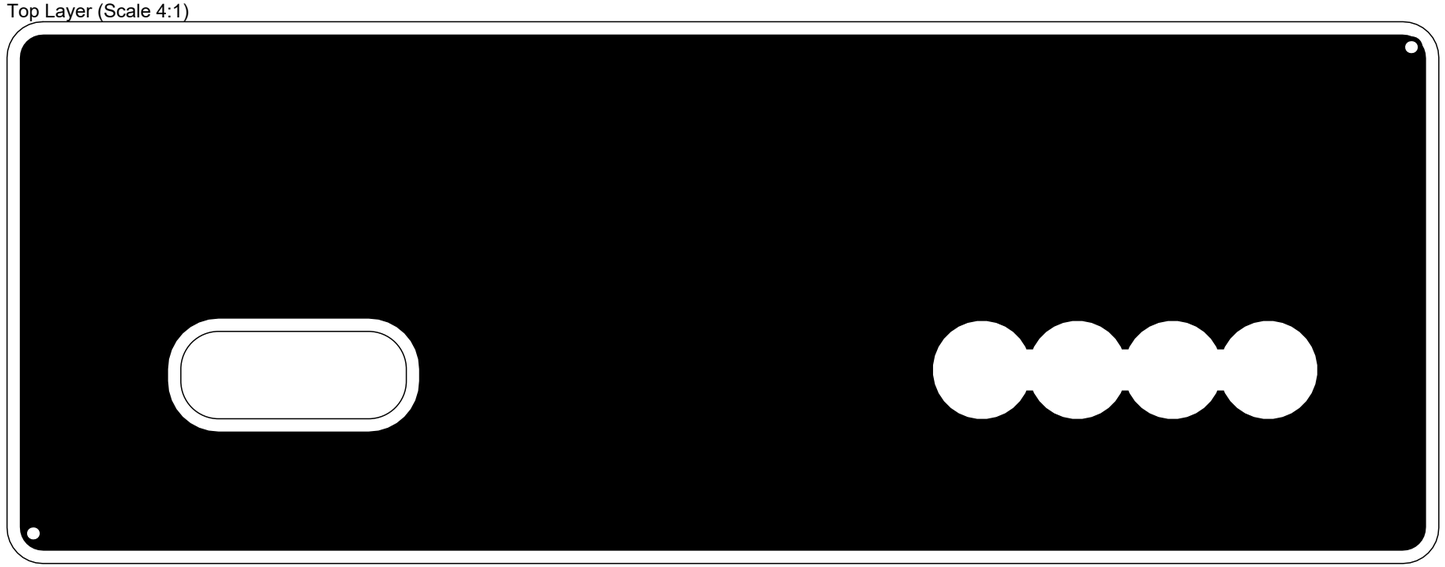
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP LAYER

Top Layer (Scale 4:1)



SILICONVALLEYGARAGE

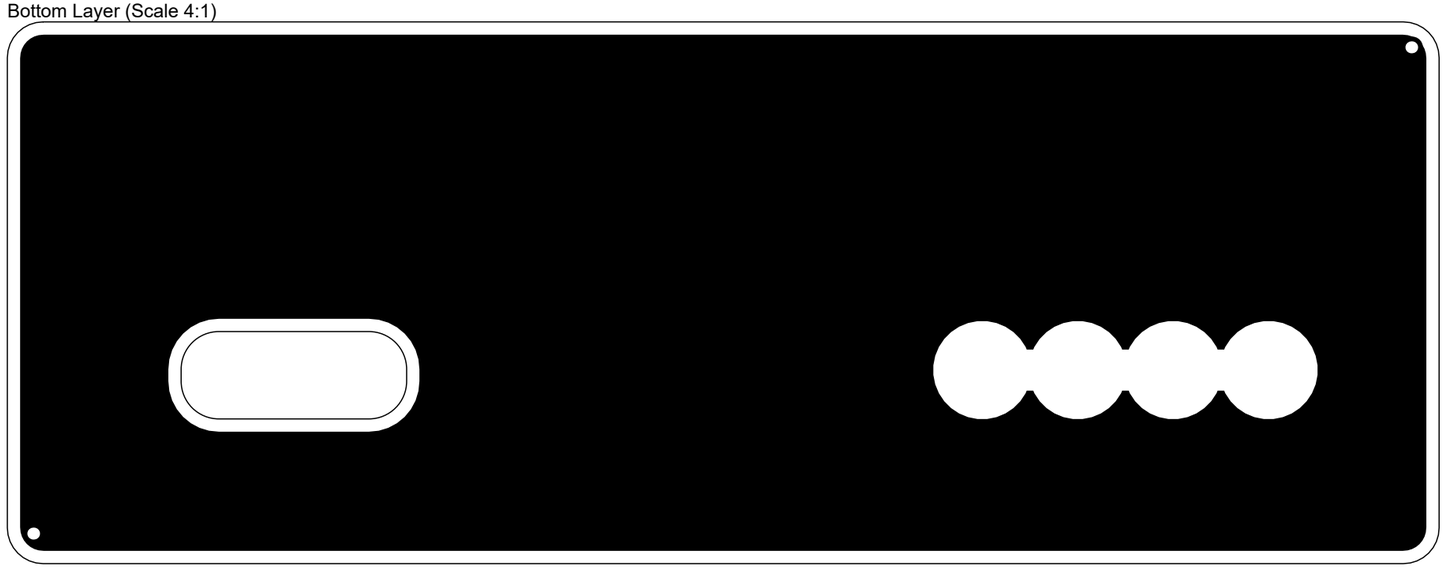
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM LAYER

Bottom Layer (Scale 4:1)



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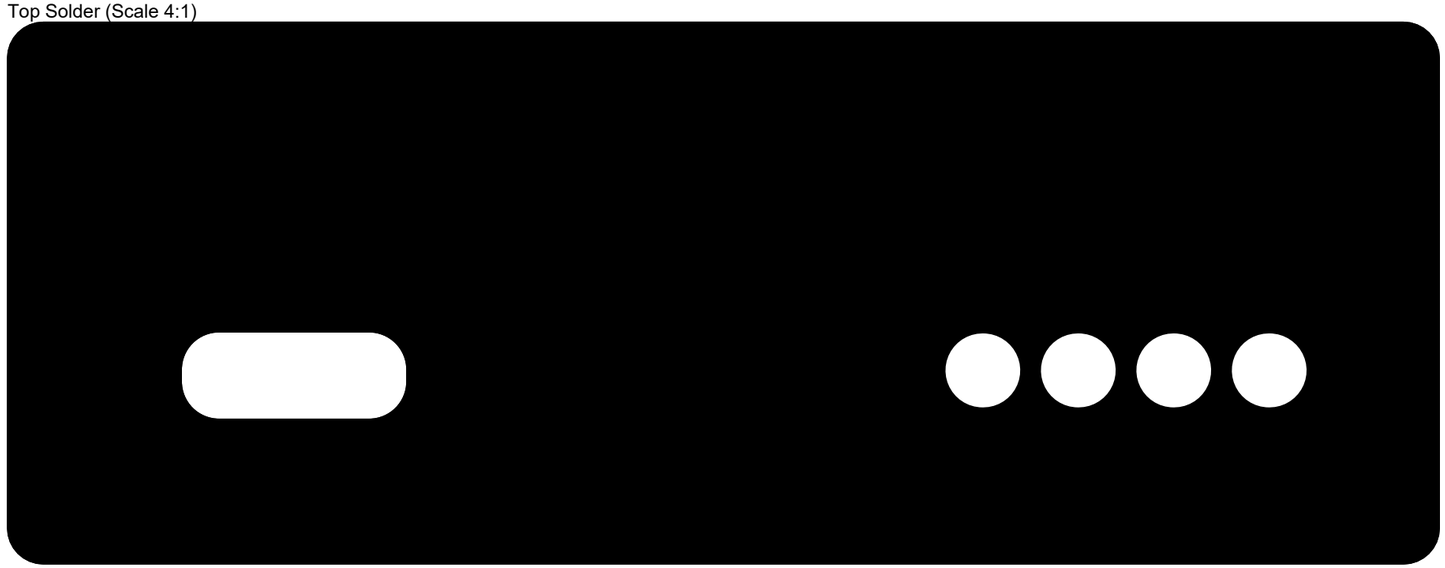
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP SOLDER MASK

Top Solder (Scale 4:1)



SILICONVALLEYGARAGE

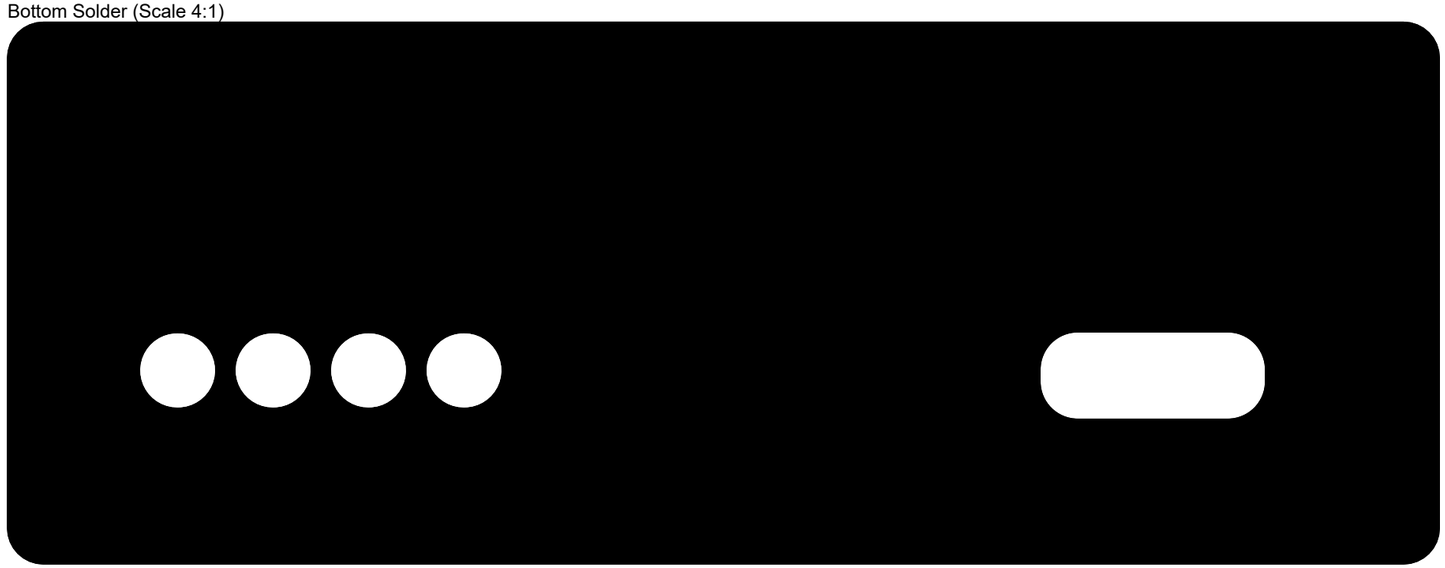
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SOLDER MASK

Bottom Solder (Scale 4:1)



SILICONVALLEYGARAGE

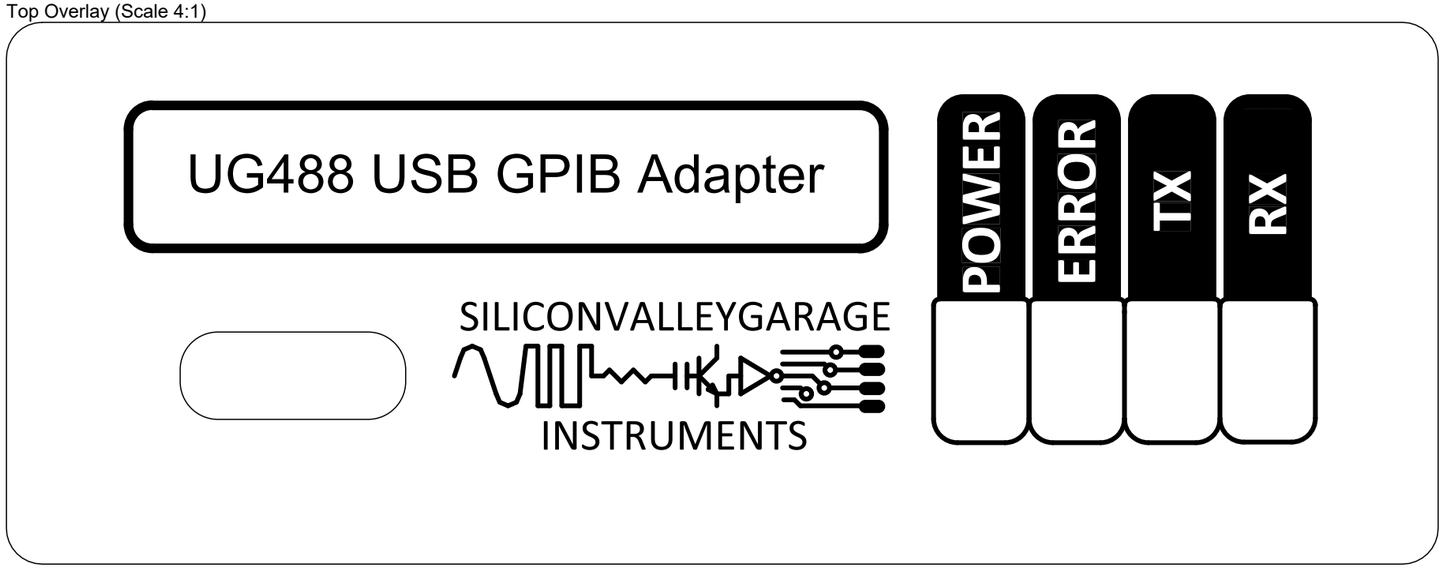
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : TOP SILKSCREEN (LEGEND)

Top Overlay (Scale 4:1)



SILICONVALLEYGARAGE

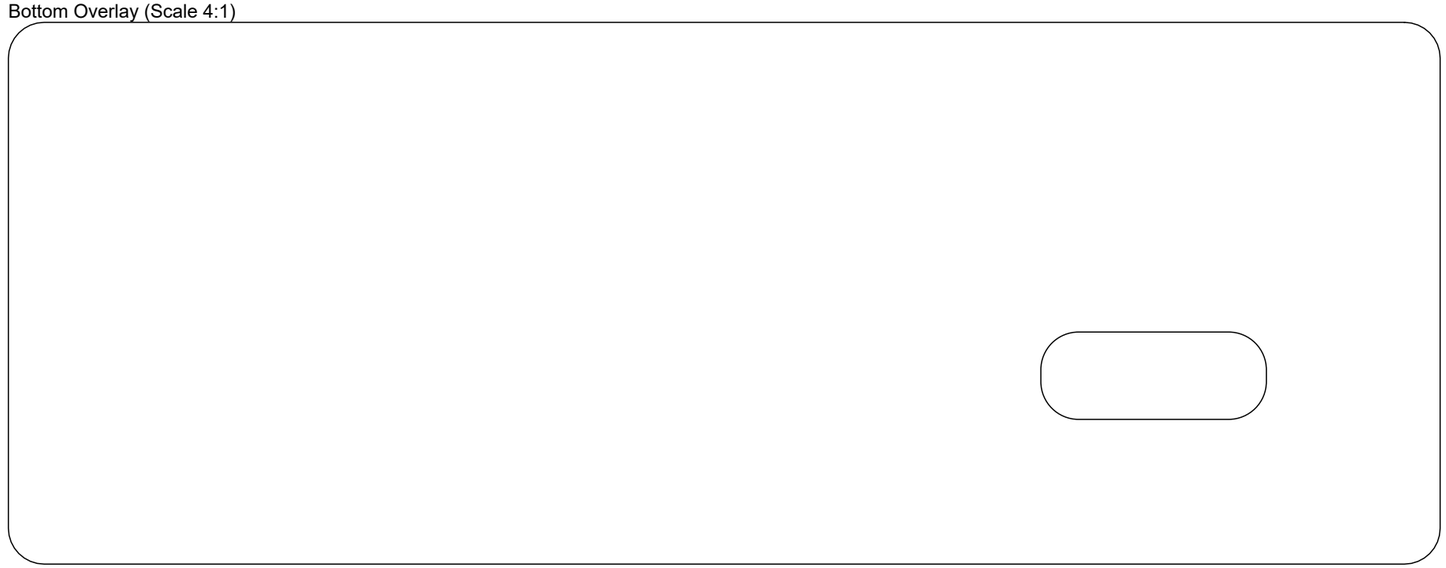
Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING

LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

Bottom Overlay (Scale 4:1)



SILICONVALLEYGARAGE

Project USB-GPIB.PrjPcb

Version: | Variant [No Variations]

FABRICATION DRAWING