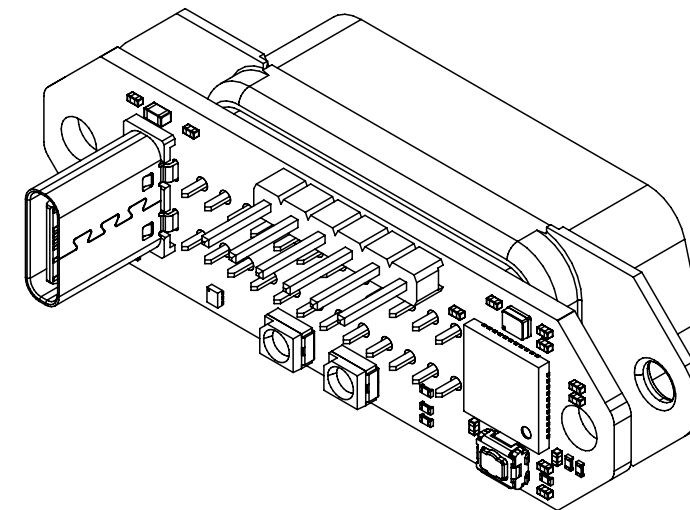
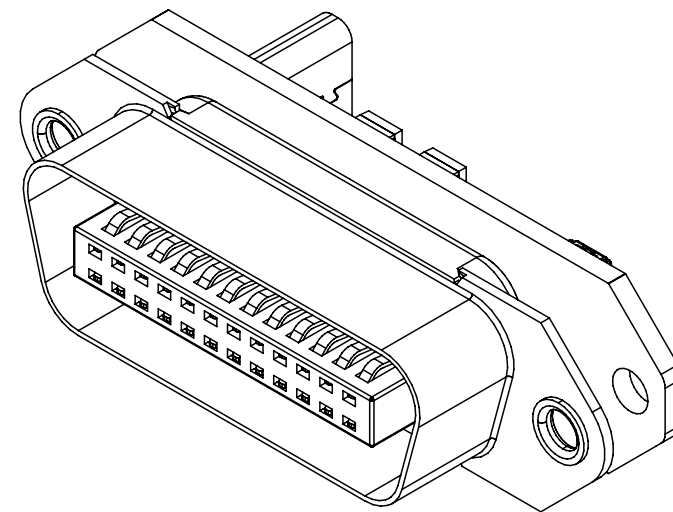
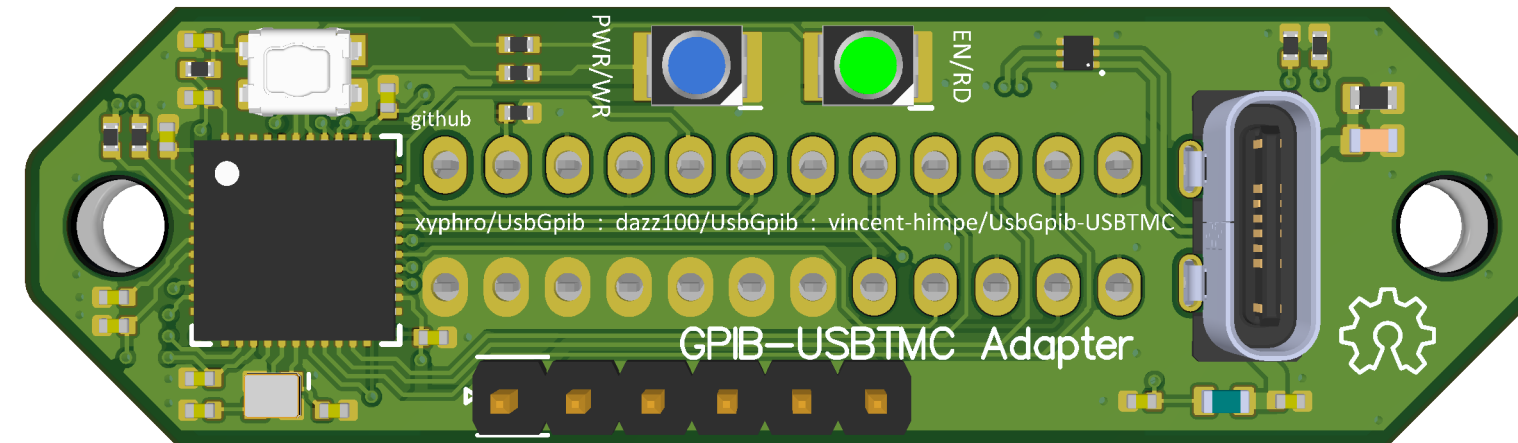
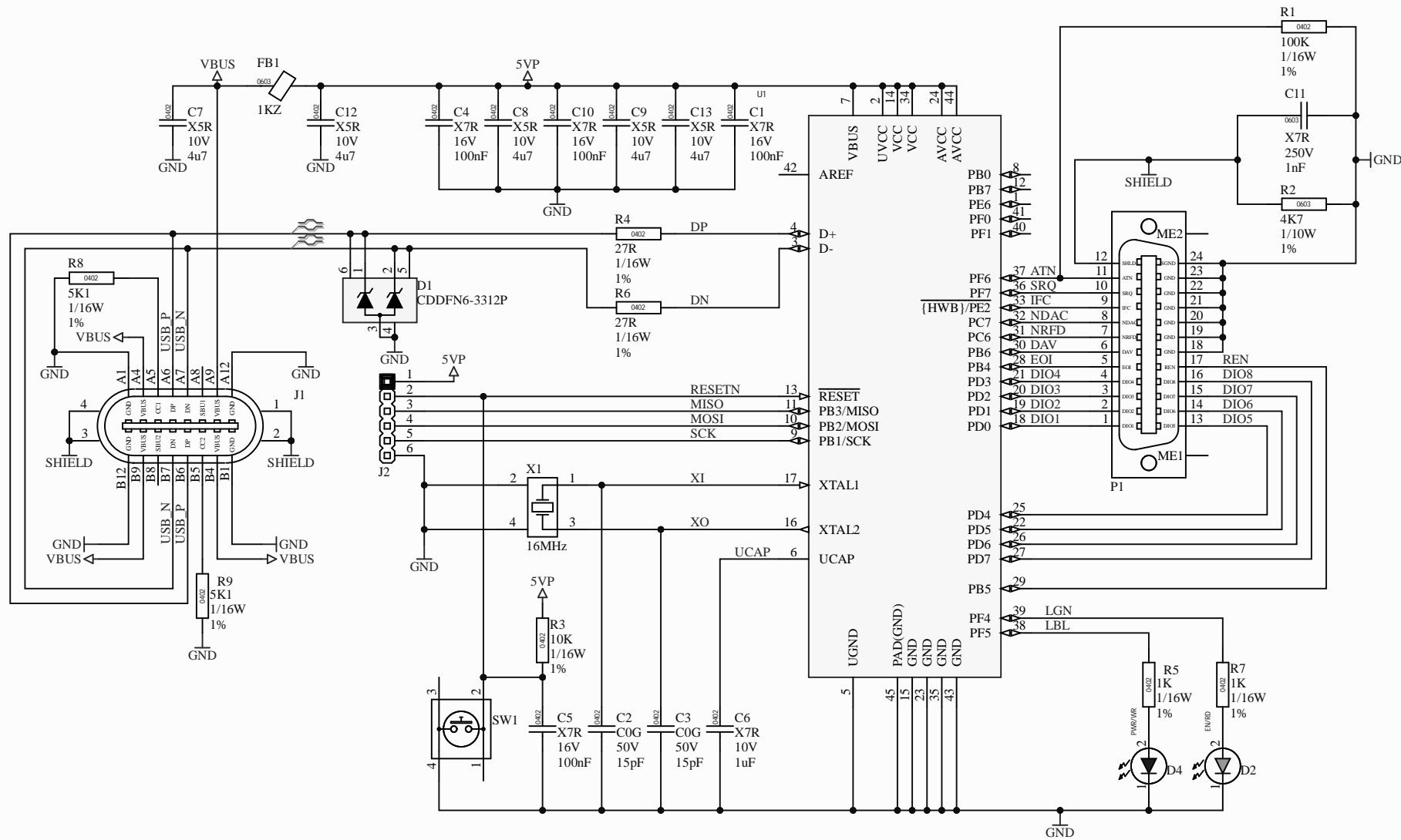


# USBgpib-USBTMC-V3mini.PrjPcb



Document Creation Date: 7/1/2025

Design : Vincent Himpe



BASED ON THE WORK OF :

<https://github.com/xyphro/UsbGpib>

<https://github.com/dazz100/UsbGpib>

Modifications by Vincent Himpe

SWITCHED TO VERTICAL GPIB CONNECTOR

Board is sized to fit behind connector

Component footprint changes (QFN,0402)

Added Ferrite bead

Reset button added






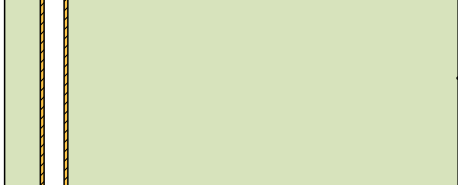





Changed TVS diode

BOM optimized for JLCPCB assembly service (LCSC parts)

1	2	3	4	5	6
GENERAL					
A	<b>GENERAL</b>				
	1. DO NOT ALTER SUPPLIED COPPER OR DRILL DATA				
	2. NO COPPER BALANCING OR REMOVAL OF UNUSED PADS ALLOWED.				
	3. SILKSCREEN MAY BE CLIPPED / TRIMMED TO EXPOSE COPPER				
	4. PCB DESIGN AND ACCEPTANCE CRITERIA SHALL FOLLOW THE REQUIREMENTS OF IPC-2221, IPC-2222, AND IPC-6012 CLASS 2				
	5. ALL SPECIFICATIONS SHALL BE THE LATEST STANDARDS, UNLESS OTHERWISE NOTED				
B	6. ALL MODIFICATIONS MUST BE COMMUNICATED AND APPROVED IN WRITING.				
	<b>MATERIALS</b>				
	7. MATERIALS SHALL BE ACCORDING TO THE STACKUP DRAWING IN THIS DOCUMENT.				
	8. MATERIAL SHALL HAVE A FLAMABILITY RATING OF UL 94V-0 OR BETTER				
	9. SURFACE FINISH : HASL				
	10. SOLDER MASK COLOR : BLACK				
C	11. SOLDERMASK MAX REGISTRATION ERROR : 0.05mm				
	12. SILKSCREEN COLOR : WHITE				
	<b>STACKUP / IMPEDANCE CONTROL</b>				
	13. THICKNESS LISTED IN LAYER STACK LEGEND REPRESENT FINAL PRESSED VALUES FOR THE PREPREG				
	14. IMPEDANCE CONTROL, IF ANY, SHALL BE PER LISTED TABLE WITH A MAX TOLERANCE OF +/-10%				
	<b>QA, ELECTRICAL TEST AND MARKINGS</b>				
D	15. PCB SHALL BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY				
				<div><div>Fullyrouted</div><div>Project USBgpib-USBTMC-V3mini.PrjPcb</div><div>Version: 3Mini   Variant [No Variations]</div><div>FABRICATION DRAWING</div></div>	
1	2	3	4	5	6

# LAYER STACK

## Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber	Dk	Weight	Constructions	Df	Resin
		Top Overlay			Legend	GTO					
	Surface Material	Top Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GTS	3.5				
	Copper	Top Layer	0.035mm(1.378mil)		Signal	GTL		1oz			
	Prepreg		0.210mm(8.284mil)	7628 x 1	Dielectric		4.1		1080	0.02	62%
	CF-004	Layer 1	0.015mm(0.598mil)		Signal	G1		0.5oz			
	Core		1.065mm(41.929mil)	FR-4	Dielectric		4.8				
	CF-004	Layer 2	0.015mm(0.598mil)		Signal	G2		0.5oz			
	Prepreg		0.210mm(8.284mil)	7628 x 1	Dielectric		4.1		1080	0.02	62%
	Copper	Bottom Layer	0.035mm(1.378mil)		Signal	GBL		1oz			
	Surface Material	Board Layer Stack Bottom Solder	0.010mm(0.400mil)	Solder Resist	Solder Mask	GBS	3.5				
		Board Layer Stack Bottom Overlay			Legend	GBO					
Total thickness: 1.607mm(63.249mil)											

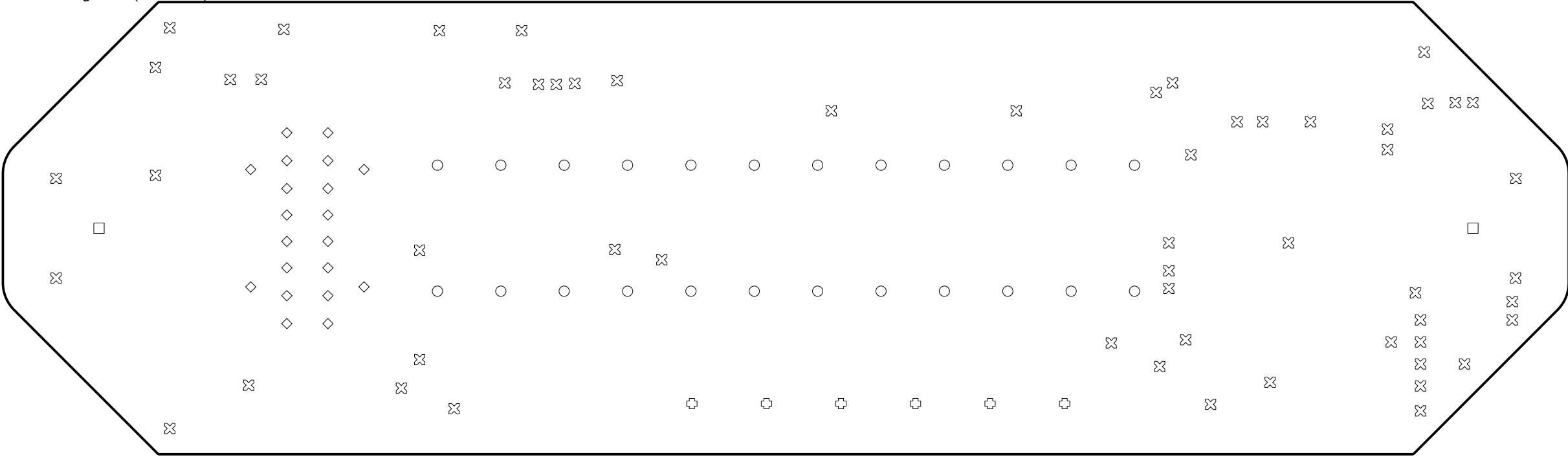
Total thickness: 1.607mm(63.249mil)





DRILL DRAWING

Drill Drawing View (Scale 6:1)



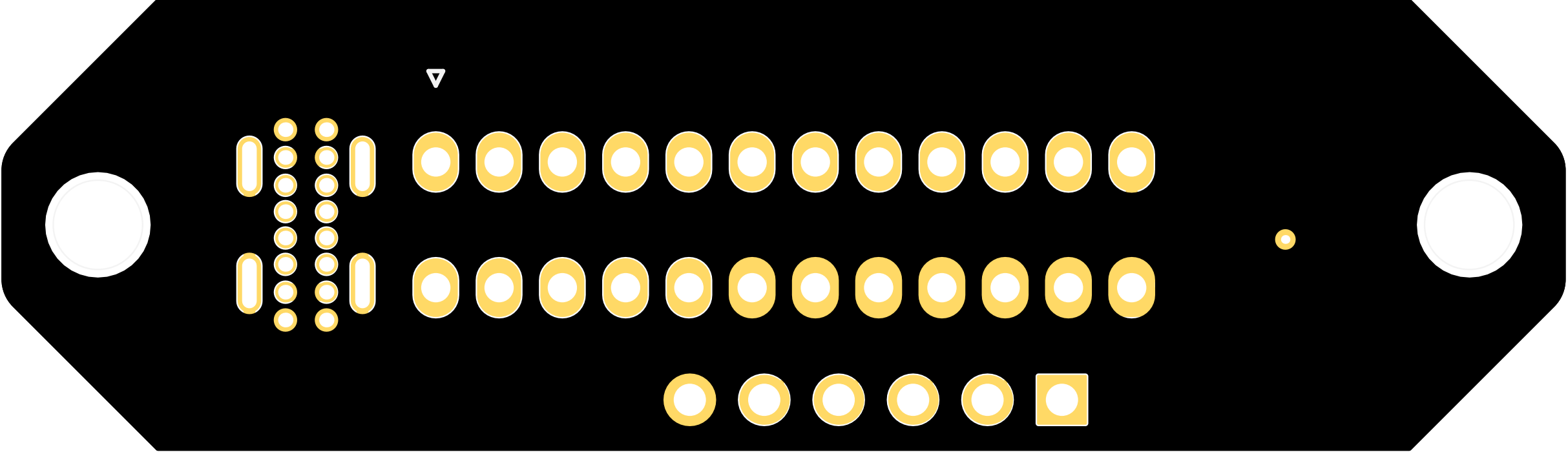
Project USBgpib-USBTMC-V3mini.PrjPcb

Version: 3Mini | Variant [No Variations]

FABRICATION DRAWING

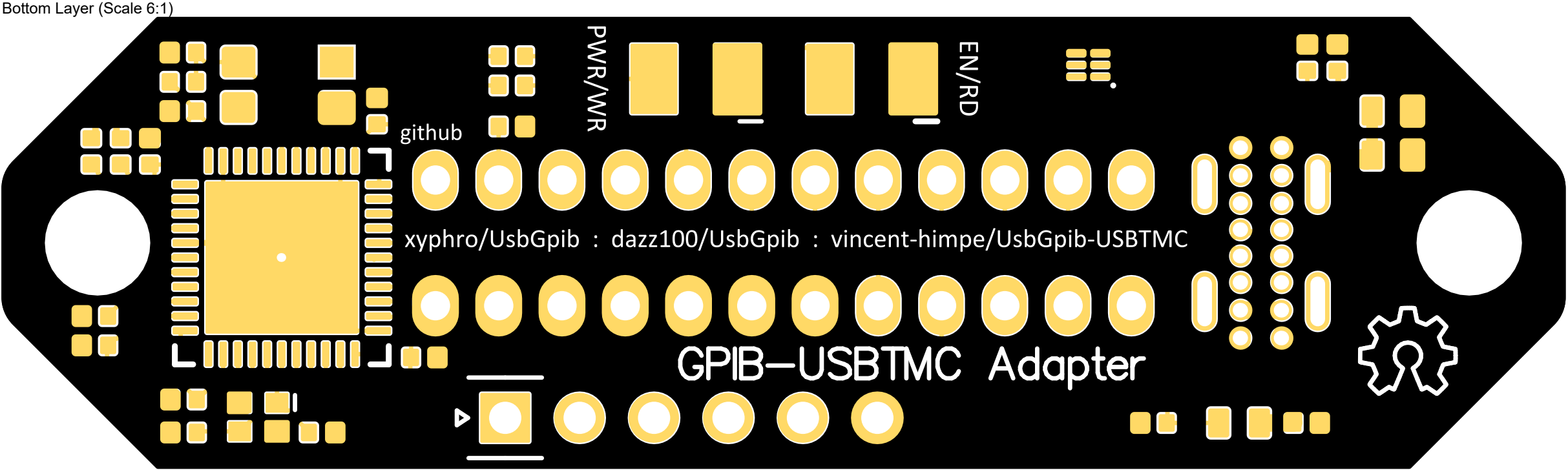
COMPOSITE VIEW FRONT

Top Layer (Scale 6:1)



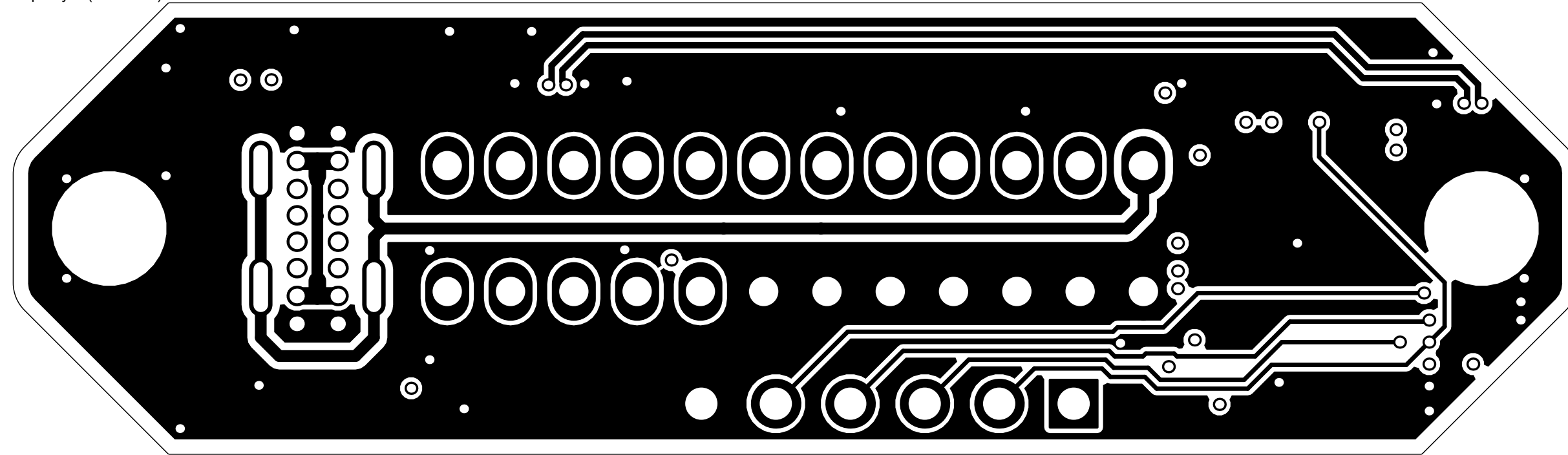


COMPOSITE VIEW BACK



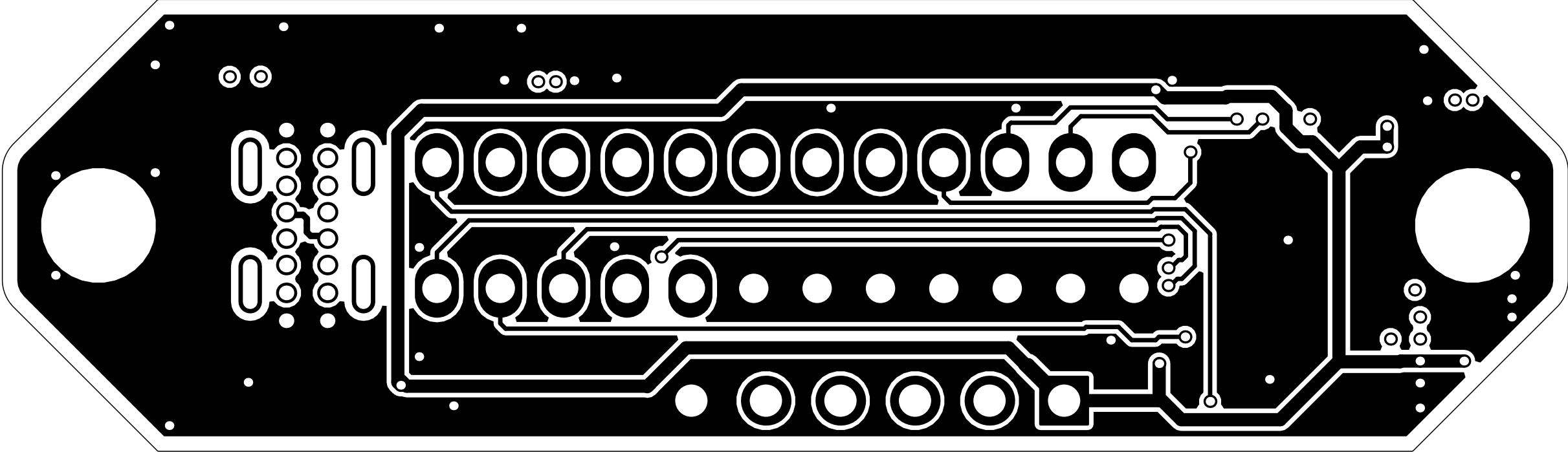
LAYER VIEW : TOP LAYER

Top Layer (Scale 6:1)



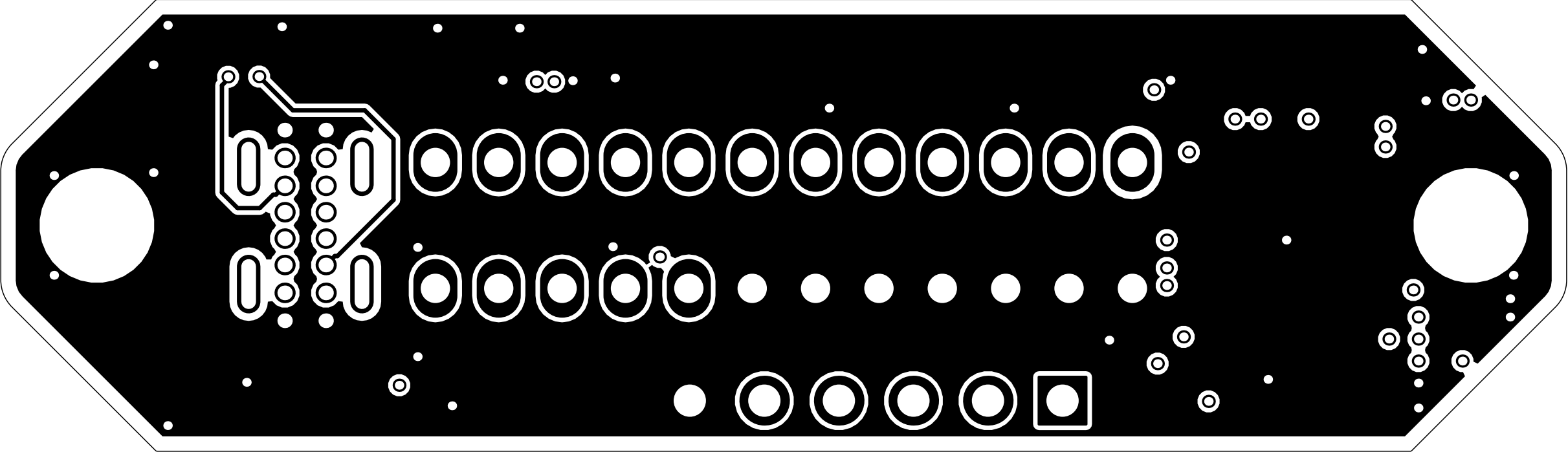
LAYER VIEW : MID LAYER 1

Layer 2 (Scale 6:1)



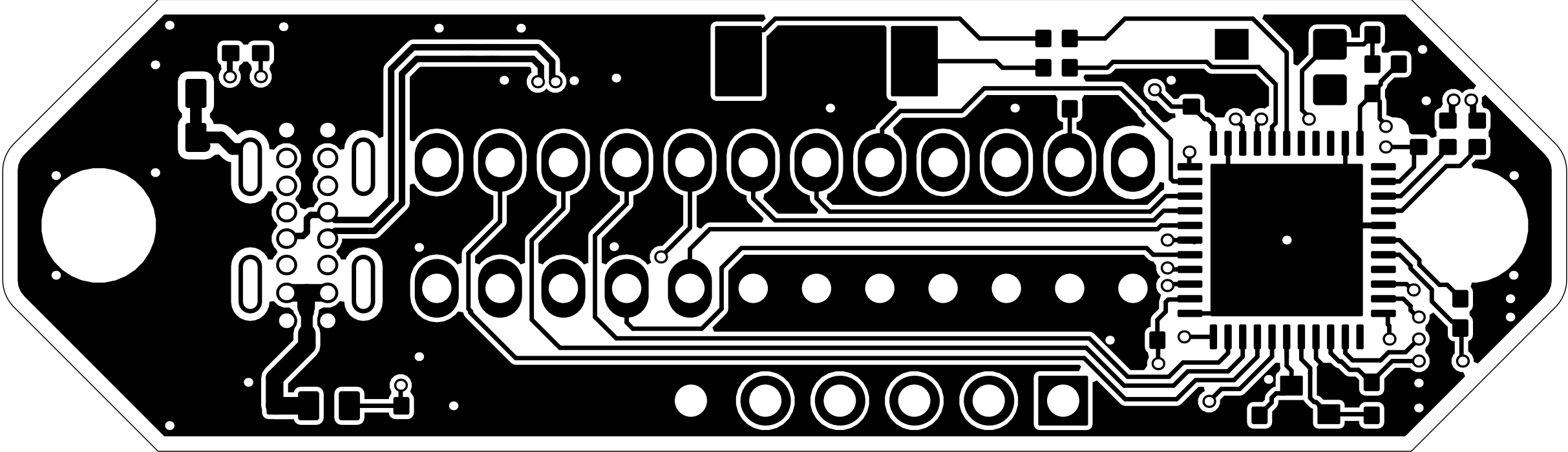
LAYER VIEW : MID LAYER 2

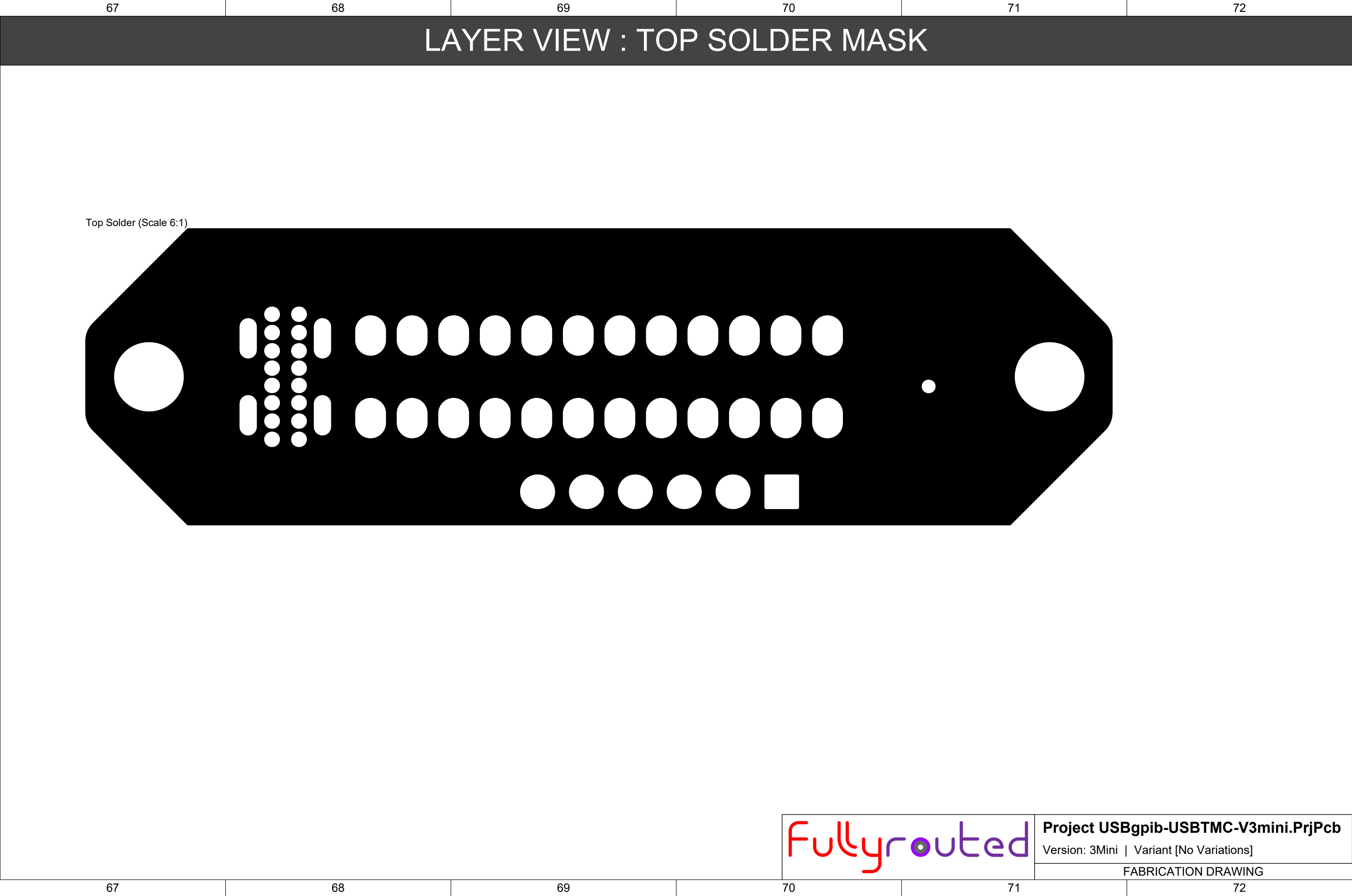
Layer 1 (Scale 6:1)



LAYER VIEW : BOTTOM LAYER

Bottom Layer (Scale 6:1)



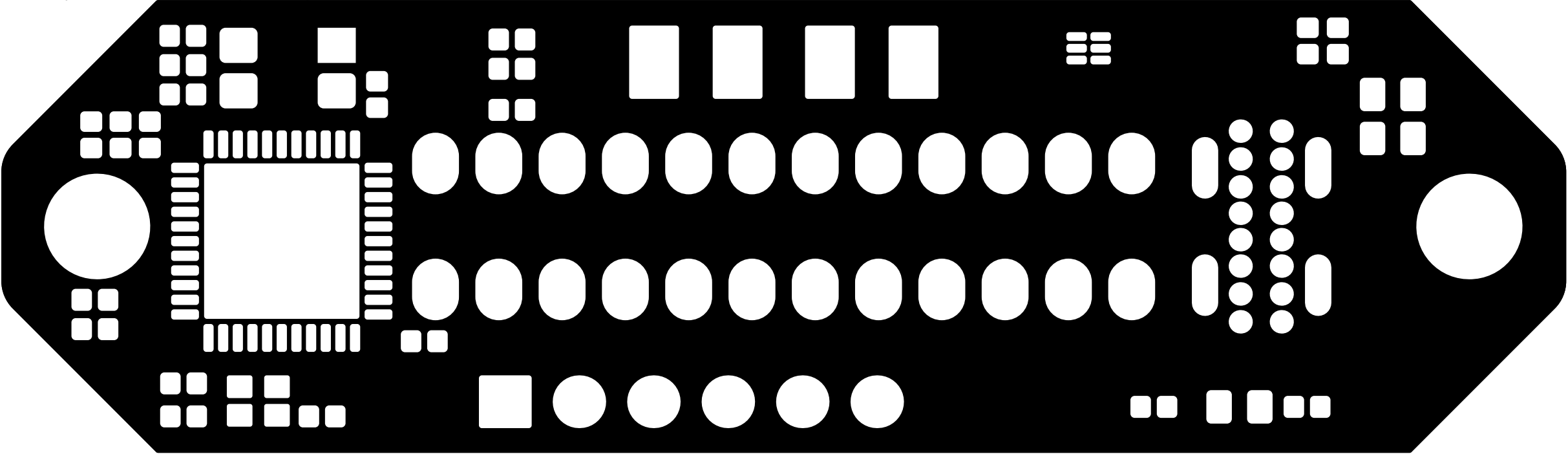


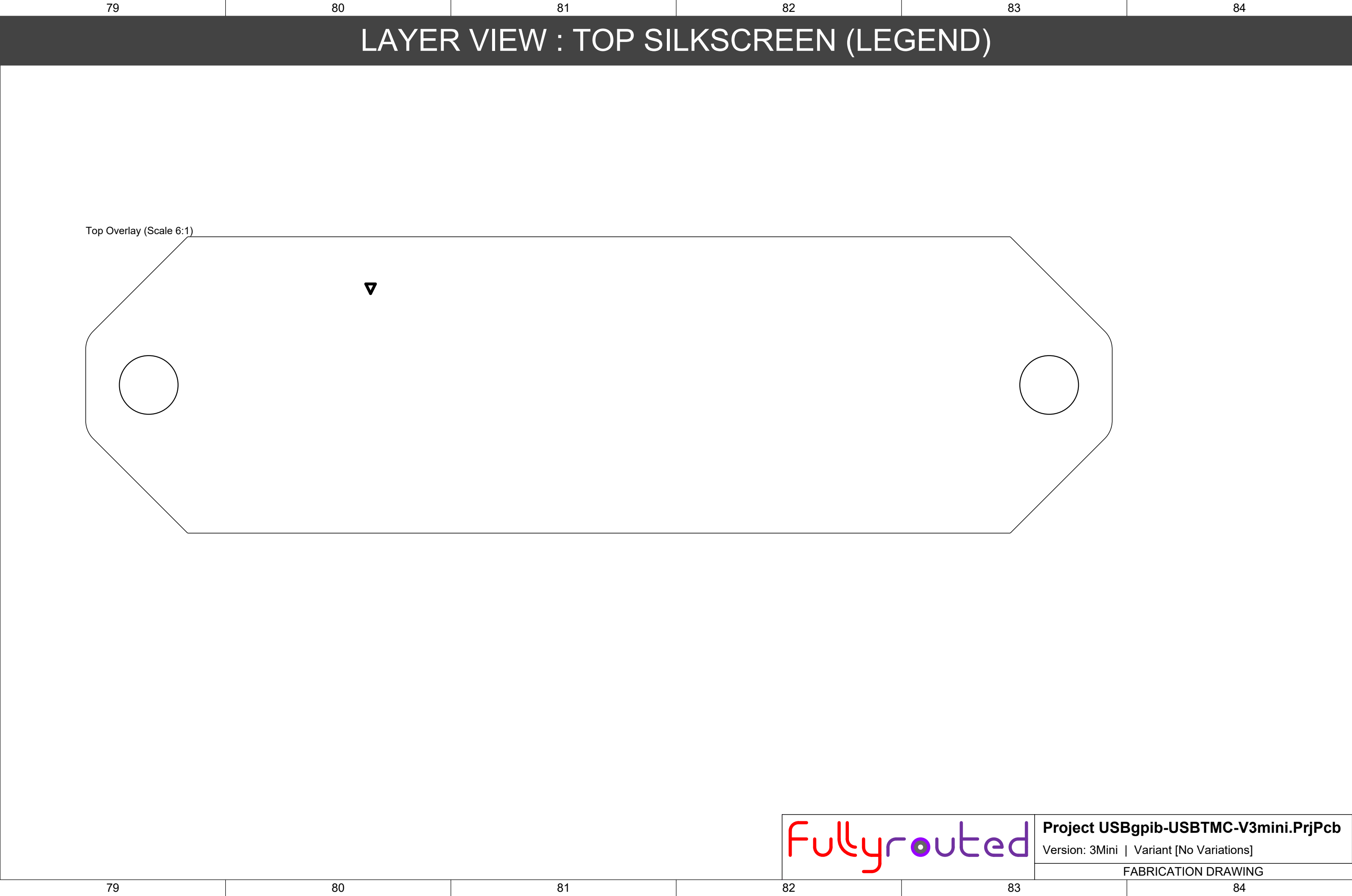
Top Solder (Scale 6:1)



LAYER VIEW : BOTTOM SOLDER MASK

Board Layer Stack Bottom Solder (Scale 6:1)





Project USBgpib-USBTMC-V3mini.PrjPcb

Version: 3Mini | Variant [No Variations]

FABRICATION DRAWING

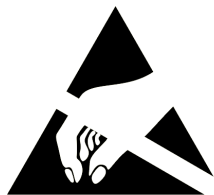


LAYER VIEW : BOTTOM SILKSCREEN (LEGEND)

Board Layer Stack Bottom Overlay (Scale 6:1)



GENERAL



Unless otherwise specified the following rules apply:

- 1. DO NOT DEVIATE FROM ARTWORK OR BOM WITHOUT PRIOR AUTHORIZATION.
- 2. ASSEMBLE AND INSPECT PER IPC-610 CLASS 2

Bill of Materials and Material Handling

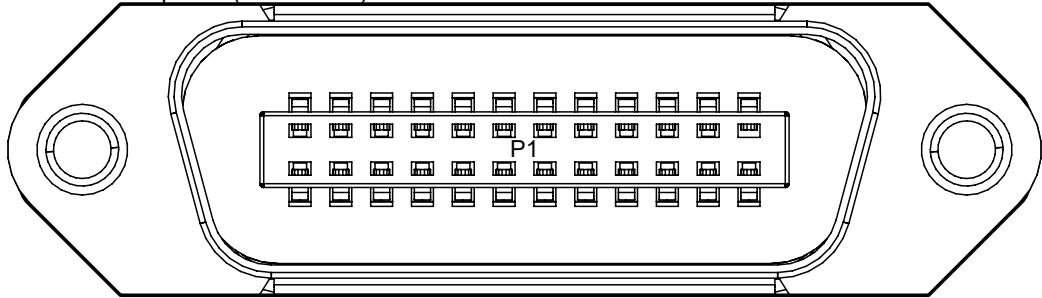
- 3. THE BOM CONTAINED IN THIS DOCUMENT IS AS-BUILT. NON-INSTALLED PARTS HAVE BEEN REMOVED. ADDITIONAL BOM FORMATS ARE AVAILABLE IN THE PROJECT FILES
- 4. ANY PART SUBSTITUTIONS MUST BE APPROVED IN WRITING BEFORE ASSEMBLY
- 5. ALL MATERIALS MUST BE PROCURED FROM MANUFACTURER AUTHORIZED DISTRIBUTORS OR THE ORIGINAL MANUFACTURER
- 6. ALL COMPONENTS AND BOARDS TO BE HANDLED AND STORED ACCORDING TO IPC GUIDELINES
- 7. ESD CONTROL PER IPC RULES

Soldering

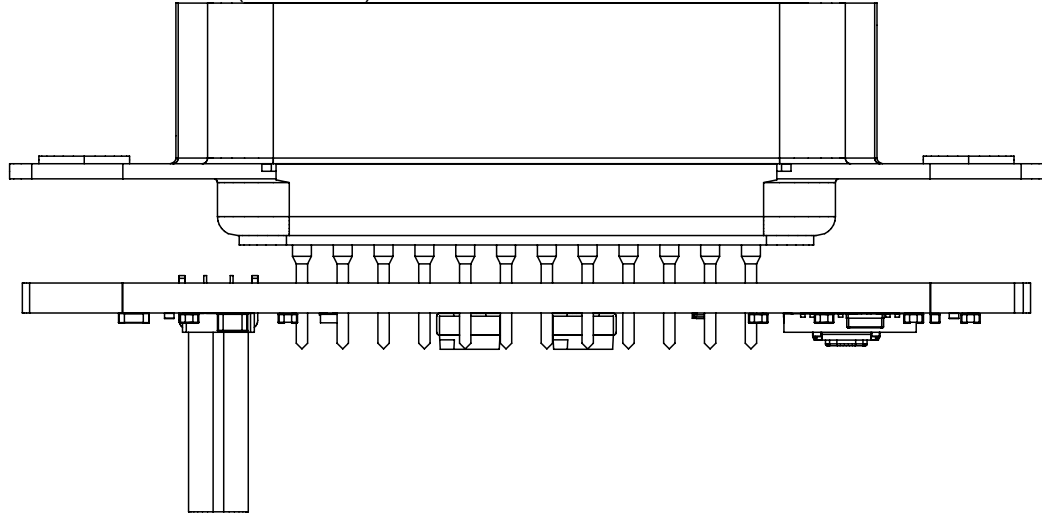
- 8. SOLDERING TO BE DONE USING SN37PB63 ALLOY USING ALLOY MANUFACTURER RECOMMENDED NO-CLEAN FLUX
- 9. BGA COMPONENTS WITH LEAD-FREE CONNECTIONS NEED TO BE REBALLED WITH SN63PB37. MIXING OF ALLOYS IS NOT PERMITTED.
- 10. SOLDERING PREFERRABLY TO BE DONE USING NITROGEN ATMOSPHERE
- 11. SURPLUS COMPONENTS TO VACUUM SEALED WITH DESSICANT IN ANTISTATIC BAGS
- 12. INCOMING MATERIAL (BOARDS AND COMPONENTS) NEEDS TO BE INSPECTED FOR HUMIDITY AND BAKED IF NEEDED PRIOR TO USE.
- 13. MANUAL REWORK / TOUCHUP TO BE DONE USING SAME ALLOY AND APPROPRIATE FLUX. FLUX MUST BE REMOVED.

2D VIEW

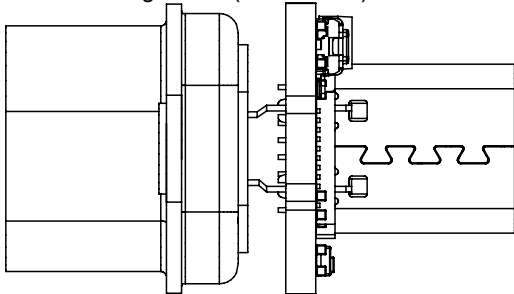
View from Top side (Scale 2.5:1)



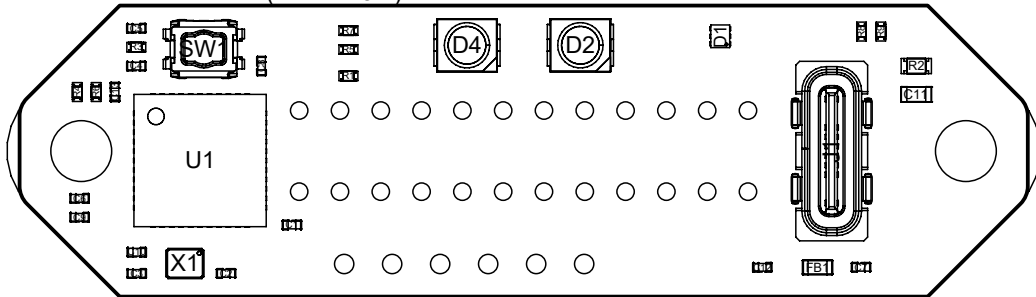
View from Front side (Scale 2.5:1)



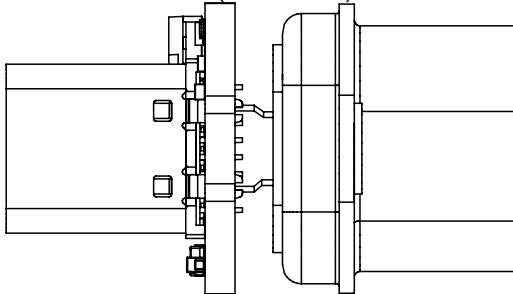
View from Right side (Scale 2.5:1)



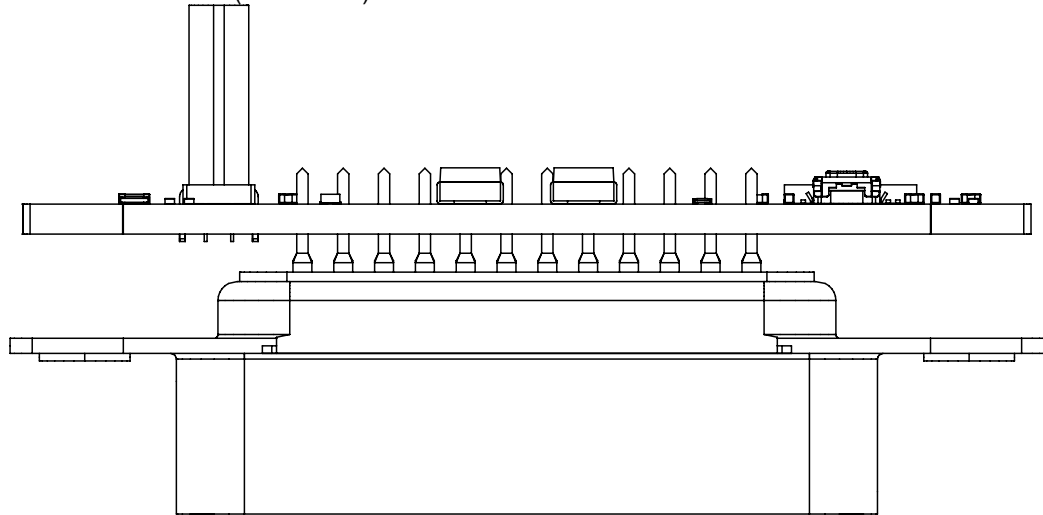
View from Bottom side (Scale 2.5:1)



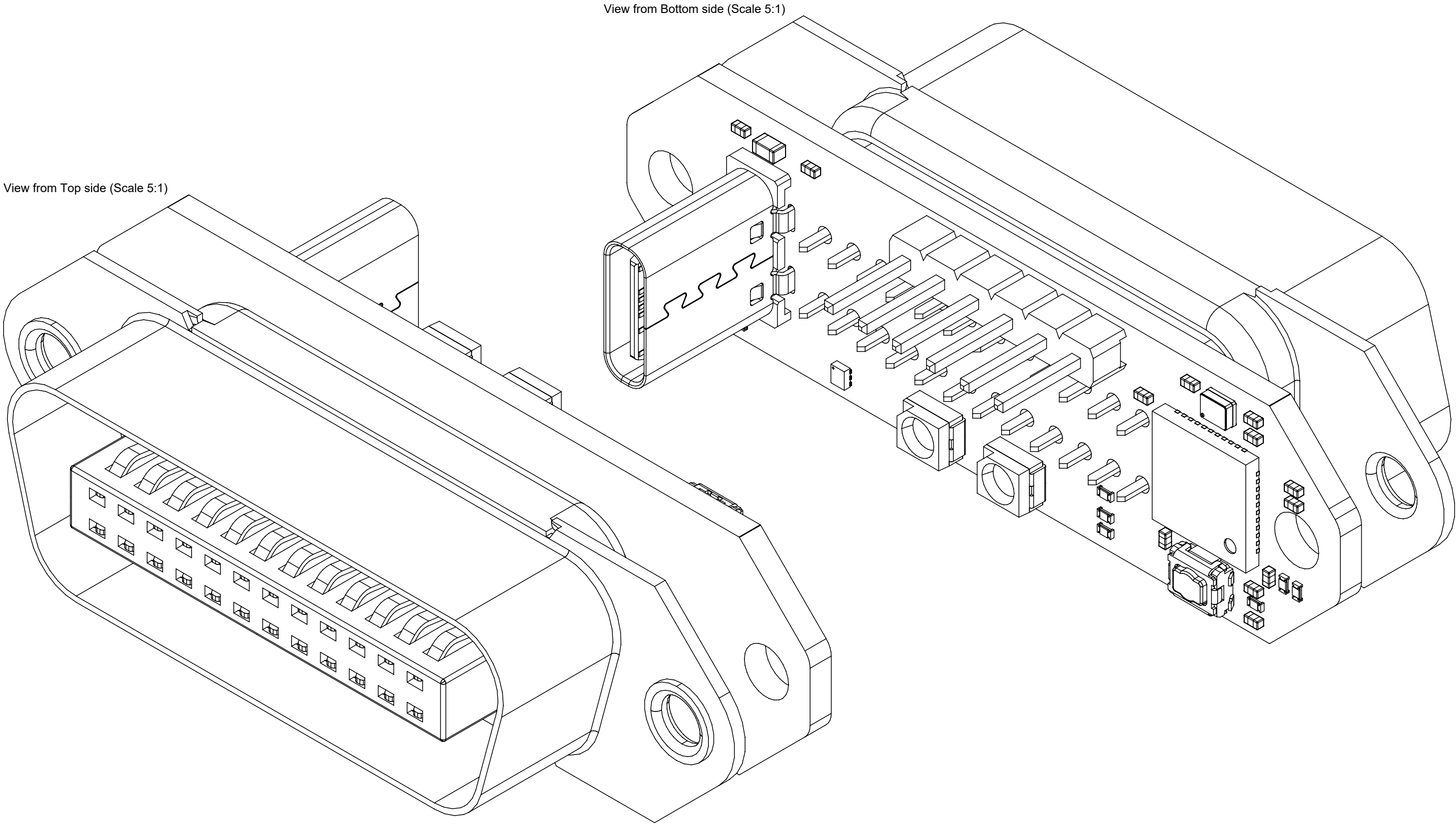
View from Left side (Scale 2.5:1)



View from Back side (Scale 2.5:1)



3D VIEW





A

A

B

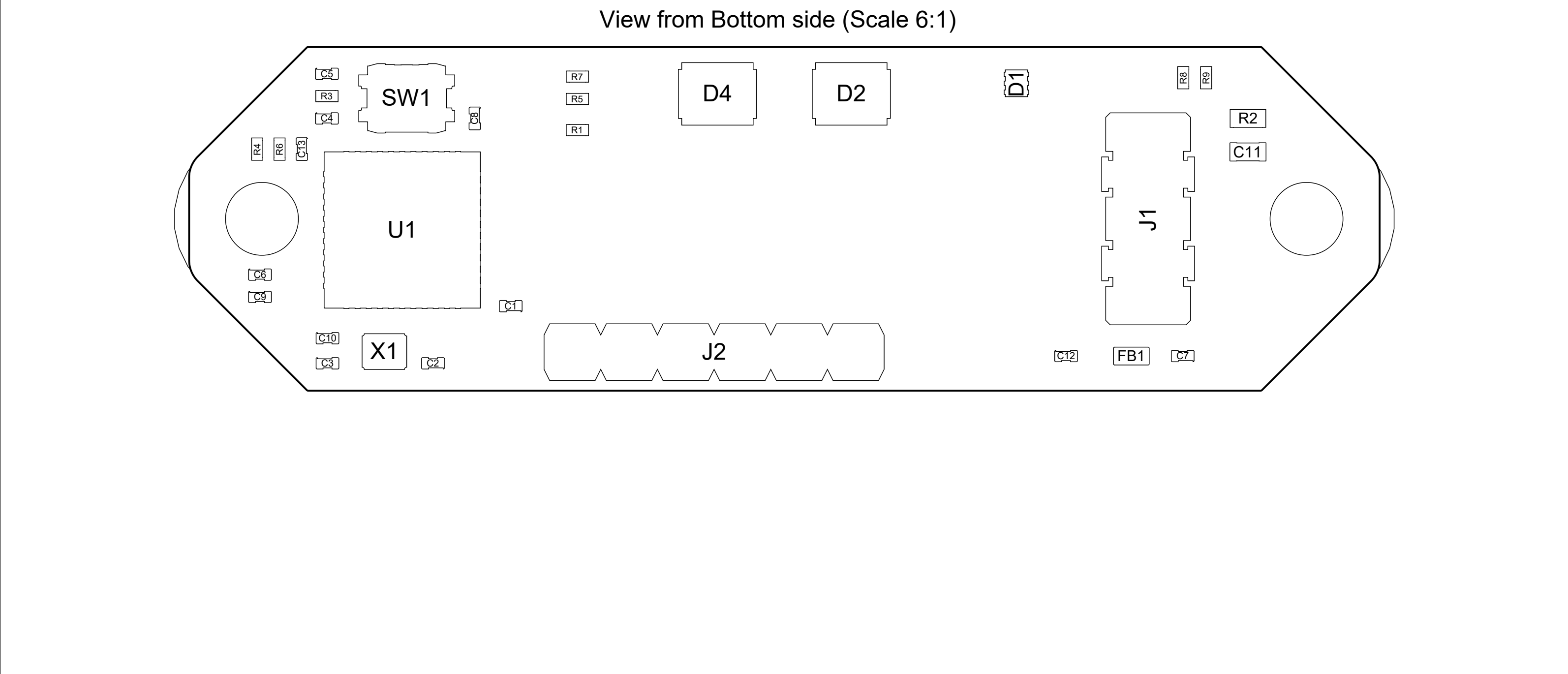
B

C

C

D

D



# PASTE MASK BOTTOM

The diagram illustrates the layout of a microprocessor chip. At the center is a large square core. Surrounding the core are various functional blocks: a horizontal row of four rectangular blocks at the top; a vertical column of four rectangular blocks on the right; a horizontal row of four rectangular blocks at the bottom; and a vertical column of four rectangular blocks on the left. Additionally, there are several smaller square and rectangular blocks scattered around the perimeter, representing control logic, cache, and I/O ports. The entire layout is enclosed within a hexagonal border.