555 Timer for Tiny Tapeout 6

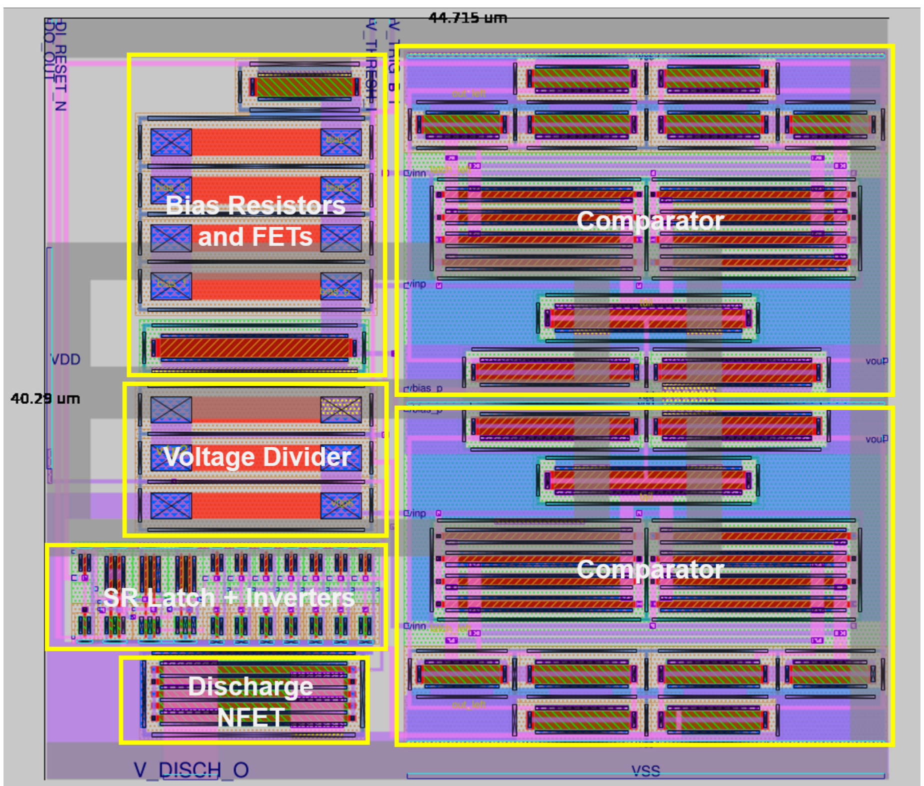
About

This project emulates the functionality of the classic 555 Timer IC.

Why

Blinking an LED using a 555-Timer has long served as the 'Hello World' for novice electronics enthusiasts. With the ongoing improvement in open-source tools and the emergence of communities like Tiny Tapeout, analog chip design is now within reach for hobbyists, hackers, and other free individuals. In light of this, I decided to take on the challenge of building my own 555 on an IC to blink an LED the hard way.

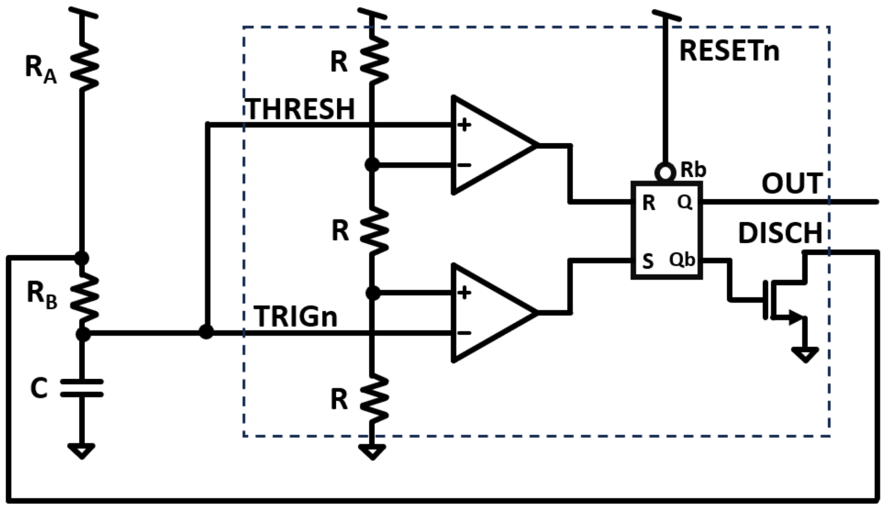
Layout



Operation

The 555 Timer is the most widely used analog IC ever made [1]. It was invented in the era of IC design when layout was still done by hand by cutting Rubylith.

Conceptually, a 555-Timer is nothing more than a couple of comparators, an internal voltage divider to set thresholds, an SR latch, and an open-drain transistor. It can be configured to be used in a variety of timer, delay, pulse generation, and oscillator applications.



In the figure above, the 555 Timer is configured as an astable multivibrator - a square-wave oscillator.

1. Suppose at startup the capacitor is at an initial voltage of 0V. S=H, R=L, Q=H, Qb=L.
2. The capacitor will begin to charge through a time constant given by $\tau_h = (R_A + R_B)C$.
3. When the capacitor crosses the $(1/3)V_{DD}$ mark, the bottom comparator will fire and: S=L, R=L, Q=Hold (H), Qb=Hold (L).
4. The capacitor continues to charge until it gets to $(2/3)V_{DD}$. The top comparator will fire and we get: S=L, R=H, Q=L, Qb=H.
5. The NFET is turned on, so the capacitor will immediately start discharging through a time constant $\tau_l = R_B C$.
6. As the capacitor voltage goes back below $(2/3)V_{DD}$, the top comparator will go low again. We have: S=L, R=L, Q=Hold (L), Qb=Hold (H).
7. The capacitor continues to discharge until it gets back down to $(1/3)V_{DD}$. The bottom capacitor will fire and we have: S=H, R=L, Q=H, Qb=L.
8. Now the NFET is off and the capacitor will begin charging again. As the capacitor begins charging we get: S=L, R=L, Q=Hold (H), Qb=Hold (L).
9. And the cycle continues.

Therefore, the frequency of oscillation and duty cycle are a function of the board designer's choice of RA, RB, and C.

The amount of time that OUT is high is given by:

$$t_1 = \frac{(R_A + R_B)C}{\sqrt{2}}$$

The amount of time OUT is low:

$$t_2 = \frac{R_B C}{\sqrt{2}}$$

And the overall frequency:

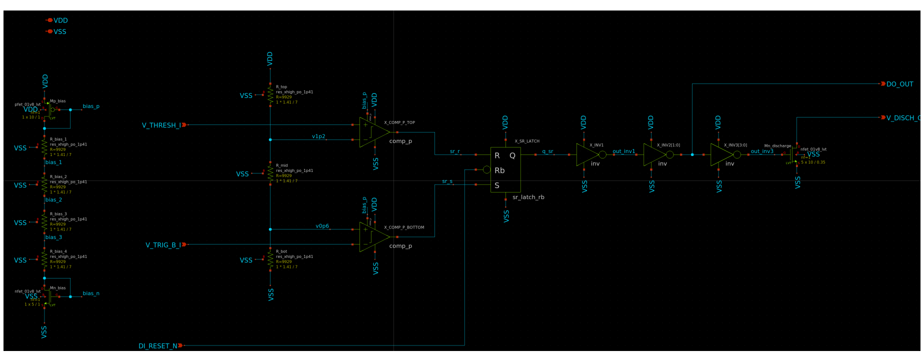
$$f = \frac{\sqrt{2}}{(R_A + 2R_B)C}$$

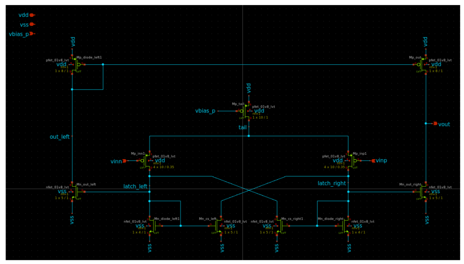
Schematics

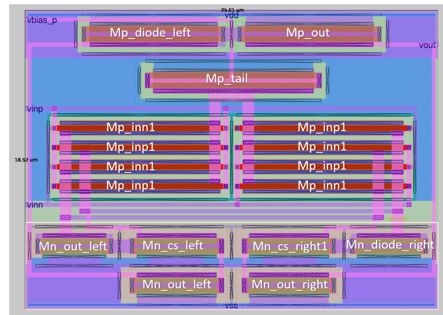
The basic functions described above can and have beeen implemented in different ways.

The original BJT version and later CMOS counterpart with actual sizing given by the creator himself are given in History.

The tt06_555 implementation is shown below:







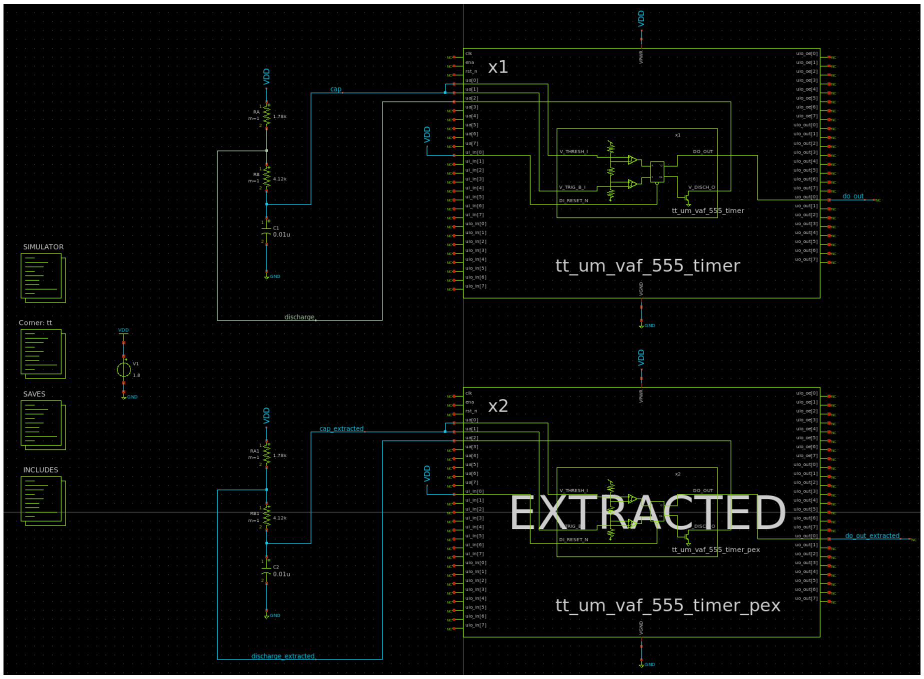
Simulation and Post-Layout Verification

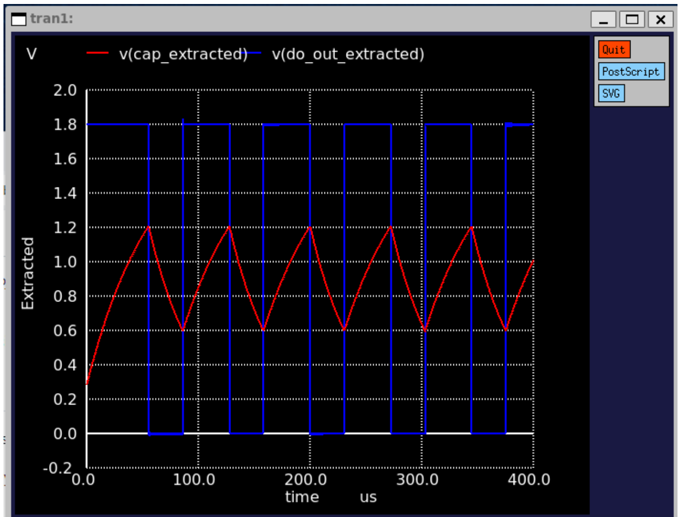
Below is a top-level testbench with the tt06_555 configured in the oscillator mode described earlier. This testbench compares the outputs of the schematic vs. the full RC extracted netlists.

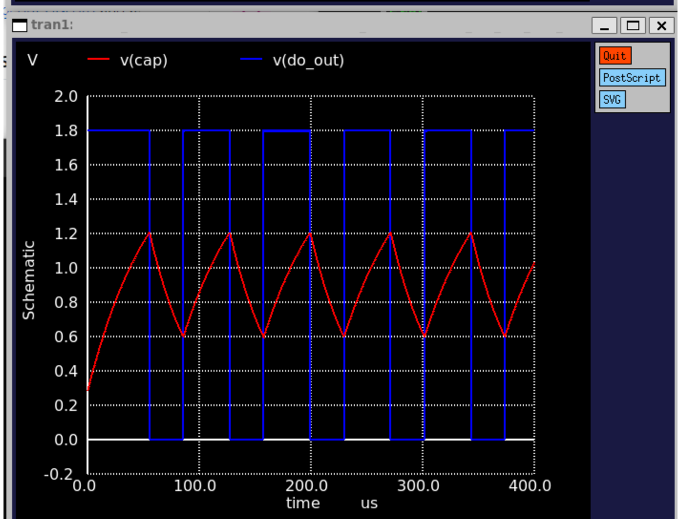
$$R_A = 1.78k\Omega$$
$$R_B = 4.12k\Omega$$
$$C = 0.01\mu F$$

From the earlier analysis with the values chosen above, we expect:

$$t_1 = 40.89\mu s$$
$$t_2 = 28.55\mu s$$
$$f = 14.37kHz$$


x1
tt_um_vaf_555_timer
x2
EXTRACTED
tt_um_vaf_555_timer_pex
SIMULATOR
Corner: tt
SAVES
INCLUDES
VDD
GND
cap
discharge
do_out
cap_extracted
discharge_extracted
do_out_extracted
1.78k
4.12k
0.01u






```
v1#branch                         -0.000761565

 Reference value :  3.93499e-04
No. of Data Rows : 4160
thigh               =  4.168814e-05 targ=  2.713503e-04 trig=  2.296
tlow                =  3.032069e-05 targ=  3.016710e-04 trig=  2.713
thigh_ext           =  4.169980e-05 targ=  2.724086e-04 trig=  2.307
tlow_ext            =  3.056850e-05 targ=  3.029771e-04 trig=  2.724
--------------------
Output High Schematic [seconds]: 4.16881E-05
Output Low Schematic [seconds]: 3.03207E-05
Frequency Schematic [Hz]: 13887.2
--------------------
Output High Extracted [seconds]: 4.16998E-05
Output Low Extracted [seconds]: 3.05685E-05
Frequency Extracted [Hz]: 13837.3
--------------------
ngspice 104 ->
```

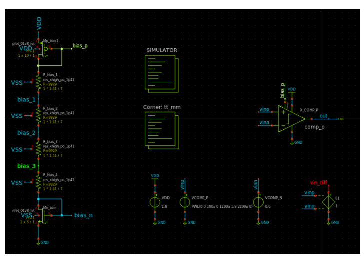
The frequency measurement between the simulated schematic and the simulated extracted RC netlist match closely, as shown above.

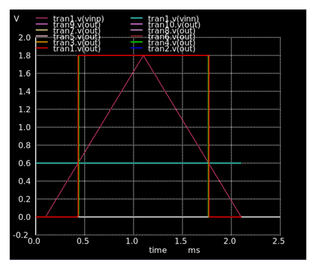
If you'd like to run the top-level simulation, simply do the following:

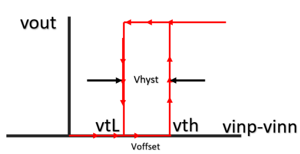
```
cd ~
mkdir projects
cd projects
git clone git@github.com:vincentfusco/tt06_555
cd tt06_555/xsch
xschem ./tb/tt_um_vaf_555_timer/tb_tt_um_vaf_555_timer_astable.Schematic
```

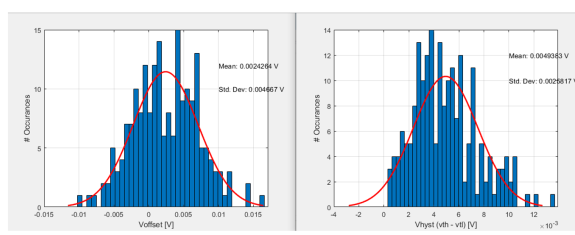
Comparator

The comparator could also be used stand-alone in another application. Below a Monte Carlo simulation is run and the offset and hysteresis at TT around a 0.6V threshold are measured, showcasing some of the nice open-source toolflow and PDK capabilities now available:



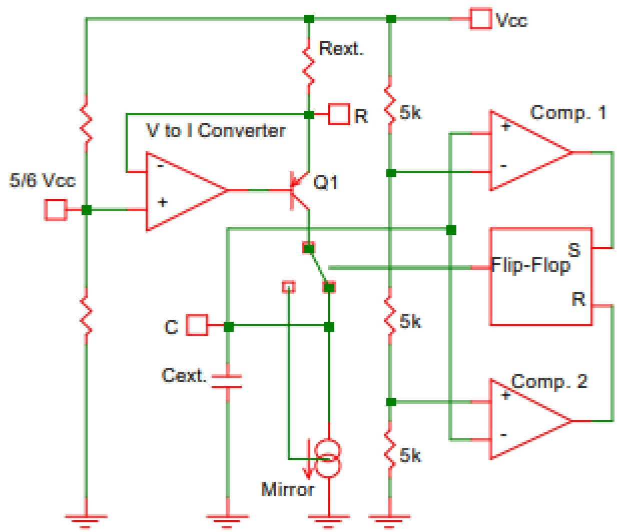




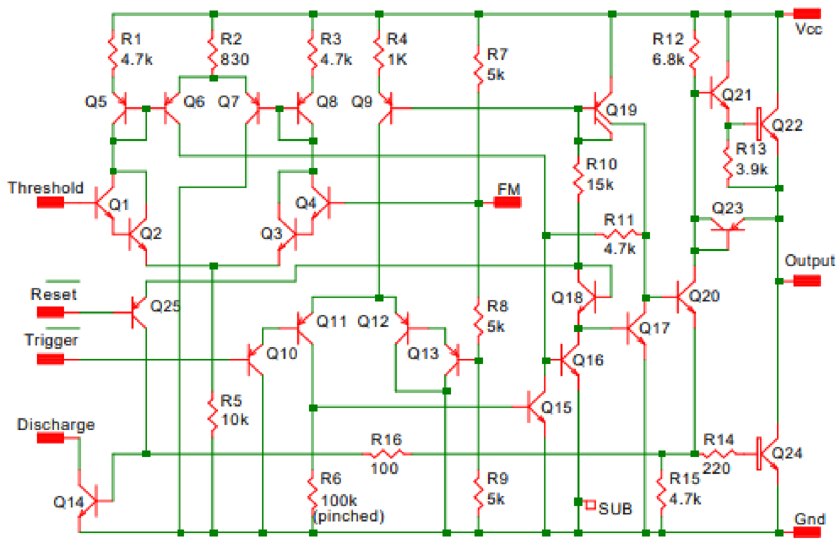


History

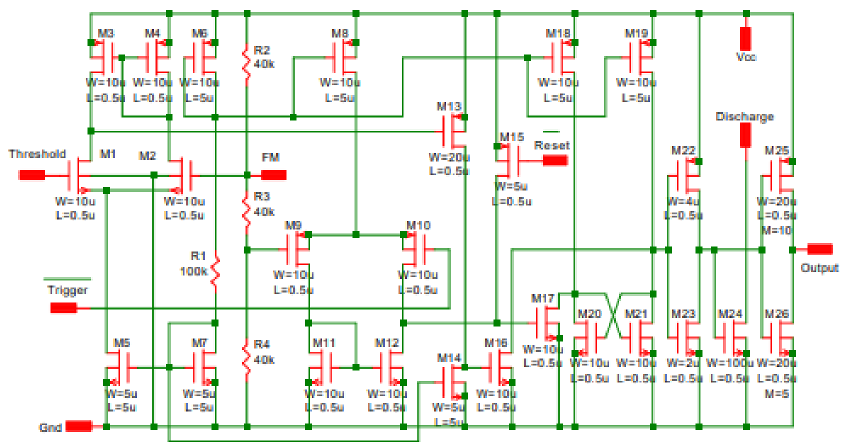
The predecessor was the NE566 Voltage-Controlled Oscillator:



The voltage-to-current source wasn't actually needed. The 555 was born:



A 5V-CMOS verion was later created.



The free e-book written by original inventor, Hans Camenzind, can be found at [2].

References

[1] https://computerhistory.org/blog/hans-camenzind-remembering-a-wizard-of-analog/

[2] http://www.designinganalogchips.com/.

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