

Vincent Fusco

Analog IC Designer | vincef@gmail.com | 202.705.3260 | US Citizen

Summary

Experienced circuit designer currently with AMD's Power Solutions group. Skilled in designing precision analog circuits for diverse applications ranging from spaceflight particle physics instruments to SoCs to guitar amplifiers to biomedical.

Expert in the Cadence Virtuoso suite and in the design of analog circuits such as op-amps, OTAs, comparators, LDOs, active filters, ADCs, DACs, switched-capacitor circuits, and voltage and current references. Comfortable taking circuit blocks from concept through requirements derivation, architecture, transistor-level design, and verification.

Work Experience

Advanced Micro Devices

Circuit Technologies

Aug 2022– Present

- Architected, designed and taped-out a new precision temperature sensor IP in TSMC 7nm FinFET CMOS.
- Sensor employed a Continuous-Time Delta-Sigma ADC for readout, and used precision analog techniques such as bitstream-controlled dynamic element matching (DEM), chopping, and digital curvature correction to obtain high accuracy and linearity with only a single-point trim.
- Achieved $< \pm 0.5$ °C temperature error (3σ) from -40 °C to 140 °C with single-point trim.
- Published a paper on the sensor in company-wide internal technical journal.
- Developed and taped-out an 8-bit 1.2GHz CDAC with switched capacitor filter targeting < 0.5 LSB DNL ($\pm 4\sigma$).
- Developed a novel push-pull linear regulator concept which utilized charge recycling and delta-sigma techniques to produce a half-rail voltage to act as a power supply & ground for thin-oxide power train switches and drivers in an Integrated Voltage Regulator (IVR). Invention disclosure submitted and patent application in process.

The Charles Stark Draper Laboratory

Analog IC Design Group

Nov 2020– Aug 2022

- Designed a fully differential instrumentation amplifier (INA), programmable gain amplifier (PGA), and SAR ADC buffer/driver for precision sensor readout and digitization in Intel 22nm FinFET technology.
- Developed a custom mixed-signal 1-3GHz Flash TDC for SoC clock monitoring.
- Designed and taped-out a low-power custom ASIC for a novel timing (10yr +) spacecraft application.

Johns Hopkins Applied Physics Laboratory

Space Science Electronics

May 2016– Nov 2020

- Led an R&D project (IRAD) to develop a new family of particle detector ASICs for NASA science instruments.
- Architected a 4-channel low-noise, solid-state detector readout IC for use in particle detector instruments.
- Designed many circuits including low-noise charge amplifiers, pulse-shapers, an ultra-low-current baseline holder, comparators, and a single-slope ADC.
- Held complete ownership of the project, managing CAD setup, process selection, specification definition, system architecture, transistor-level design, layout, tape-out, and testing. Taped out four test chips.
- Designs in flight include circuits currently en route to Jupiter on the Jupiter Icy Moon Explorer spacecraft, currently orbiting the sun on Parker Solar Probe, and en route to the asteroid Psyche.

Education

Johns Hopkins University

Master of Science – Electrical Engineering