Vineetha Govindaraj

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About Me
I am a graduate student working on computer architecture, datacenter power/performance and programming languages. I am looking for opportunities to engage myself in distributed systems research as a PhD student.

Research Interests
Computer Architecture

Compiler Technologies

Distributed Systems

Programming Languages

Skills
🏠 Programming and Scripting

    ✈ C, C++

    ✈ Python, Latex, Shell

🏠 Hardware Design/Verification

    ✈ System Verilog, UVM

    ✈ Synopsis VCS, Cadence SimVision

▤ Tools and APIs

    ✈ Apache Spark, lambda

    ✈ pthreads, sockets

    ✈ matplotlib, numpy, pandas, scikitlearn

▤ Architecture Simulators

    ✈ distributed gem5, McPAT

▤ Performance Measurement Tools

    ✈ Intel VTune, Linux Perf

Relevant Coursework
- Advanced Computer Architecture
- Advanced Compiler construction
- Advanced Operating Systems
- Cloud Computing
- Advanced Computer Vision
- Data Structures and Algorithms

Education

2018 – 2020   **Master of Science by thesis**   Pennsylvania State University
Focus:Computer Science and Engineering. CGPA: 3.65/4
Master Thesis
Advisors: Prof.Vijaykrishnan Narayanan,Prof.Mahmut Kandemier,Prof. Jack Sampson
Power management exploration for datacenter workloads

2011 – 2015   **Bachelor of Science**   National Institute of Technology,Trichy
Focus: Electronics and Comunication engineering.
Bachelor Thesis
Performance evaluation of an interconnect topology present in multicore processors.

Work Experience

Aug 2018 - May 2020   **Graduate Teaching Assistant**   Pennsylvania State University
Teaching assistant for introductory courses:Embedded systems, Python Programming, Computer Vision .

2016 – 2018   **Senior Hardware Engineer**   Samsung Semiconductors India Research
Developed testbench for Physical Layer of PCIe using UVM methodology for an in-house PCIe Verification IP particularly targeting link equalization, lane margining and retimers.Worked on verification of NVMe controller by developing scoreboards.

2015 – 2016   **Hardware Engineer**   Freescale Semiconductors India
Verified I2C and GPIO protocols for an ARM based SoC and performed code coverage.

Publications

2020   **PowerPrep: A power management proposal for user-facing datacenter workloads**   Submitted: ICCAD
Vineetha Govindaraj, Sumitha George, Mahmut Taylan Kandemir, Jack Sampson, Vijaykrishnan Narayanan
Analyzed the CPU utilization with a varying load on latency-critical datacenter workload Memcached. Based on this, developed a set of necessary conditions required in hardware for enabling deep sleep states in data centers while maintaining Service Level Objectives.

2020   **Fluid: A Framework for Approximate Concurrency via Controlled Dependency Relaxation**   Submitted: MICRO
*Huaipan Jiang, Haibo Zhang, Xulong Tang, **Vineetha Govindaraj**, Jack Sampson, Mahmut Taylan Kandemir, Danfeng Zhang*
Developed framework containing language and runtime extensions that allow for the expression of regions in source codes within which dataflow dependencies can be approximated. Identified execution patterns within workloads that are amenable to approximation and has increased performance under the framework.

Projects

2019   **Simple Parallel File System**   Operating Systems
Developed Parallel File System which provides access to file data striped across multiple file servers. Used Google Remote Procedure Calls(gRPC) for communication between client-server.

2019   **Comparative Study of Spark on EC2 and Lambda**   Cloud Computing
Analyzed execution time, cost and CPU Utilization of spark workloads running on EC2 and Lambda. Observed the run time behaviour of spark to understand collocation, network latency and memory access delays for Lambda and EC2.

2018   **ConfigNVPSim: NVP Simulator**   Advanced Computer Architecture
Developed a non-volatile processor(NVP) simulator: ConfigNVPSim, using Gem5 simulator.ConfigNVPSim simulates NVPs by throttling the progress of applications based on the energy harvested levels.

2015   **Performance Analysis of interconnect topology**   Bachelor's Thesis
Evaluvated performance of an interconnect topology present in multi-core processors. Used power, latency, throughput and area utilization as objectives to observe the performance of multicore interconnect topologies.