Lab 9 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

Lab Exercises	TA Initials	Score
Complete CPU design including updated schematic with caches (Pipeline + Caches + Memory)	_____	_____/02
Code for D-cache controller and CPU interface	_____	_____/02
Software Demonstrations		
caches (write test bench)	_____	_____/03
caches integrated with CPU:		
-*mult.asm*	_____	_____/03
-*fib.asm*	_____	_____/03
-*search.asm*	_____	_____/03
Synthesis Demonstrations		
caches integrated with CPU:		
-*mult.asm*	_____	_____/03
-*fib.asm*	_____	_____/03
-*search.asm*	_____	_____/03
Hardware Demonstration		
-*mult.asm*	_____	_____/05
-*fib.asm*	_____	_____/05
-*search.asm*	_____	_____/05
TA Grading script	_____	_____/40