Lab 8 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

Lab Exercises	TA Initials	Score
Block Diagram for Entire L1 Cache (I+D) (make sure to indicate clearly how each field in your cache block looks like, i.e. how many bits, and how your overall cache looks like, i.e. how many rows, columns, blocks and words, plus an example showing how CPU interface combinational logic works)	_____	_____/04
Code for I-cache controller and CPU interface	_____	_____/02
Software Demonstrations		
I-cache alone (write test bench)	_____	_____/03
I-cache integrated with CPU:		
-*mult.asm*	_____	_____/01
-*fib.asm*	_____	_____/01
-*search.asm*	_____	_____/01
Synthesis Demonstrations		
I-cache integrated with CPU:		
-*mult.asm*	_____	_____/01
-*fib.asm*	_____	_____/01
-*search.asm*	_____	_____/01
Hardware Demonstration		
I-cache integrated with CPU:		
-*mult.asm*	_____	_____/01
-*fib.asm*	_____	_____/01
-*search.asm*	_____	_____/01

TA Grading script	_____	_____/01

Question
What program behavior will
cause the I-cache to behave poorly?
Write pseudo code that will
behave as poorly as possible on a I-cache.
(HINT: loop) _____ _____/01