Lab 10 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

Lab Exercises	TA Initials	Score
Initial Dual-core memory hierarchy diagram (in moderate detail)	_____	_____/02
Completed top level VHDL code and Memory Arbitrator (Arbitrator connecting 2 pipelines, 4 caches, and 1 memory)	_____	_____/07
Parallel Sort Algorithm (use of LL/SC is required)	_____	_____/10
TA Grading script	_____	_____/01