# Lab 11 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

| **Lab Exercises** | TA Initials | Score |
|---|---|---|
| Complete Dual-core memory hierarchy diagram (in explicit detail, coherence signals and their names are required) as well as state diagrams of coherence controller (MSI) | _____ | _____/02 |
| Code for coherence controller (does not have to be fully functional, but fully VHDL implementation is required. testbench to this module is preferred for your own benefit. the following programs are fully parallel, only require an arbitrator/mux for memory access, which you have to get working for this week) | _____ | _____/07 |
| **Software Demonstrations** | | |
| -*dual.rtype.asm* | _____ | _____/05 |
| -*dual.loadstore.asm* | _____ | _____/05 |
| -*dual.mult.asm* | _____ | _____/05 |
| -*dual.llsc.asm* | _____ | _____/05 |
| TA Grading script | _____ | _____/01 |