Lab 5 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

Lab Exercises	TA Initials	Score
Initial CPU block diagram (your lab will not be acecpted if it does not contain a diagram), including pipeline registers and control signals	_____	_____/02
Modular design	_____	_____/01
VHDL code for top level, control unit stage registers and priorty mux	_____	_____/03
Pre-synthesis Tests		
-*test.ldst1.asm*	_____	_____/01
-*test.ldst2.asm*	_____	_____/01
Text file with list of hazard cases and stalls that can be encountered in the pipeline. (includes structural, data, and branch hazards.)	_____	_____/01
Grading of submitted CPU design with TA Grading script	_____	_____/01