

Computer Organisation - II

Solⁿ1 a) Opcode Size = 8 bits, $2^8 > 150$

b) Address Size = $24 - 8 = 16$ bits

c) Maximum allowable memory = $2^{16} \times 24$ bits
Since 2^{16} address and each location can hold
24 bits maximum unsigned binary = $2^{24} - 1$

Solⁿ2 Clock speed is not only the factor by which we can decide that which is faster, other factors such as the system components (memory, buses, architecture) and instruction sets must also be taken into account. The system can be compared to each other on how long they take to complete to each other or on how long they take to complete these tasks.

Solⁿ3 Given 32 bit processor

16 bit External bus

8 MHz clock and

Bus cycle time 4 clock cycle

a) Since minimum bus cycle = 4 clock & 8 MHz

$$\text{Maximum Bus cycle rate} = \frac{8}{4} = 2 \text{ MHz}$$

Data transferred per bus cycle = 16 bit = 2 B

Data transfer per second = Bus Cycle Rate \times Data provided cycle

$$= 2 \text{ M} \times 2$$

$$= 4 \times 10^6 \text{ B/Sec}$$

b) Now CLK Speed = $8 \times 2 = 16$ MHz
Maximum Bus cycle rate = $\frac{16}{4} M = 4M$ / sec

Data transferred per bus cycle = 16 bit = 2B
Data " " Second = Bus Cycle Rate x Data per bus
= $4M \times 2$
= $8 \times 10^6 B/Sec.$

c) Data transferred per ~~bus~~ bus = ~~32~~ bit cycle
: 32 bit = 4B

Data transfer per Second = $2M \times 4$
= $8 \times 10^6 B/Sec$

d) According to formula there is no change in Data transfer per second if we double the CLK Speed or make external bus 16 bit to 32 bit.
Both will work as a same.

Soln) i) Direct EA = 400

ii) Relative = PC + Direct Address Value = $502 + 400$
= 902

iii) Register indirect = 200

iv) Indexed Address = Regular Indirect + Direct Address

$$\begin{aligned} &= 200 + 400 \\ &= 600 \end{aligned}$$

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b) Now CLK Speed = $8 \times 2 = 16 \text{ MHz}$
Maximum Bus cycle rate = $\frac{1}{16} \text{ m} = 4 \text{ m/sec}$

Data transferred per bus cycle = 16 bit = 2B
Data per second = Bus cycle Rate \times
Data per bus
= $4 \text{ m} \times 2$
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c) Data transferred per bus ~~bus~~ cycle : 32 bit = 4B
Data transfer per second = $2 \text{ M} \times 4$
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Sol
Q5.

$$R = 10011100$$

After ARS $\rightarrow 1100110$

After ASI $\rightarrow 00111000$ | overflow as a -ve change
1 to positive.

Sol Q

freq

Cycles

30%

6 cycles

50%

4 cycles

20%

3 cycles

$$\begin{aligned}
 CPI &= 0.3 \times 6 + 0.5 \times 4 + 0.2 \times 3 \\
 &= 1.8 + 2.0 + 0.6 \\
 &= 4.4
 \end{aligned}$$

Sol 7 Instruction = 1 million sum at 3 GHz

30% \rightarrow 4 clock

50% \rightarrow 3 clock

20% \rightarrow 5 clock

$$\begin{aligned}
 CPI &= 0.3 \times 4 + 0.5 \times 3 + 0.2 \times 5 \\
 &= 1.2 + 1.5 + 1 \\
 &= 3.7
 \end{aligned}$$

$$Time = \frac{1}{freq} = \frac{1}{3 \times 10^8} = 0.3 \times 10^{-9} \text{ sec}$$

$$\begin{aligned}
 Execution time &= N \times CPI \times Time \\
 &= 1 \times 10^8 \times 0.3 \times 10^{-9} \times 3.7 \\
 &= 11.1 \times 10^{-3}
 \end{aligned}$$

Sol 8. A micro operation is an elementary operation performed on information stored in one or more register.

Example shift, count, clear & load

- 1) Register transfer micro-operation transfer binary information from one register to another.
- 2) Arithmetic micro-operation perform arithmetic operations on ~~no~~ numerical data stored in registers.
- 3) Logic micro operations operation bit manipulation operation or non numerical data stored in registers.
- 4) Shift micro-operation perform shift micro operation perform on data