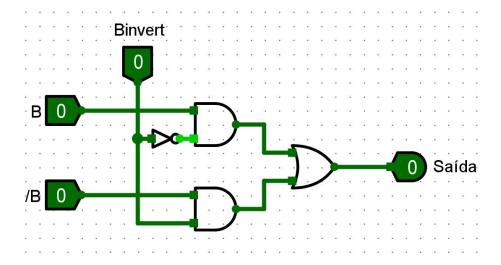
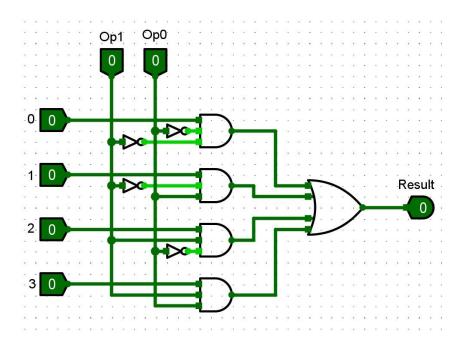
Aluno: Vinícius Figueiredo Ferreira, Matrícula 747482

Parte 1:

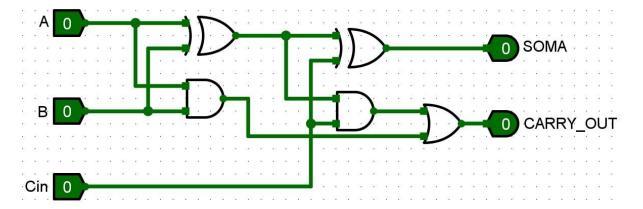
Mux 2x1:



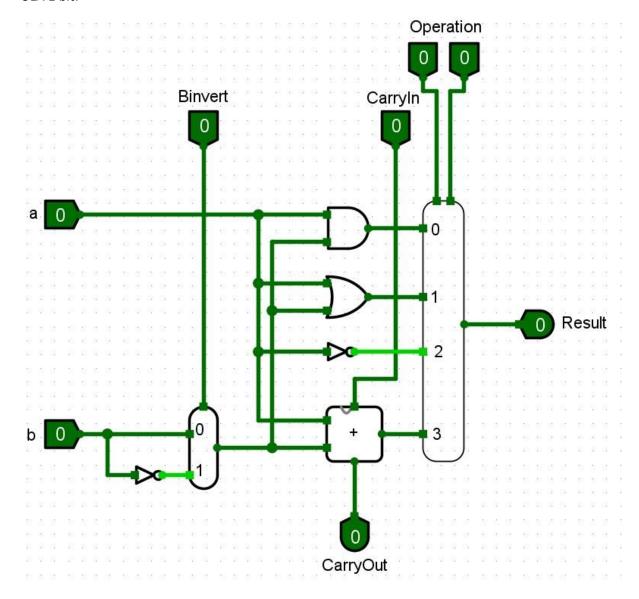
Mux 4x2:



Somador Completo:



ULA 1 bit:



ULA 4 bits:

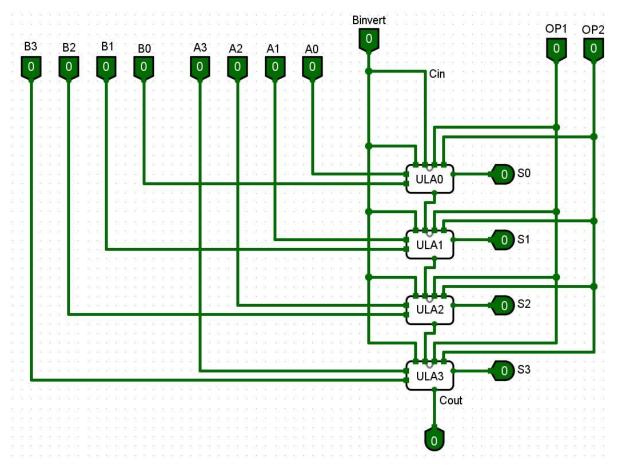


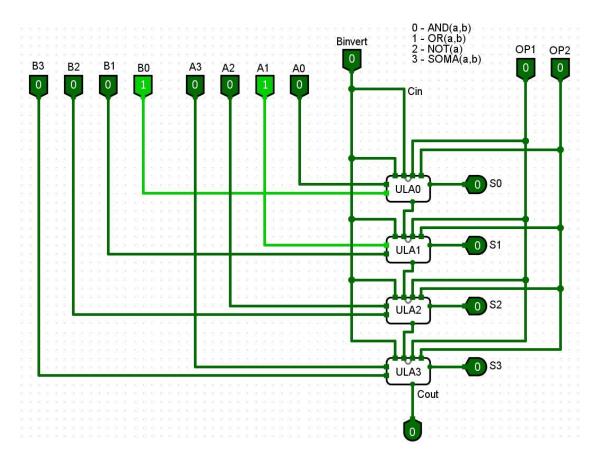
Tabela preenchida:

Instrução realizada	Binário (A, B,	Valor em Hexa	Resultado em binário
	Op.code)	(0x)	
AND(A,B)	0010 0001 00	(00 <mark>00 10</mark> 00 0100) = 0x084	0000
OR(A,B)	0010 0011 01	(0000 1000 1101) = 0x08D	0011
SOMA(A,B)	0010 0011 11	(00 <mark>00 10</mark> 00 1111) = 0x08F	0101
NOT(A)	1100 0011 10	(0011 0000 1110) = 0x30E	0011
AND(B,A)	1101 1100 00	(0011 0111 0000) = 0x370	1100

A=2; (ou A=0010)

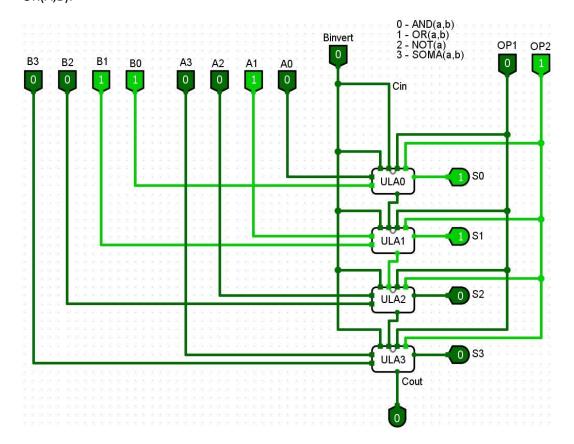
B=1; (ou B=0001)

AND(A,B):

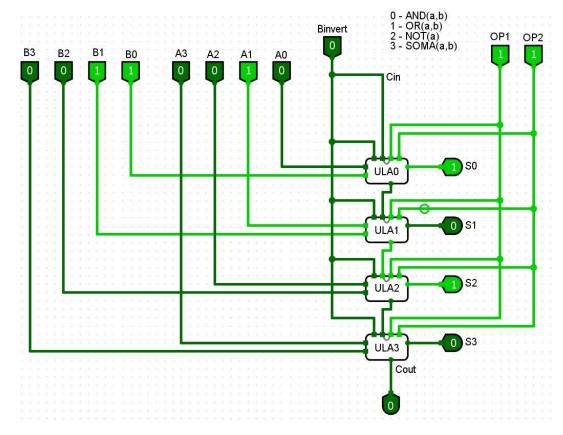


B=3; (ou B=0011)

OR(A,B):

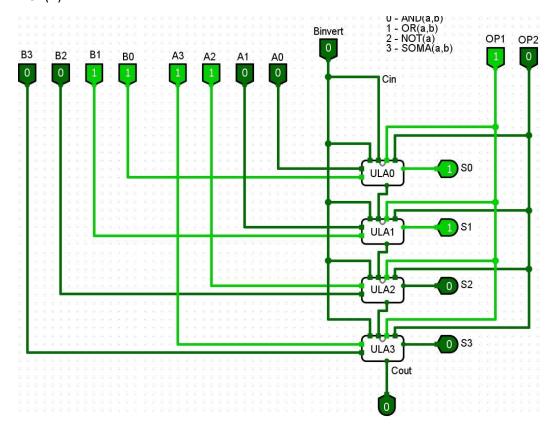


SOMA(A,B):



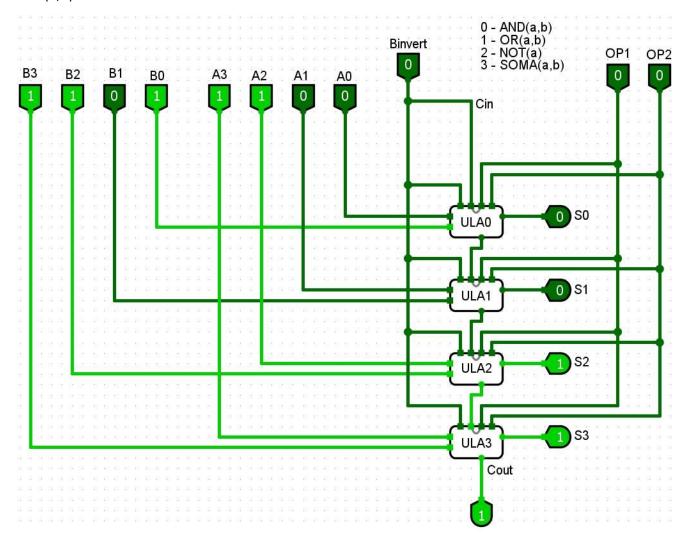
A=12; (ou A=1100)

NOT(A):



B=13; (ou B=1101)

AND(B,A):



Parte 2:

Instruções	Binário	Resultado da operação
450	0100 0101 0000	13
CB1	1100 1011 0001	0
A32	1010 0011 0010	1
C43	1100 0100 0011	0
124	0001 0010 0100	15
785	0111 1000 0101	7
9B6	1001 1011 0110	2
CD7	1100 1101 0111	0
FE8	1111 1110 1000	14
649	0110 0100 1001	13
D9A	1101 1001 1010	9
FCB	1111 1100 1011	12
63C	0110 0011 1100	15
98D	1001 1000 1101	15
76E	0111 0110 1110	7
23F 0010 0011 1111		2

Α

