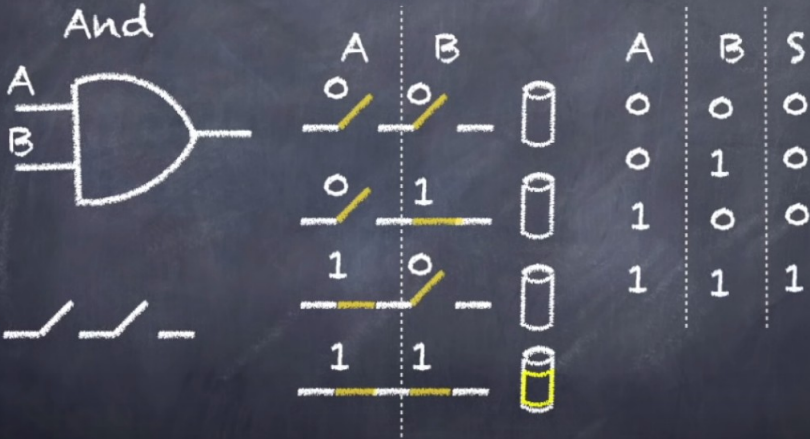


Portas Lógicas

Aula I - Expressões Booleanas, Circuitos Lógicos e Tabela Verdade

Antes de começar

And



The diagram shows an AND gate with inputs A and B. Below it, a truth table is presented with columns for A, B, and the output S. The rows represent all possible combinations of A and B (00, 01, 10, 11). The output S is 1 only when both A and B are 1.

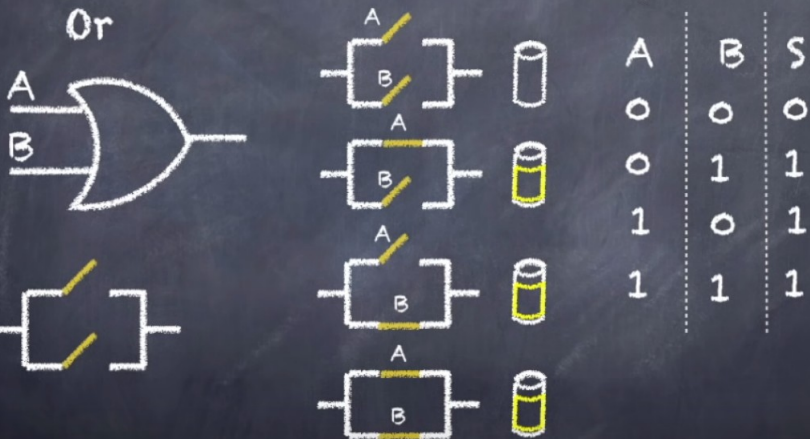
A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

3:48 / 25:25

Aula I - Expressões Booleanas, Circuitos Lógicos e Tabela Verdade

Antes de começar

Or



The diagram shows an OR gate with inputs A and B. Below it, a truth table is presented with columns for A, B, and the output S. The rows represent all possible combinations of A and B (00, 01, 10, 11). The output S is 1 for all combinations except when both A and B are 0.

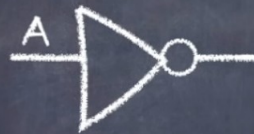
A	B	S
0	0	0
0	1	1
1	0	1
1	1	1

5:26 / 25:25



Antes de começar

Not



1

0

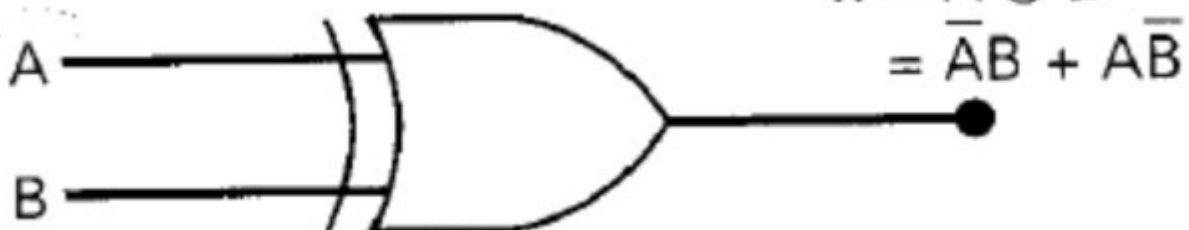
A	S	\overline{S}
0	0	1
1	1	0



6:12 / 25:25



A	B	x
0	0	0
0	1	1
1	0	1
1	1	0



Expressão booleana

1. $AB + (C + D)$ para valores de $A=0$, $B=1$, $C=0$, $D=1$

$$0 \cdot 1 + (0 + 1)$$

$$0 + (0)$$

$$0$$

Circuito lógico

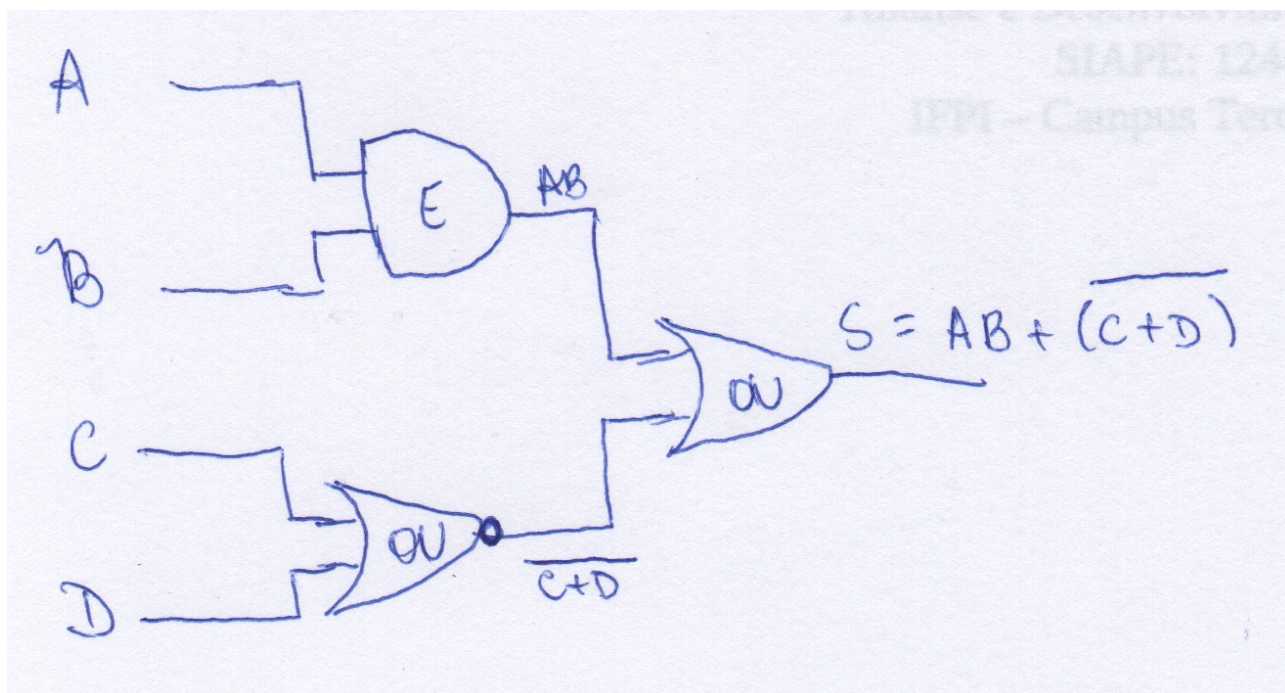


Tabela Verdade

A	B	C	D	AB	C+D	$\overline{C+D}$	S
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	1	1
1	0	0	1	0	1	0	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	0	0
1	1	0	0	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	1