A Prototype of a Narrowband Hybrid PLC/Wireless Transceiver

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Outlines

Introduction

Motivation

- There is a recent interest to turn electric power grids into smart grids (SGs) and to widespread the concept of Internet of Things (IoT).
- Power line communication (PLC) systems is one of the main data communication technologies for accomplishing or assisting this aim.
- On the other hand, wireless communication is also a remarkable alternative to constitute telecommunication infrastructures for SG and IoT.
- It is a common sense that SG and IoT will be supported by a wide range of data communication technologies, as no single solution fits all the expected scenarios.
- Recent researches are showing that these two technologies can bring improvements when combined, exploiting the existing diversity between PLC and wireless channels.

Introduction

Motivation

- There is a scarcity of works which comprehensive investigates PHY and link layers designs for maximizing the usage of the existing diversity among PLC and wireless channels.
- Prototype a testbed that is capable of demonstrating the advantages and disadvantages that hybrid data communication technologies may offer.

Introduction

Objectives

Then, this work addresses the prototype of a NB hybrid PLC/Wireless transceiver, which is based on a field programmable gate array (FPGA) device. The main objectives are:

- To discuss **adaptations and enhancements** which must be introduced in the IEEE 1901.2 Standard to allow its use as the core standard at the PHY layer and medium access control (MAC) sublayer of the NB hybrid PLC/Wireless transceiver. The adaptations are based on the **Hilbert transform**, which allows the recovery of the quadrature component of the received signal and performs carrier frequency offset estimation and correction. On the other hand, the enhancements are a **routing protocol** and an **error-correcting technique** that are implemented in a MAC sublayer level. The former allows us to introduce a hybrid data network based on the IEEE 1901.2 Standard that can cover more than one hop, while the latter can reduce packet error rates at the MAC sublayer level.

Introduction

Objectives

- To introduce and describe the **NB hybrid PLC/Wireless transceiver prototype**, which is constituted by a processor, PLC-analog front-end (AFE) (P-AFE), and wireless-AFE (W-AFE). Furthermore, to **analyze the performance of the used error-correcting technique** to recover received packets with error at the MAC sublayer, considering the IEEE 1901.2 Standard time constraints, in terms of hardware resource usage and time consumption. Also, to **evaluate the hardware resource usage** demands of an FPGA device, comparing NB PLC transceiver based on the IEEE 1901.2 Standard with the proposed NB hybrid PLC/Wireless transceiver.

Problem formulation

Approach I: PLC and wireless

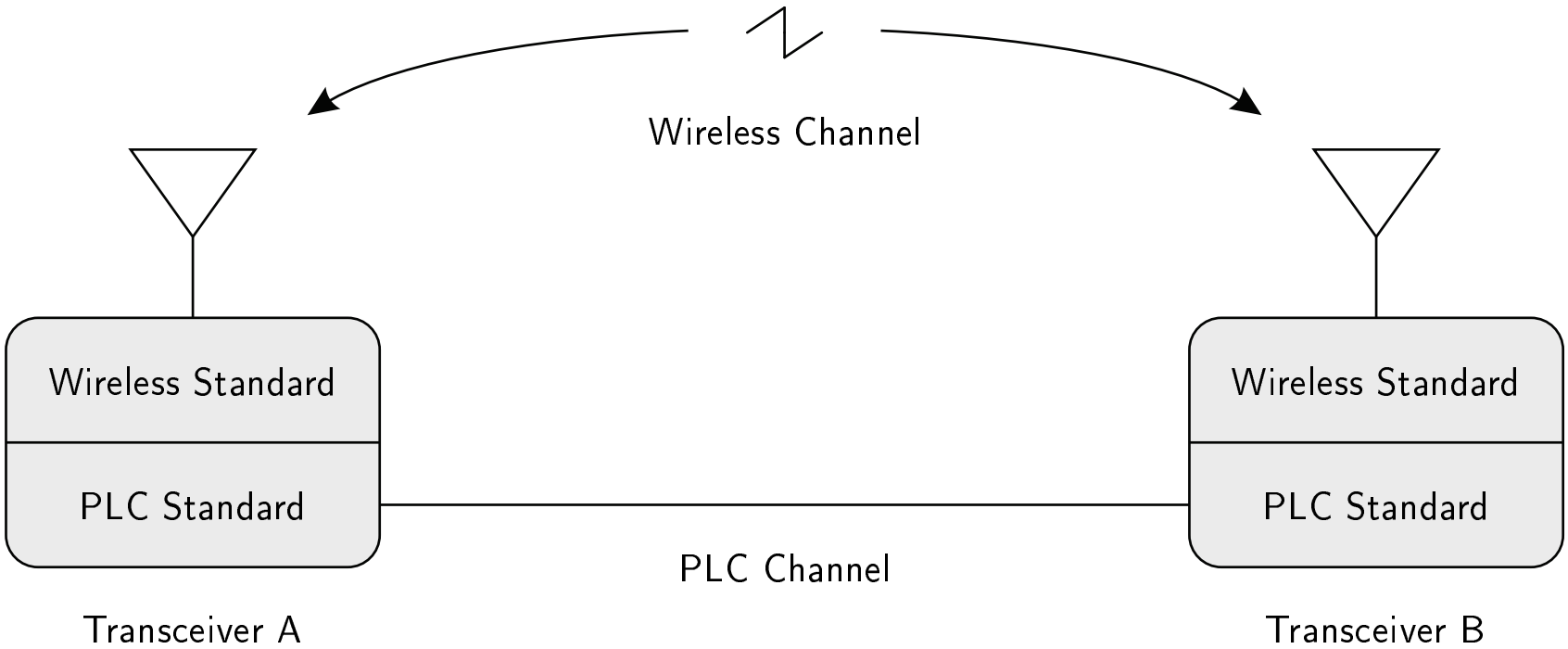


Figure: PLC and wireless approach.

Problem formulation

Approach II: hybrid

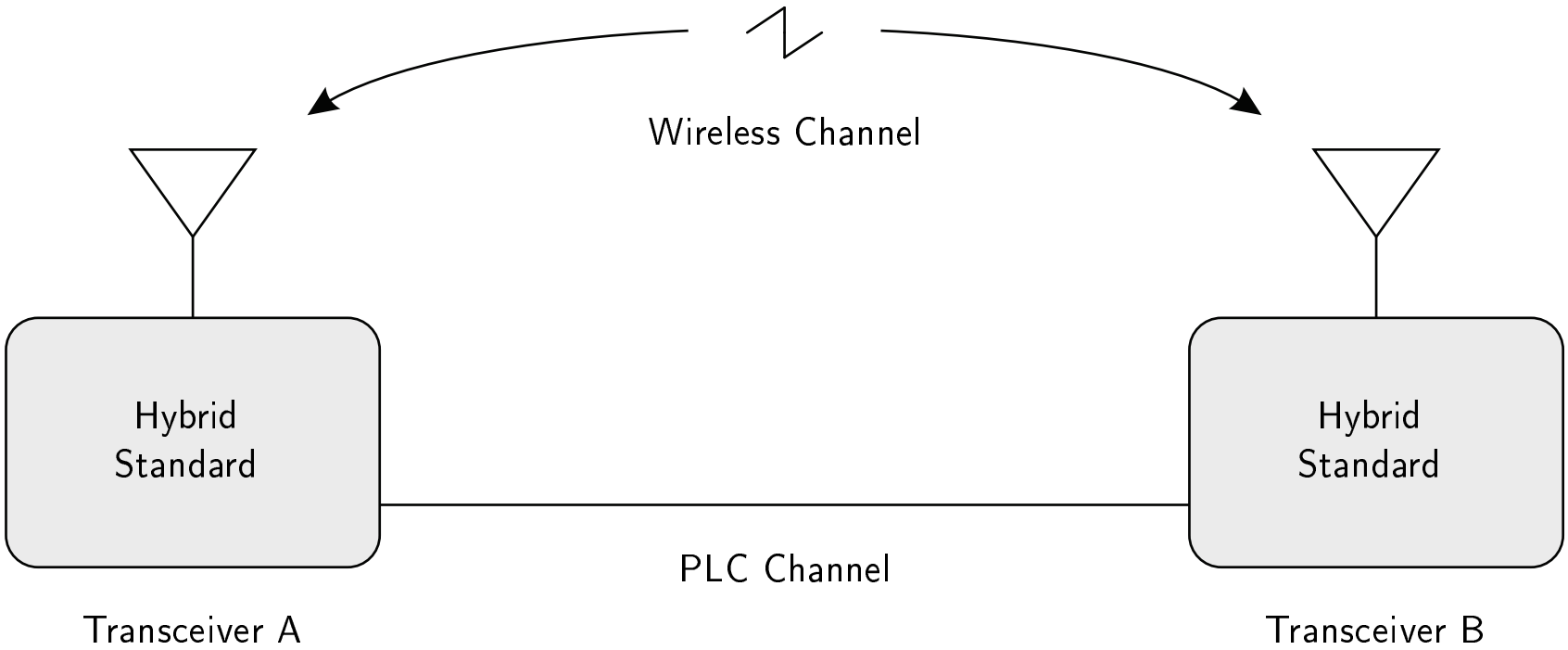


Figure: Hybrid approach.

Problem formulation

Approach III: wireless-only

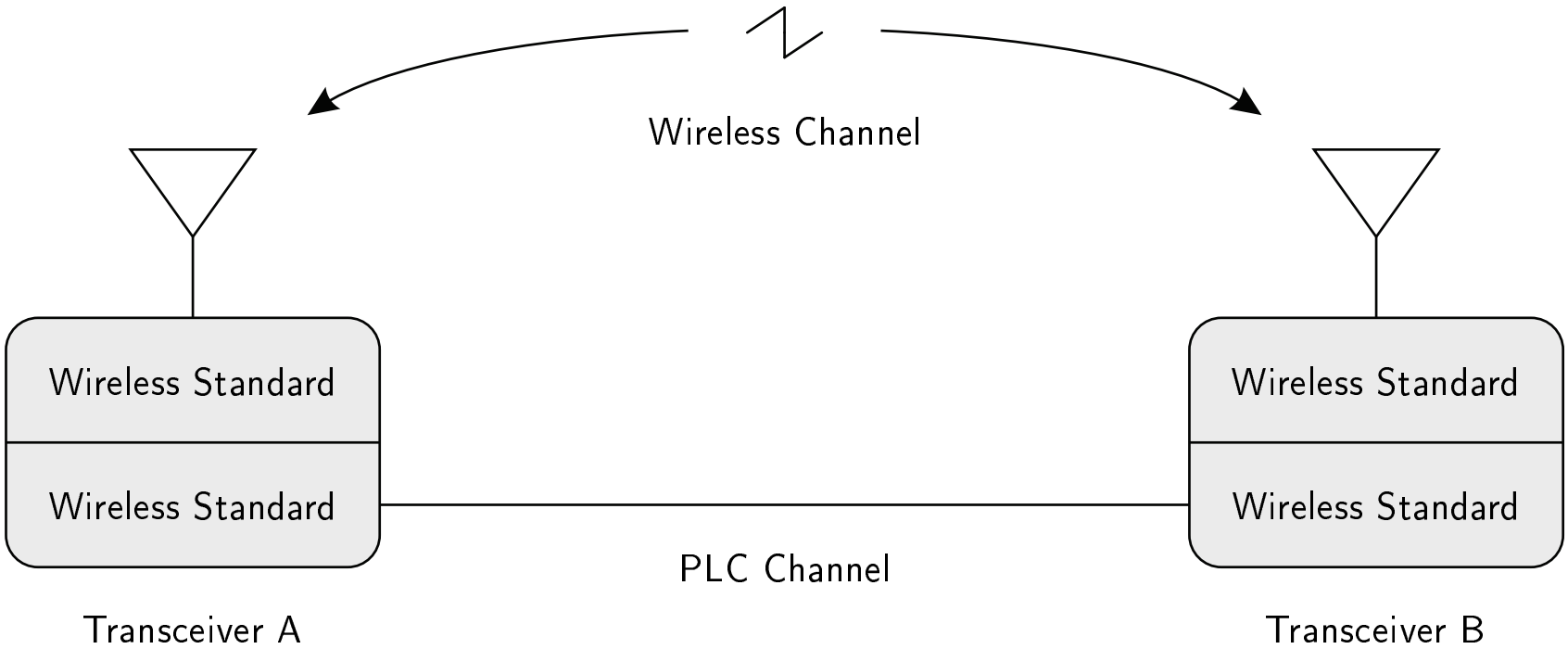


Figure: Wireless-only approach.

Problem formulation

Approach IV: PLC-only

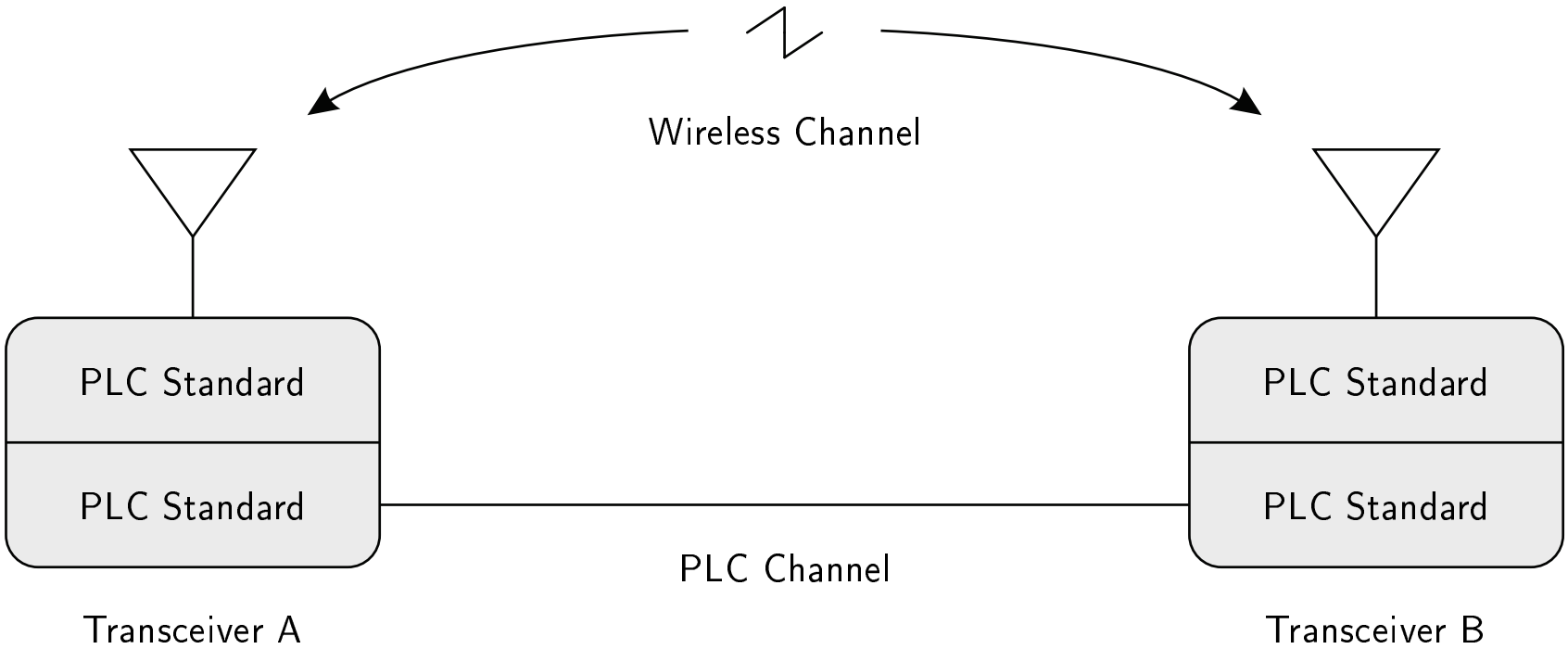


Figure: PLC-only approach.

Problem formulation

Analyzing the four approaches

- PLC-only seems to be an interesting choice for SGs and IoT applications.
- PLC channels are hostile $\Longrightarrow$ PLC standard is highly robust for providing data communication in comparison to the wireless one.
- In this regard, a NB-PLC standard is considered for implementing the NB hybrid PLC/Wireless transceiver prototype.

Problem formulation

Comparison and definition of the NB-PLC standard adopted

- Main candidates: PRIME, G3-PLC, ITU-T G.hnem, and IEEE 1901.2 Standard.
- Multicarrier scheme and OFDM-based.
- The IEEE 1901.2 Standard highlights:
  - Designed to support SG applications.
  - Can interoperate with PRIME and G3-PLC.
  - Achieve data-rates that attend SG and IoT applications.
  - IEEE's standards are well-accepted.

Problem formulation

Comparison and definition of the NB-PLC standard adopted

Based on the choice of the IEEE 1901.2 Standard to constitute the PHY layer and MAC sublayer of the proposed NB hybrid PLC/Wireless prototype, the following questions arise:

- Is that possible to adapt the IEEE 1901.2 Standard to make it the core data communication protocol of a NB hybrid PLC/Wireless technology?
- Which kind of changes must be implemented?
- Can it be prototyped?

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard

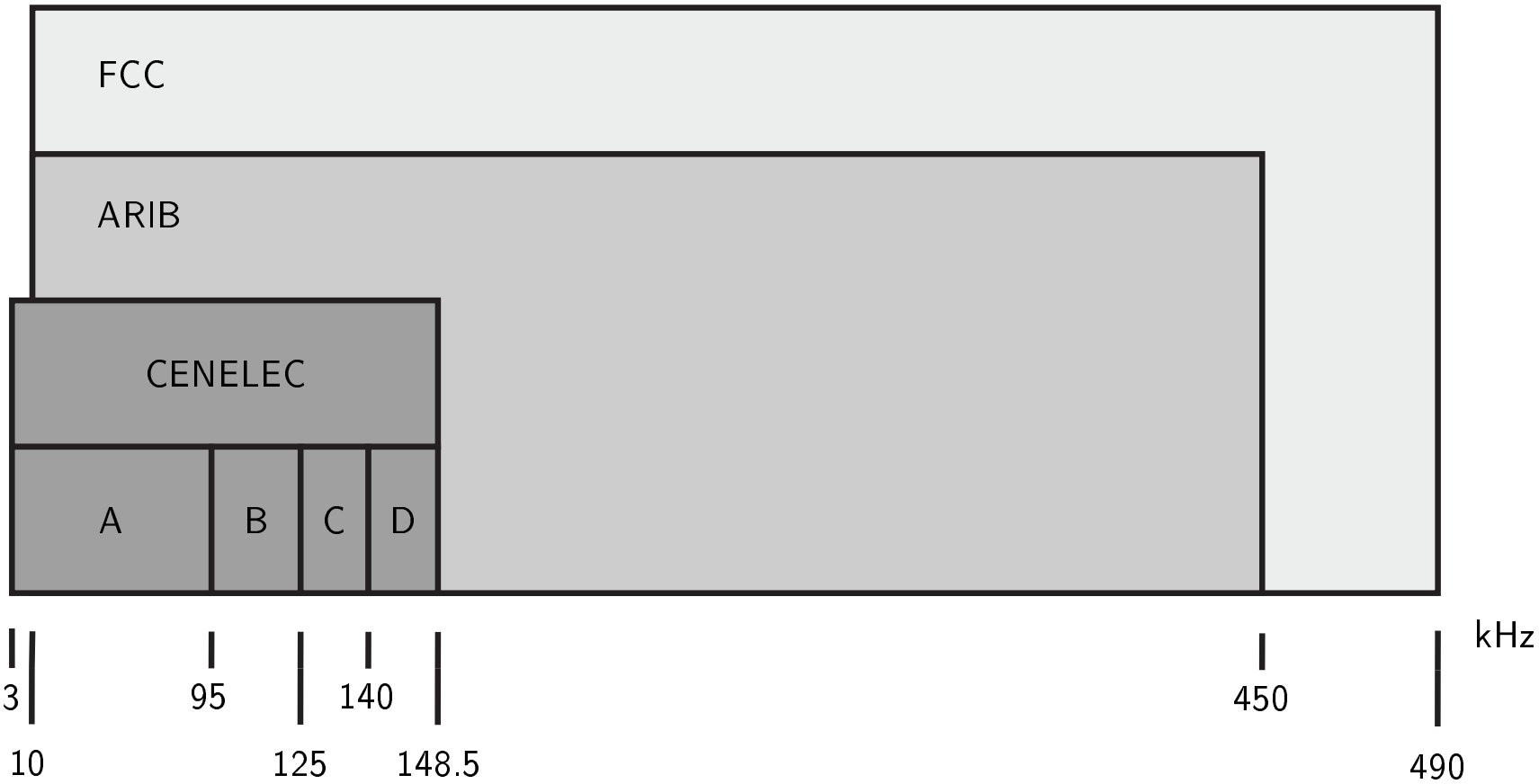


Figure: Regulatory frequency map

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - general information

Table: General information of the IEEE 1901.2 Standard.

Parameter	Details
Band plan	FCC
PHY frequency band (kHz)	10 to 490
Frequency sample (MHz)	1.2
FEC encoder/decoder	Scrambler/Unscrambler, Reed-Solomon encoder/decoder, convolutional encoder/decoder, repetition encoder/decoder, and interleaver/deinterleaver
OFDM modulator/ demodulator	Modulator/demodulator, mount symbol, IDFT/DFT, reorder DFT, add/remove CP, and windowing
Repetition encoder modes	Normal, ROBO, and S-ROBO

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - general information

Modulation	BPSK, DBPSK, DQPSK, D8PSK and optional QPSK, 8-PSK, 16-QAM
Cyclic prefix (samples)	30 or 52
Number of overlapped samples	8
Maximum subcarrier enable	72
Maximum OFDM symbols per frame	57
OFDM symbol length (samples)	256
Number of FCH bits per packet	72
Maximum valid bits of information per packet	1912
Time interval of one data symbol (μs)	232

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - general information

Time interval of one preamble symbol (μs)	213

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - general information

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - frame and packet structures

Figure: The frame structure in the PHY layer.

- Preamble: 9.5 or 13.5 symbols.
- FCH: 12 symbols.
- PSDU: up to 57 symbols.

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - frame and packet structures

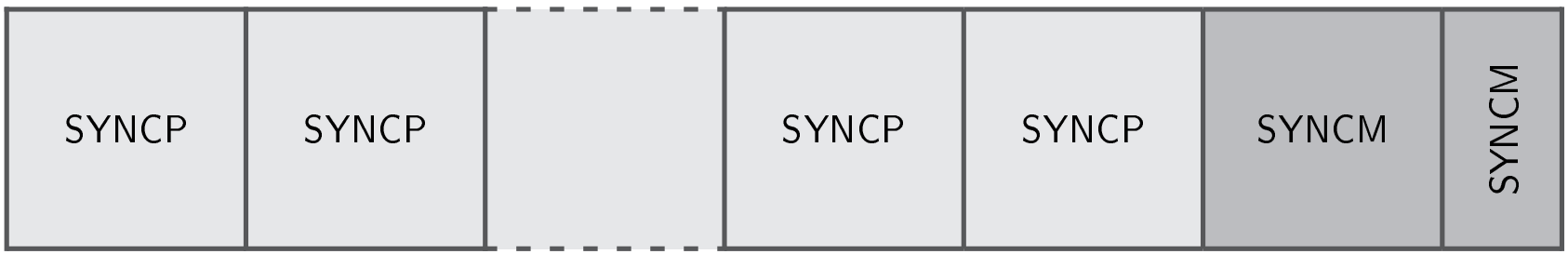


Figure: The structure of the preamble part.

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - frame and packet structures

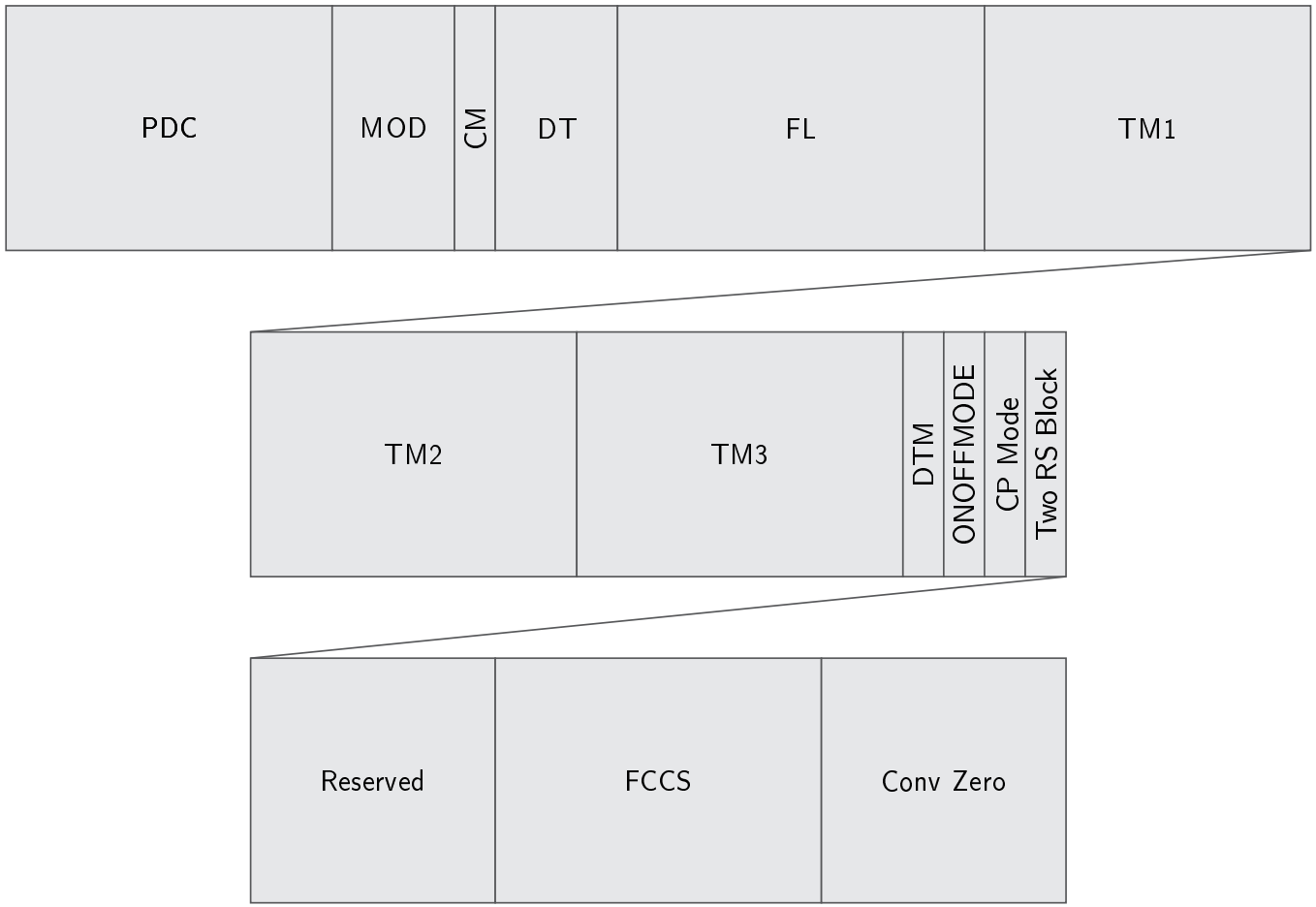


Figure: The structure of the FCH part.

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - frame and packet structures

PSDU:

- May or may not be present in the frame structure.
- Constituted by the MAC frame.
  - MAC header (MHR).
  - MAC payload.
  - MAC footer.
- MAC frame may be long enough to require segmentation.

The NB hybrid PLC/Wireless transceiver

The IEEE 1901.2 Standard - channel access control

- Carrier sense multiple access/collision avoidance (CSMA/CA) mechanism (protocol) with a random backoff time.
- This mechanism randomly spreads the transmission attempts of each node in a period of time.

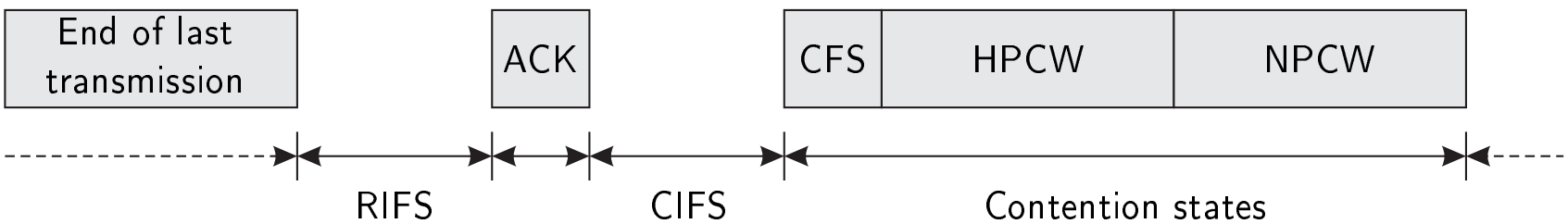


Figure: Priority contention Windows.

The NB hybrid PLC/Wireless transceiver

The block diagram of the NB hybrid PLC/Wireless transceiver

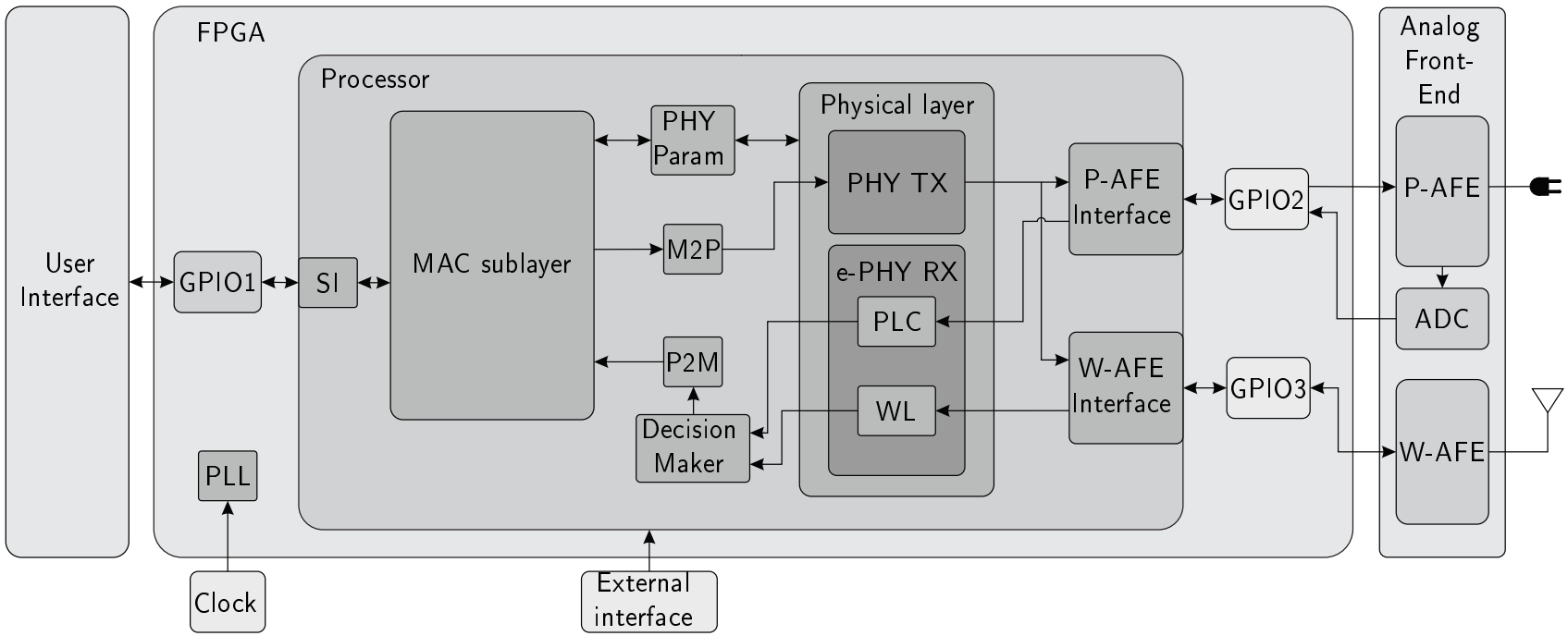


Figure: The block diagram of the proposed NB hybrid PLC/Wireless transceiver.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

- Feature incorporated in the IEEE 1901.2 Standard.
- It enables any node to work as a relay node.
- Alternative paths for accomplishing data communication among nodes that are not visible to each other.
- This feature rises the data network reliability $\Rightarrow$ increases the success of communication.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

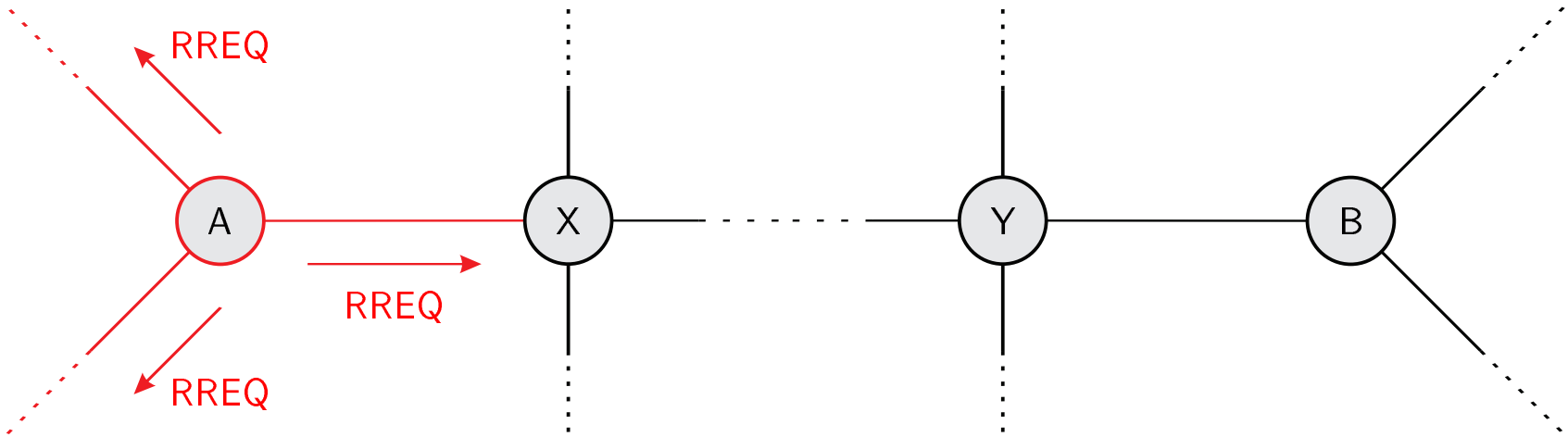


Figure: RREQ message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

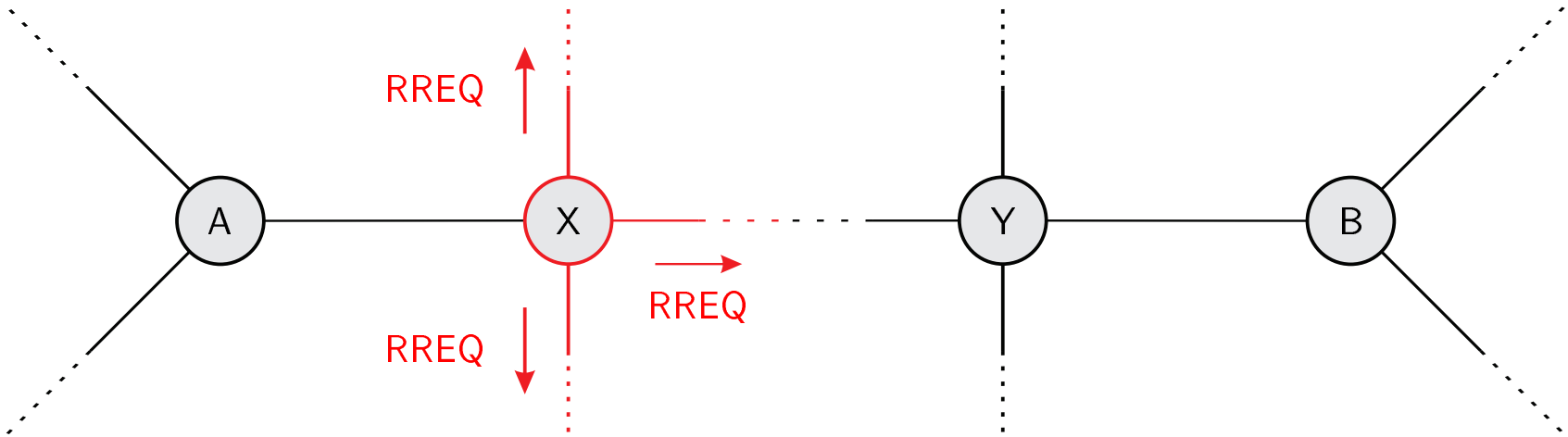


Figure: RREQ message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

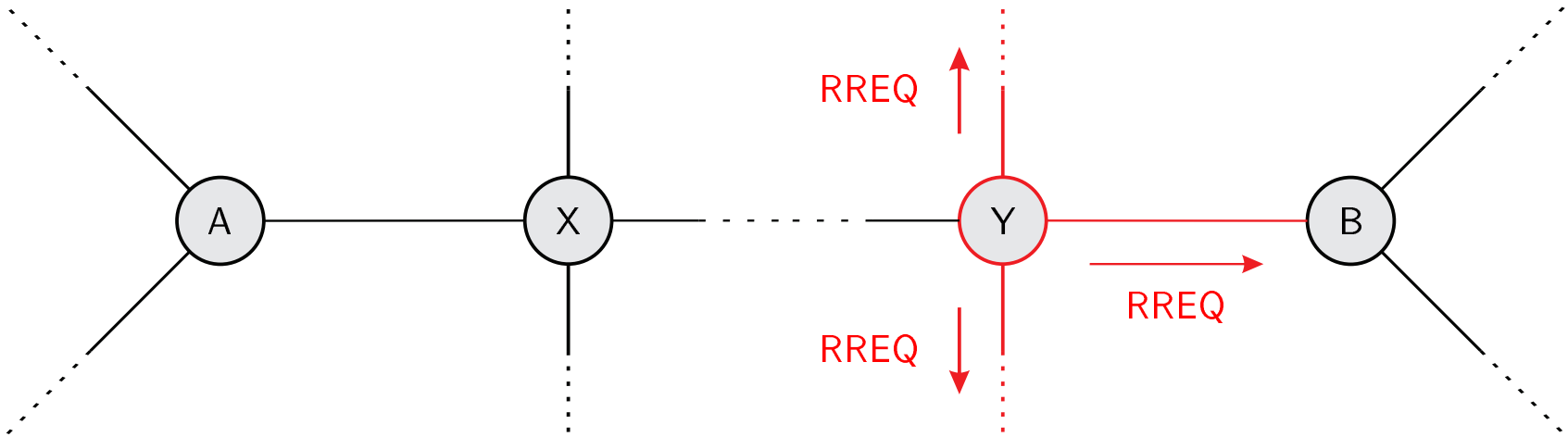


Figure: RREQ message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

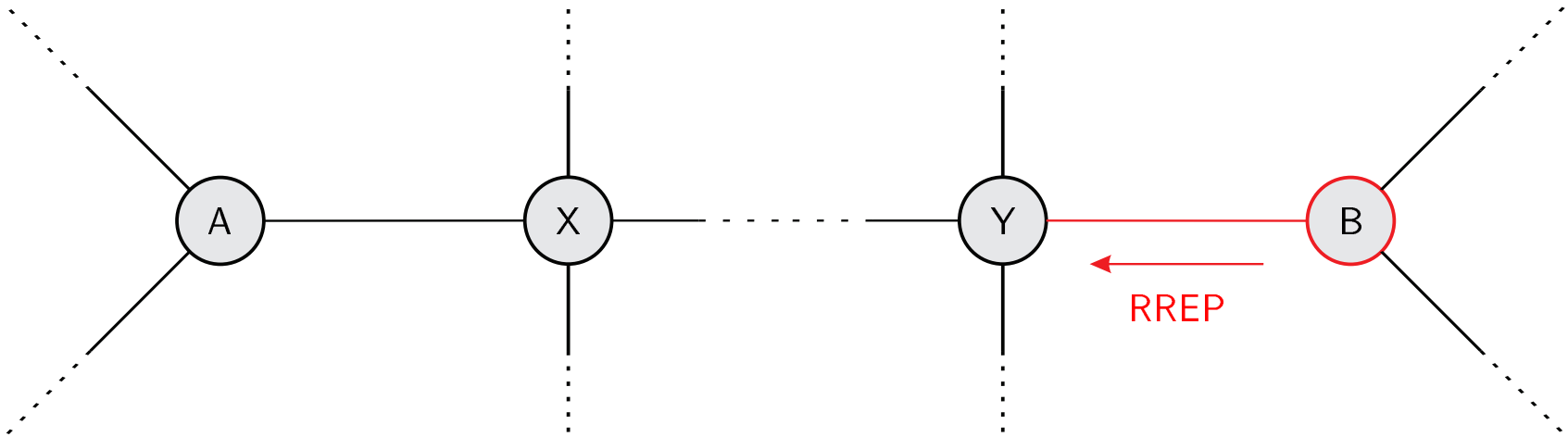


Figure: RREP message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

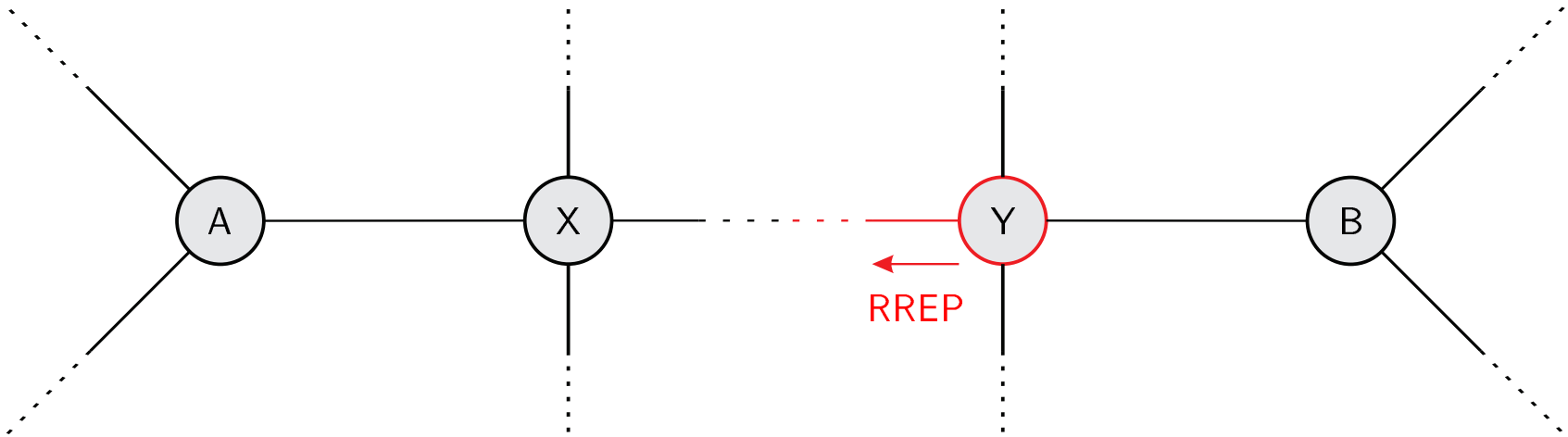


Figure: RREP message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

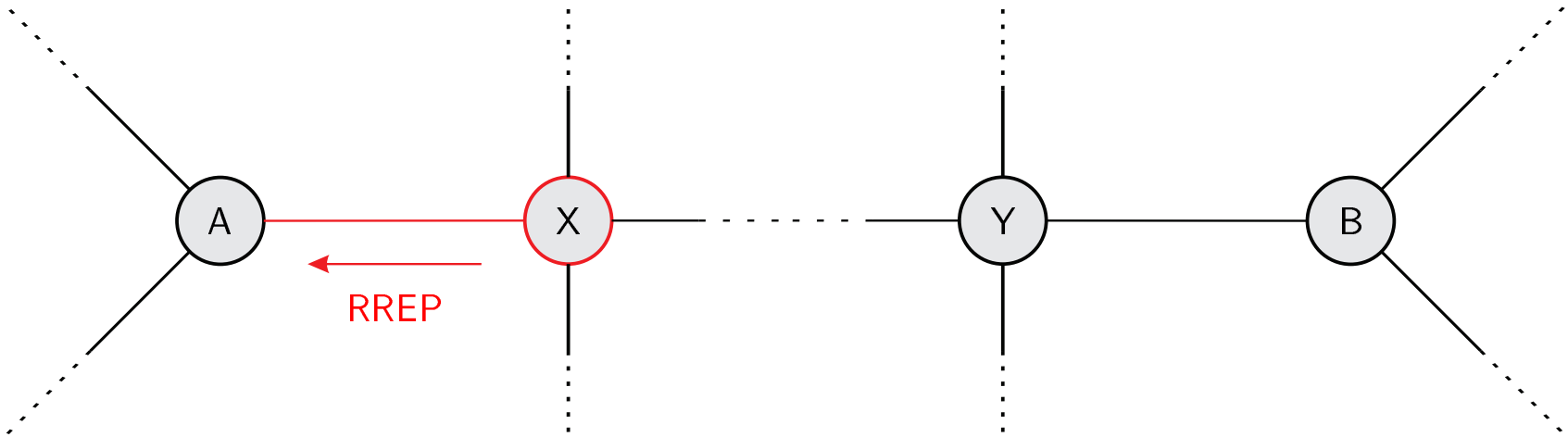


Figure: RREP message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

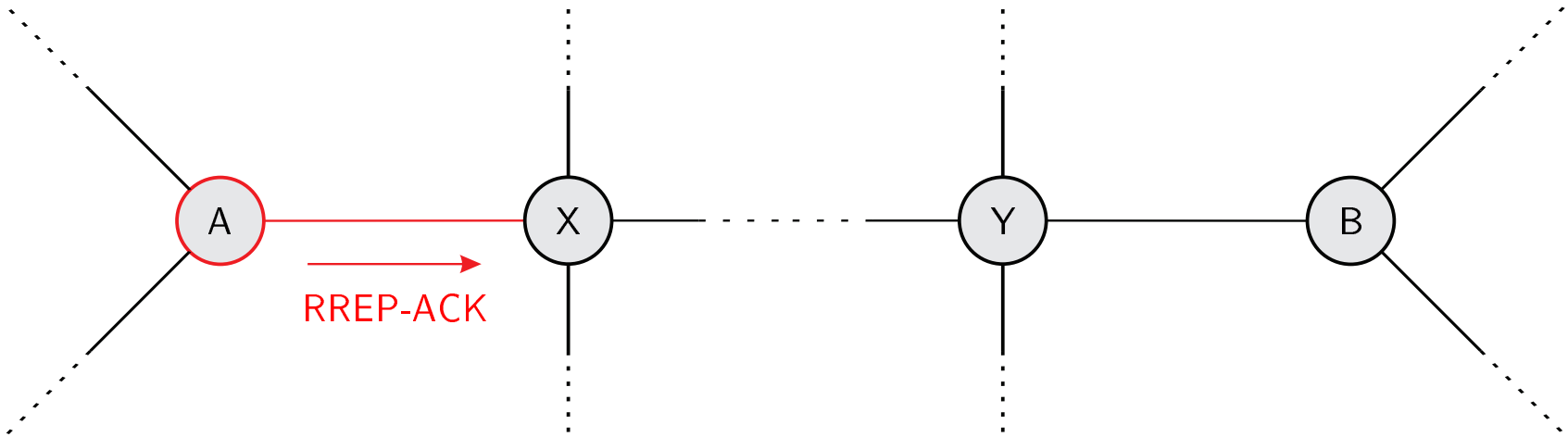


Figure: RREP-ACK message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

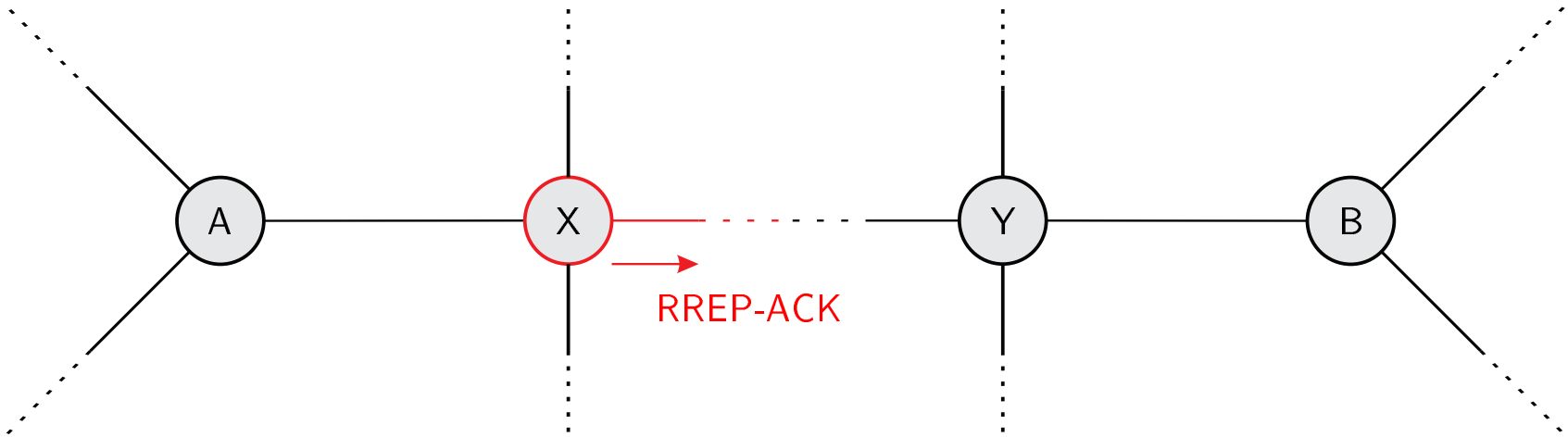


Figure: RREP-ACK message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - routing node process

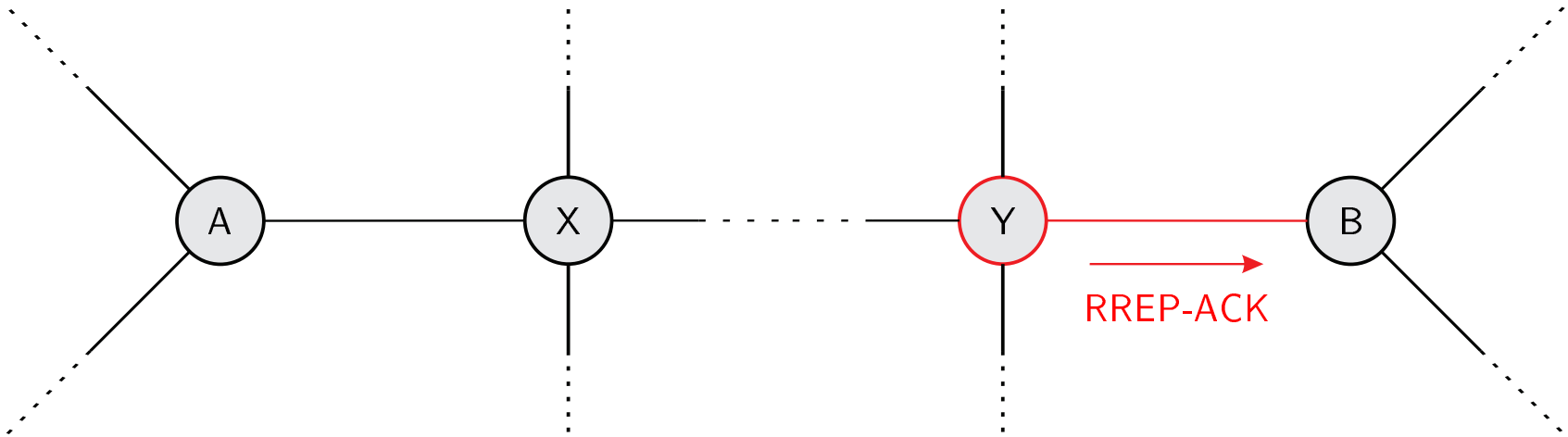


Figure: RREP-ACK message.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - Decision Maker block

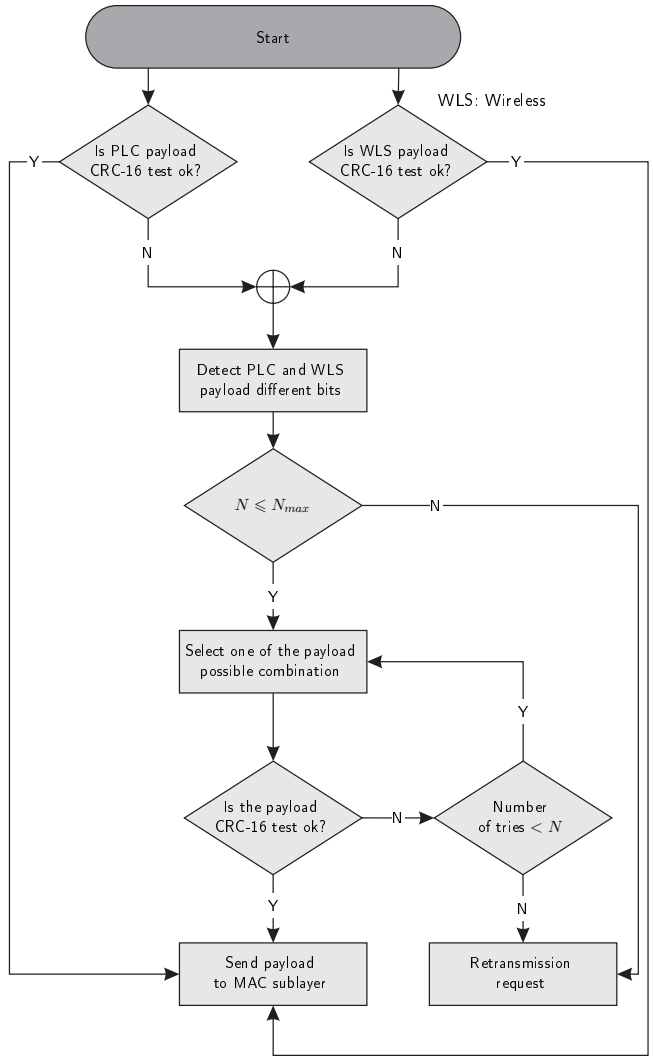


Figure: Decision maker block flowchart.

The NB hybrid PLC/Wireless transceiver

Enhancements and adaptations - Hilbert transform

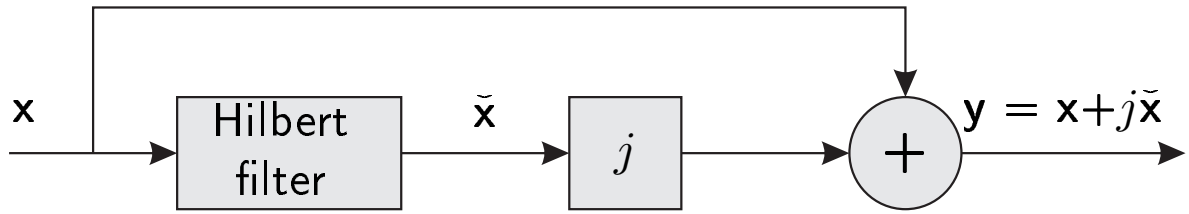


Figure: Hilbert transform block diagram.

- Recovery of in quadrature components of the preamble.
- Estimates the frequency deviation between the clock of the transmitter and receiver.
- Provides a better estimative of OFDM symbols to the digital demodulator, avoiding errors in the mapping process.

Prototyping the NB hybrid PLC/Wireless transceiver

FPGA implementation - physical layer

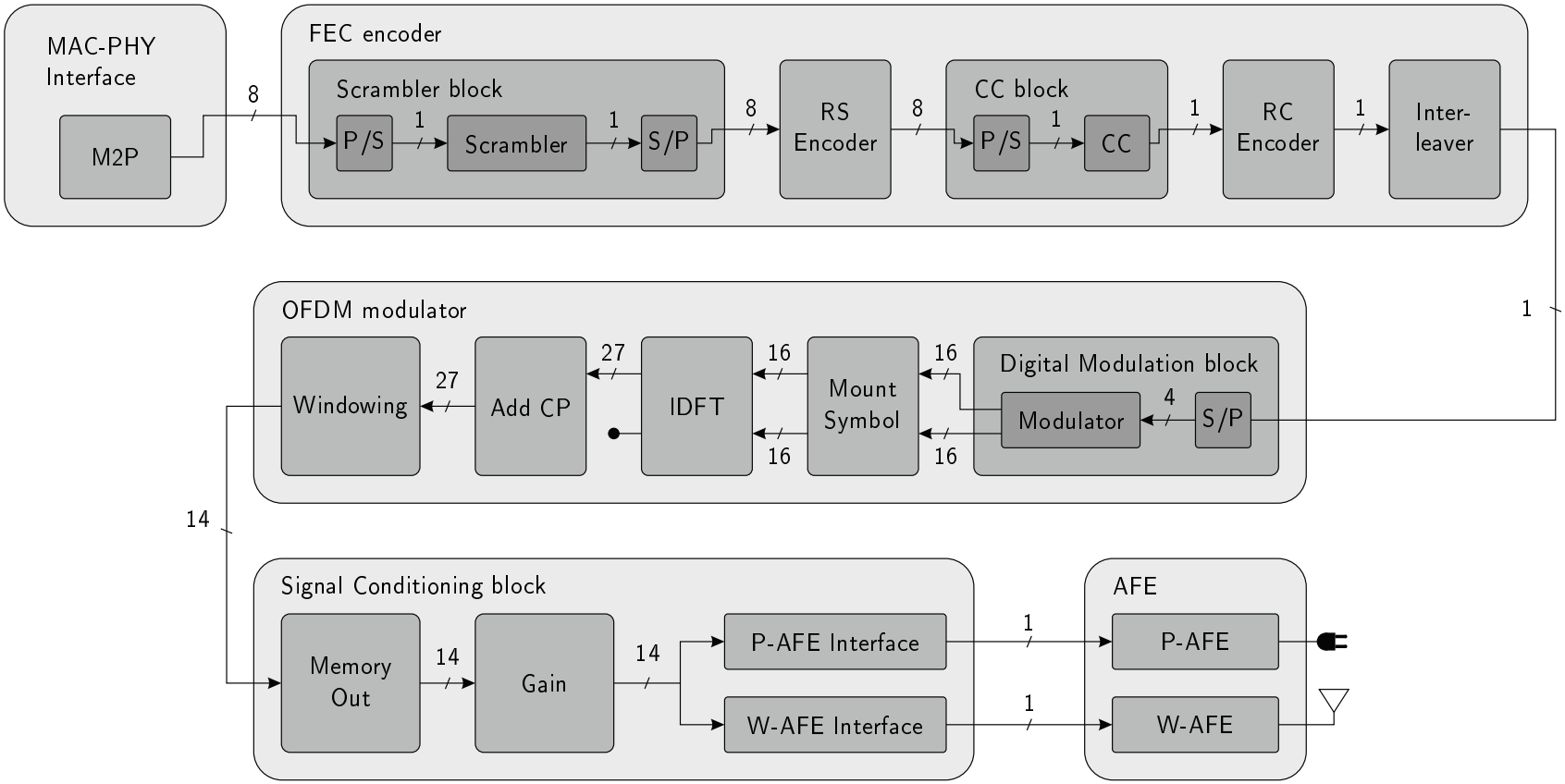


Figure: PHY TX FPGA implementation.

Prototyping the NB hybrid PLC/Wireless transceiver

FPGA implementation - physical layer

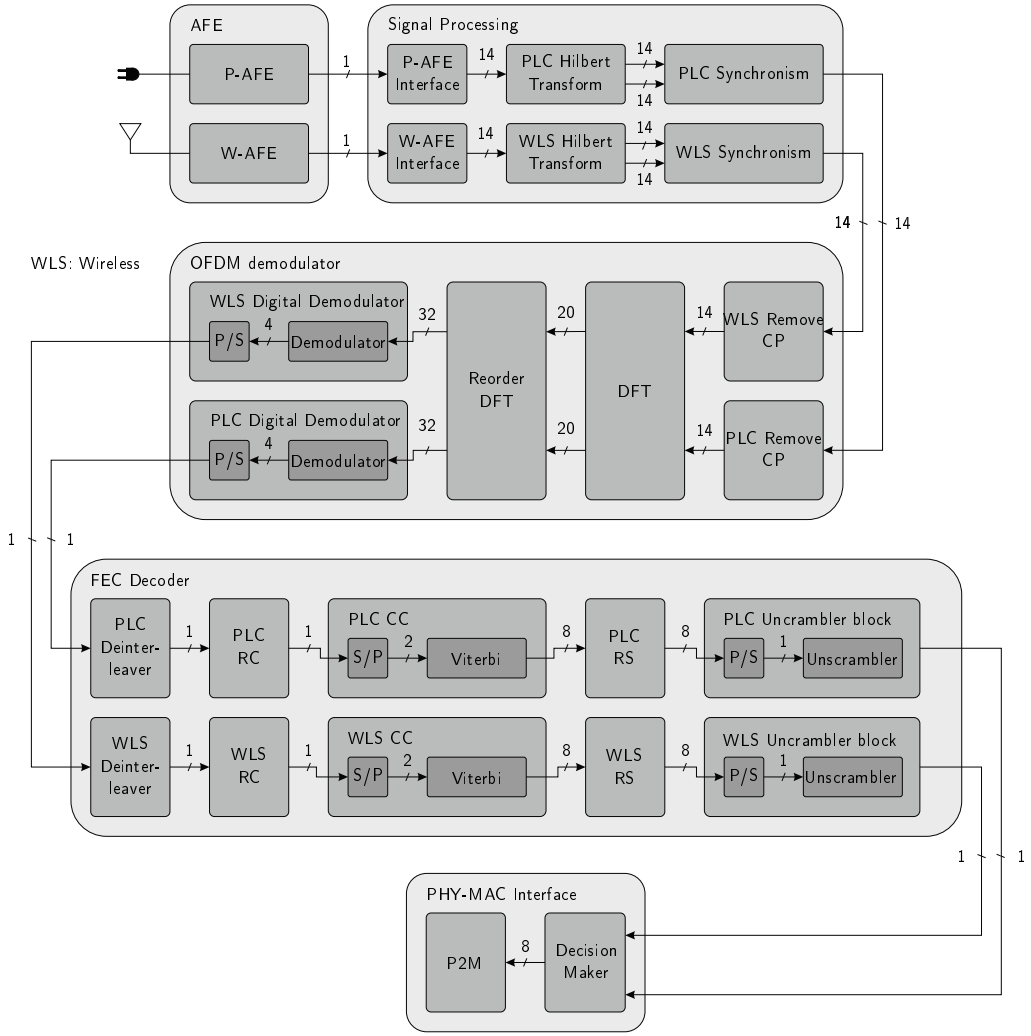


Figure: e-PHY RX FPGA implementation.

Prototyping the NB hybrid PLC/Wireless transceiver

FPGA implementation - physical layer

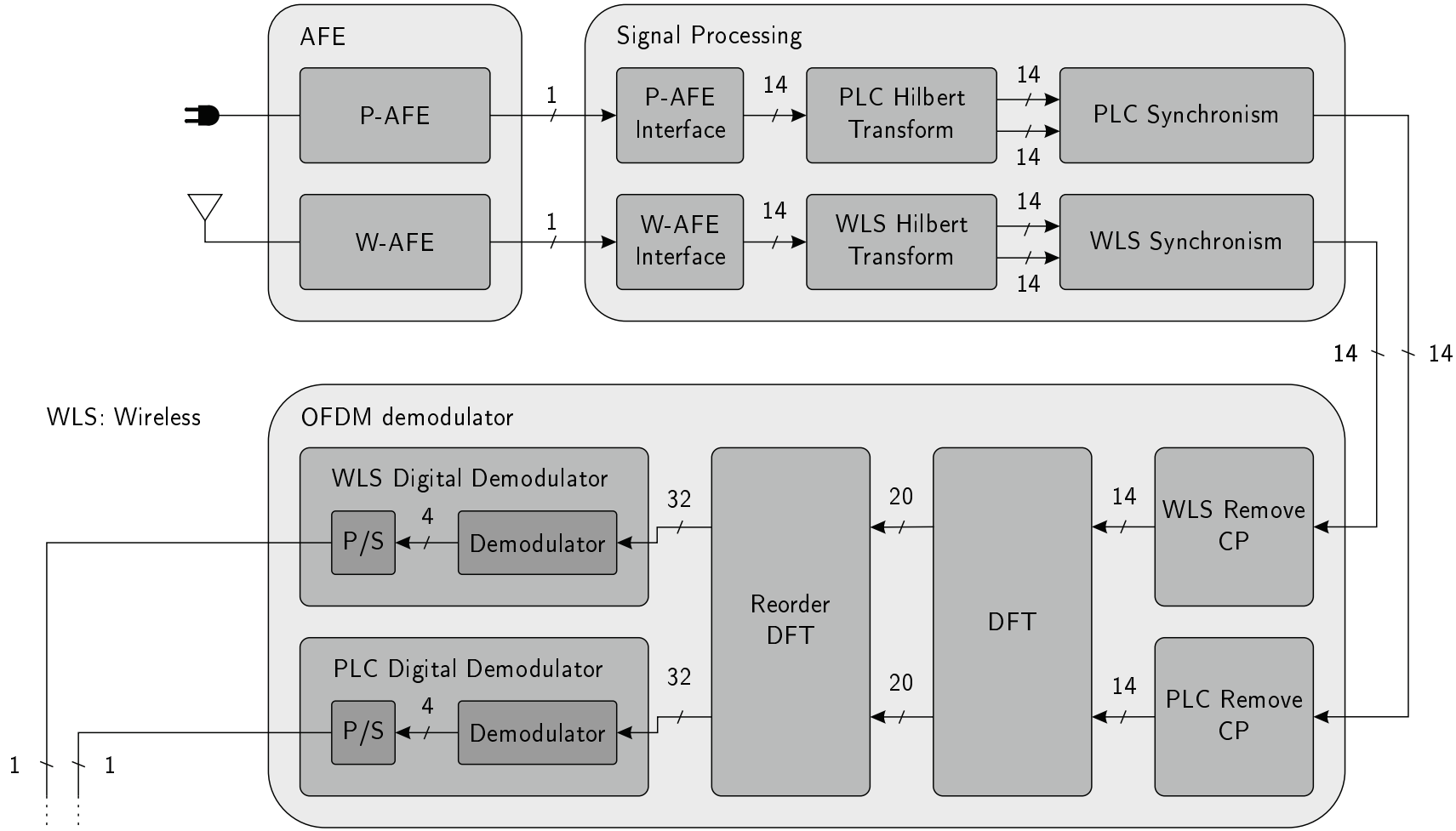


Figure: e-PHY RX FPGA implementation.

Prototyping the NB hybrid PLC/Wireless transceiver

FPGA implementation - physical layer

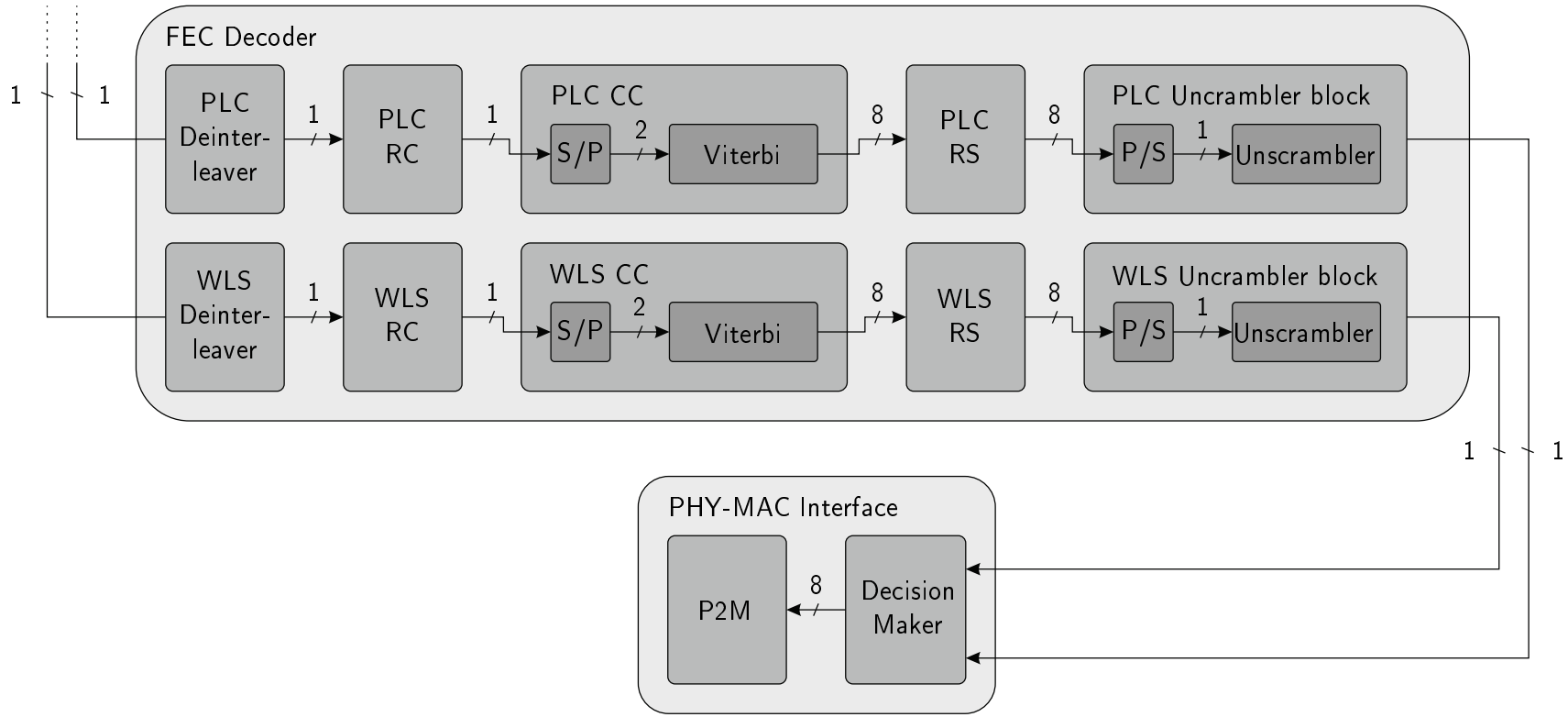


Figure: e-PHY RX FPGA implementation.

Prototyping the NB hybrid PLC/Wireless transceiver

FPGA implementation - data control standard

Avalon interface was chosen due to its simplicity and easiness of use.

- Avalon Streaming (Avalon-ST) interface:

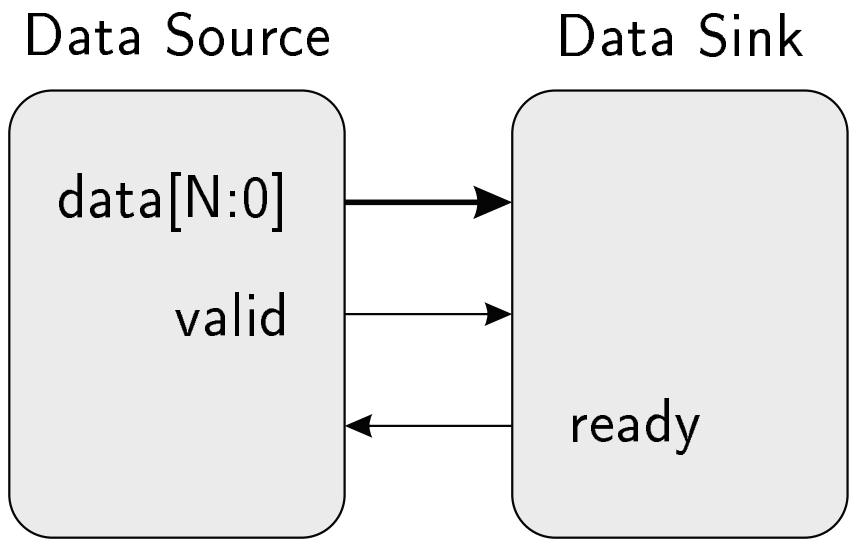
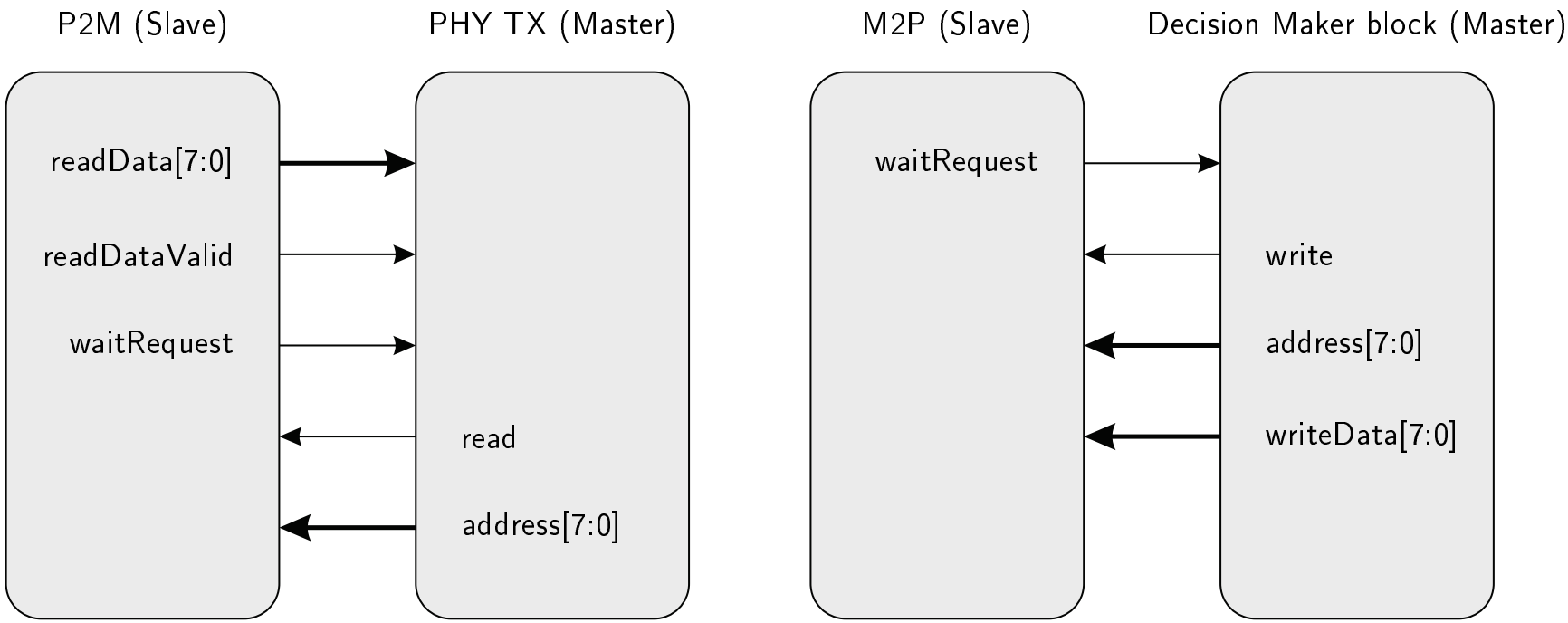


Figure: Avalon-ST interface.

Prototyping the NB hybrid PLC/Wireless transceiver

FPGA implementation - data control standard

- Avalon Memory-Mapped (Avalon-MM) interface:



(a) Transmitter direction. (b) Receiver direction.

Figure: Avalon-MM interface.

Prototyping the NB hybrid PLC/Wireless transceiver

The NB hybrid PLC/Wireless transceiver prototype

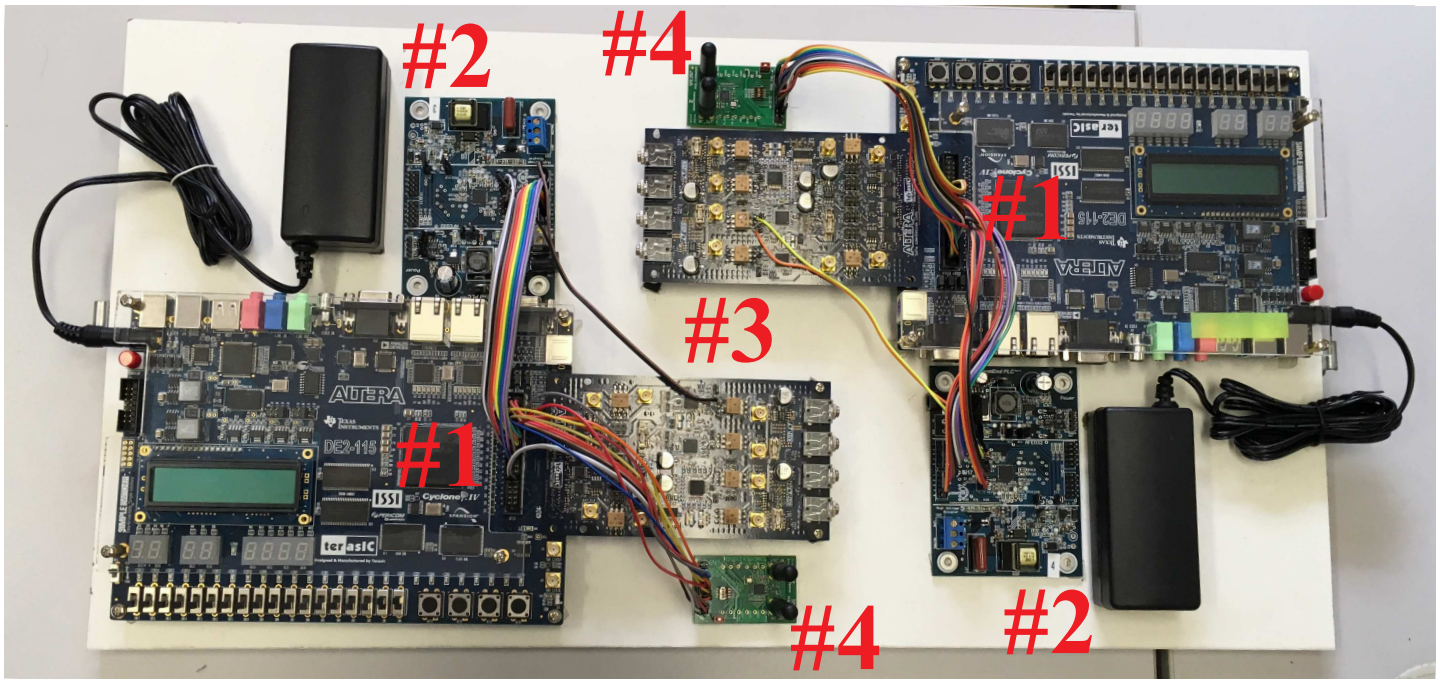


Figure: Setup of the NB hybrid PLC/Wireless transceiver prototype.

#1: Processor.
#2: PLC analog front-end.
#3: ADC.
#4: Wireless analog front-end.

Prototyping the NB hybrid PLC/Wireless transceiver

The NB hybrid PLC/Wireless transceiver prototype

- Processor:
  - Implemented in an FPGA device.
  - EP4CE115F29C7 FPGA chip from Cyclone IV family, designed by Altera, was chosen $\Rightarrow$ provides enough hardware resources.
- PLC analog front-end:
  - AFE032 chip from Texas Instrument.
  - Low-cost, integrated, and half-duplex AFE.
  - Supports CENELEC A, B, C, and D, ARIB, and FCC band plans.
  - Complies with G3-PLC, PRIME, IEEE 1902.1, and ITU-G.hnem standards.
- Wireless analog front-end:
  - SX-1257 chip from Semtech.
  - Operates from 862 MHz to 960 MHz.
  - Satisfies ETSI, ARIB, and FCC band plans.
  - Operate in half or full-duplex mode.

Prototyping the NB hybrid PLC/Wireless transceiver

The NB hybrid PLC/Wireless transceiver prototype

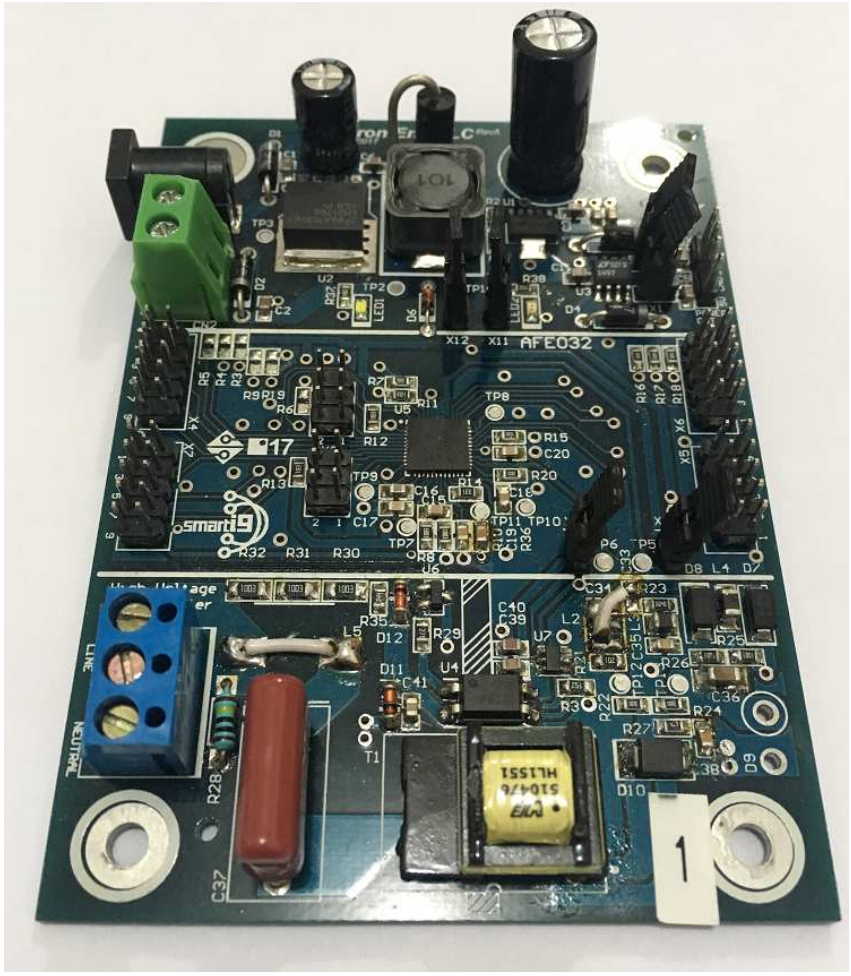


Figure: PLC analog front-end.

Prototyping the NB hybrid PLC/Wireless transceiver

The NB hybrid PLC/Wireless transceiver prototype

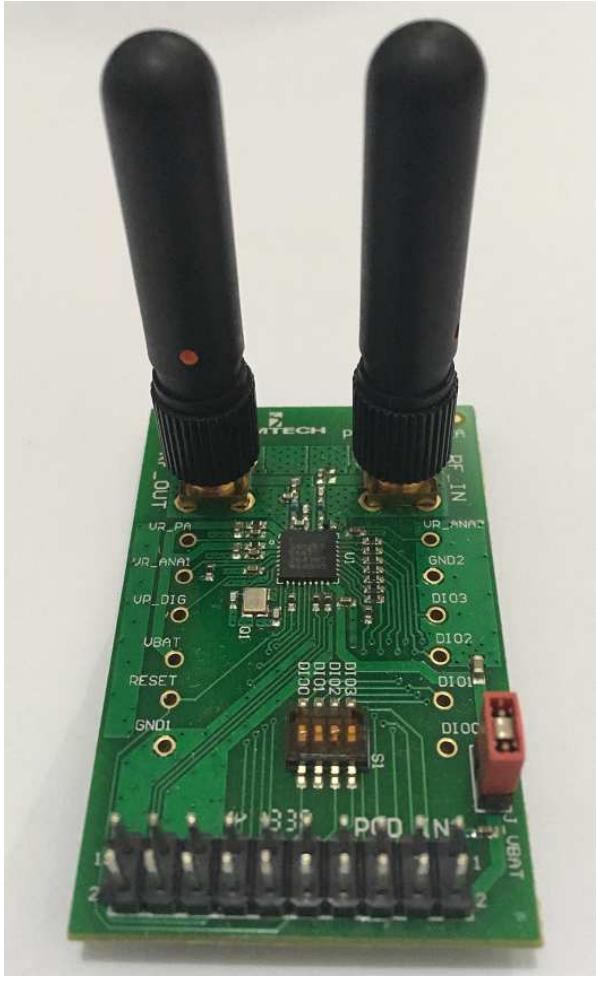


Figure: Wireless analog front-end.

Performance analyses

Decision Maker time analysis

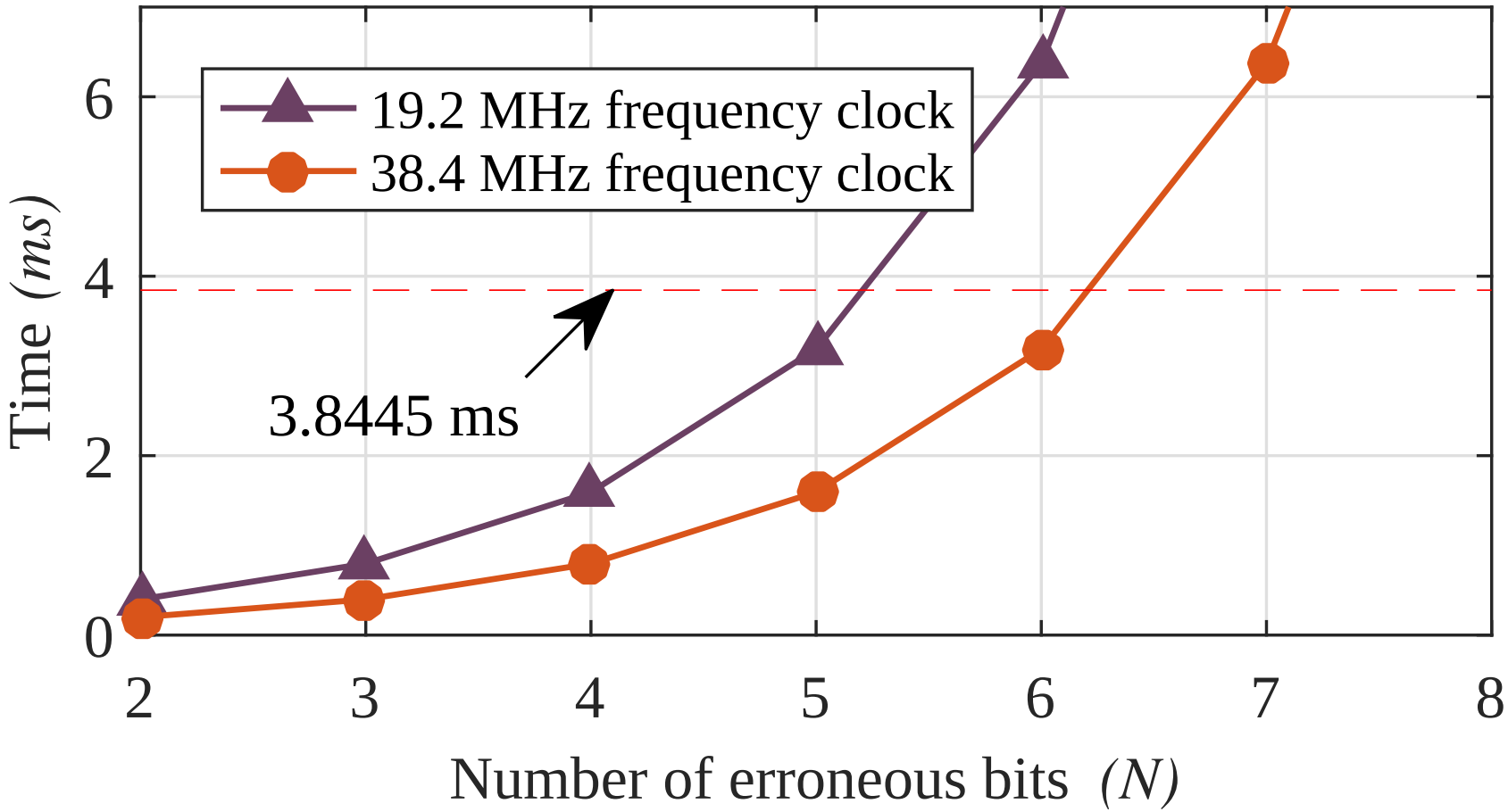


Figure: Time interval demanded by the Decision Maker block.

Performance analyses

Physical layer data-rate analysis

Table: Data-rates of the NB hybrid PLC/Wireless transceiver.

Modulation	Data-rate (kbps)
S-ROBO (BPSK)	14.4182
ROBO (BPSK)	23.3236
BPSK	101.3517
QPSK	210.3366
8-PSK	318.8974

Performance analyses

Hardware resource usage analysis

Table: Hardware resource usage per block.

Block	LE				Memory bits	M9Ks	DSP 9×9	DSP 18×18
	LUT-Only LEs	Register-Only LEs	LUT/Register LEs	Total LE				
Hilbert transform	833	315	765	1913	60	1	0	0
Synchronism	2971	671	1853	5495	290634	52	0	27
RX IEEE 1901.2	7624	2792	7556	17972	146232	55	0	20
TX IEEE 1901.2	4910	2007	5523	12440	676800	114	0	12
Decision Maker	170	104	205	479	3968	2	0	0
P-AFE	88	84	154	326	0	0	0	0
W-AFE	232	82	275	589	0	30	0	0
MAC sublayer	6140	2002	5778	13920	990726	152	0	29

Performance analyses

Hardware resource usage analysis

NB PLC transceiver:

- MAC sublayer, Hilbert transform, synchronism block, PHY TX IEEE 1901.2, PHY RX IEEE 1901.2, and a P-AFE block.

NB hybrid PLC/Wireless transceiver:

- MAC sublayer, two Hilbert transforms, two synchronism blocks, PHY TX IEEE 1901.2, two PHY RX IEEE 1901.2, the Decision Maker block, P-AFE block, and W-AFE block.

Performance analyses

Hardware resource usage analysis

Table: Hardware resource usage for NB PLC and NB hybrid PLC/Wireless transceiver prototypes.

Hardware resource		PLC	PLC-Wireless	ρ
LE	LUT-Only LEs	22566	34396	0.524
	Register-Only LEs	7871	11835	0.503
	LUT/Register LEs	21629	32283	0.492
	Total LE	52066	78514	0.508
Memory		2104452	2545346	0.209
M9Ks		374	514	0.374
DSP 9×9		0	0	-
DSP 18×18		88	135	0.534
$f_{\max}$ (MHz)		19.68	19.67	-0.005
Power consumption (mW)		311.92	348.4	0.117

Conclusions

- The best choice concerning the approach to be adopted is to use a PLC standard and extend it to be used in the wireless medium.
- The IEEE 1901.2 Standard showed up as the most promising standard.
- The Hilbert transform allows the estimation and correction of the frequency deviation between the transmitter and receiver's clock.
- The routing between nodes rises system coverage and reliability.
- Decision Maker block reduces the necessity of ARQ messages and, consequently, increasing the data network throughput.

Conclusions

- Regarding the Decision Maker block time analysis, it is not worth rising the PHY layer clock frequency in order to be able to correct a great number of bits.
- The data-rate varies from a few tens of kbps up to a few hundred of kbps.
- NB hybrid PLC/Wireless transceiver consumes less than twice the hardware resource usage and power consumption of the NB PLC transceiver.
- It is an expected result, having in mind that the NB hybrid PLC/Wireless transceiver was implemented aiming to increase performance and save hardware resources.

Future works

- To test the NB hybrid PLC/Wireless transceiver prototype in the field, facing more realistic and variety situations.
- To verify under which channel conditions the Decision Maker block can provide a maximum and a minimum performance.
- To improve AFE interface blocks, making them able to automatically reconfigure the AFEs to adapt to current channel conditions.
- Study of the P-AFE and W-AFE's behavior in several channel conditions.

Publications

List of journal and conference papers

The list of journal papers submitted during the graduate period is as follows:

- DA COSTA, VINÍCIUS LAGROTA R.; FERNANDES, VICTOR; RIBEIRO, MOISÉS VIDAL, "A Prototype of a Narrowband Hybrid PLC/Wireless Transceiver,"
  IEEE Internet of Things, 2017, under review.
- COSTA, LUIS GUILHERME DA SILVA; COLEN, GUILHERME R., QUEIROZ, ANTÔNIO CARLOS MOREIRÃO DE; DA COSTA, VINÍCIUS LAGROTA R.; VÍTOR, ULYSSES R. C.; RIBEIRO, MOISÉS VIDAL. "Access Impedance in Brazilian In-Home Broadband and Low-voltage Electric Power Grids: Measurement, Characterization and Modeling," *Journal of Communication and Information Systems (JCIS)*,*Electric Power Systems Research*, 2017, under review.

Publications

List of journal and conference papers

The list of journal papers submitted during the graduate period is as follows:

- DA COSTA, VINÍCIUS LAGROTA R.; SCHETTINO, HUGO VIVEIROS; CAMPONOGARA, ÂNDREI; DE CAMPOS, FABRÍCIO P.V.; RIBEIRO, MOISÉS VIDAL. "Digital filters for clustered-OFDM-based PLC systems: Design and implementation". *Digital Signal Processing*, v. 70, p. 166-177, 2017.
- COSTA, LUIS GUILHERME DA SILVA; DE QUEIROZ, ANTÔNIO CARLOS MOREIRÃO; ADEBISI, BAMIDELE; DA COSTA, VINICIUS LAGROTA RODRIGUES; RIBEIRO, MOISÉS VIDAL. "Coupling for Power Line Communications: A Survey". *Journal of Communication and Information Systems (JCIS)*, v. 32, p. 8-22, 2017.

Publications

List of journal and conference papers

The list of conference papers published during the graduate period is as follows (SBrT):

- COSTA, V. L. R.; MIRANDA, C. R.; SOUZA, S. A.; MARTINS, C. H. N.; CAMPOS, F. P. V.; OLIVEIRA, T. R.; RIBEIRO, M. V. "Front-End Analógico para Power Line Communication na faixa entre 1.7 e 50 MHz". In: *XXXIII Simpósio Brasileiro de Telecomunicações*, 2015, Juiz de Fora. SBrT, 2015.
- COSTA, L. G. S.; PICORONE, A. A. M.; COSTA, V. L. R.; RIBEIRO, M. V. "Projeto e Caracterização de Acopladores para Power Line Communication". In: *XXXIII Simpósio Brasileiro de Telecomunicações*, 2015, Juiz de Fora. SBrT, 2015.
- COSTA, L. G. S.; PICORONE, A. A. M.; QUEIROZ, A. C. M.; COSTA, V. L. R.; RIBEIRO, M. V. "Caracterização da Impedância de Acesso à Rede de Energia Elétrica Residencial para Uso em Sistemas Power Line Communications". In: *XXXIII Simpósio Brasileiro de Telecomunicações*, 2015, Juiz de Fora. SBrT, 2015.

Thank you!