ECE 593

Fundamentals of Pre-Silicon Validation

Final Project

MESI Intersection Controller

Waveform

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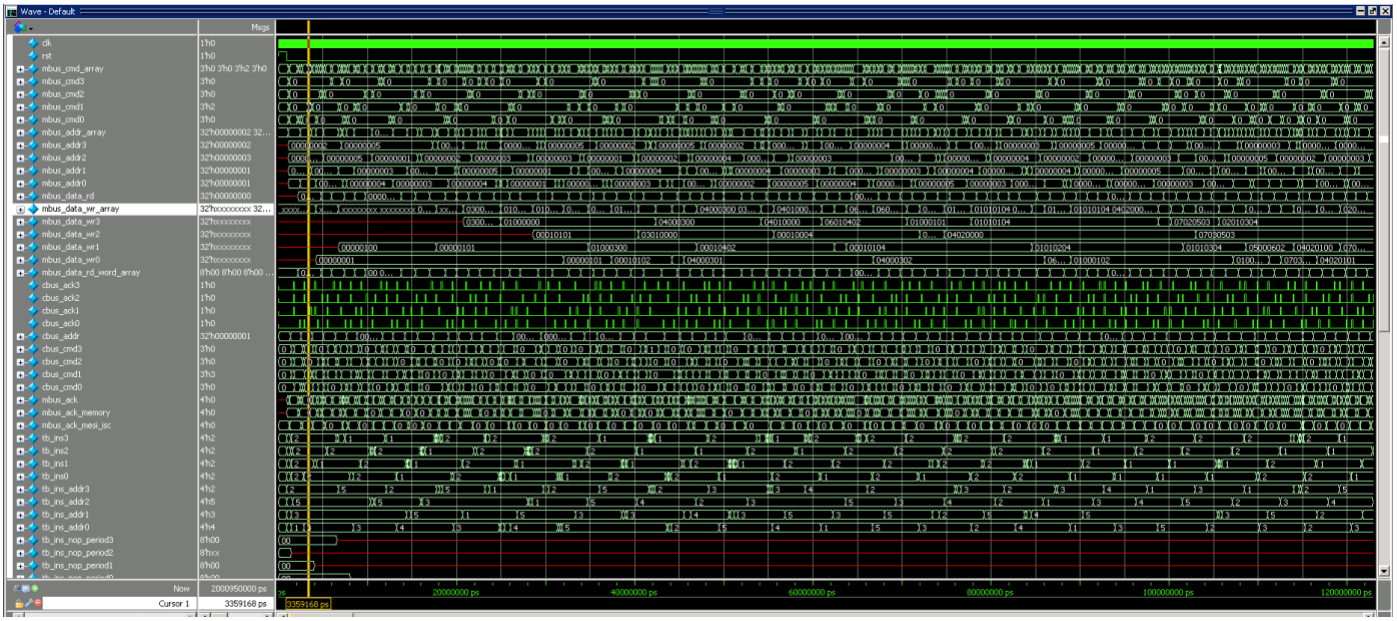
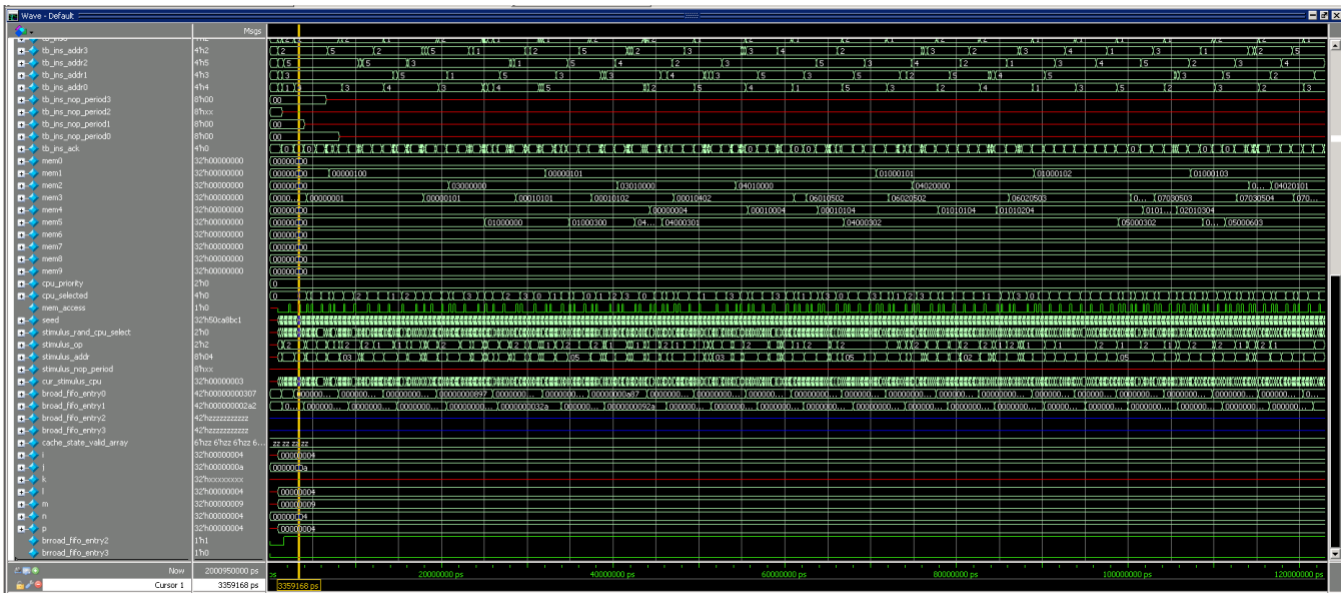
Waveform

Description:

- The MESI_ISC receives the broadcast request from the system masters through the main bus.
- It sends the write snoop, read snoop, write-enable, and read-enable to the system masters through the coherency bus.
- As there are four processors, there are four main buses and four coherency buses.
- MESI_ISC separates each broadcast request that a master sends (initiator) to a separated snoop requests for each master, except for the initiator.
- The transcript output displays the number of reads, Number of writes and NOP operations.
- The inputs are Clk, Reset, Memory bus commands, Memory bus address, Coherence bus acknowledge. Outputs are Coherence bus address, Coherence bus commands, Memory bus acknowledge.
- MESI_ISC has four processors and a main memory. Each processor has a main bus for performing memory read and memory write accesses.
- In the below waveform we could see there are four addresses each on one main bus as there are four processors. The main bus and coherence bus are used for coherence protocol.
- There are internal signals like FIFO control signals which





Transcript

```
# Start time: 16:25:01 on May 17,2019
# ** Note: (vsim-8009) Loading existing optimized design _opt19
# Loading work.mesi_isc_tb(fast)
# Loading work.mesi_isc(fast)
# Loading work.mesi_isc_broad(fast)
# Loading work.mesi_isc_broad_cntl(fast)
# Loading work.mesi_isc_basic_fifo(fast)
# Loading work.mesi_isc_breq_fifos(fast)
# Loading work.mesi_isc_breq_fifos_cntl(fast)
# Loading work.mesi_isc_basic_fifo(fast__1)
# Loading work.mesi_isc_tb_cpu(fast)
VSIM 2> run -all
# Watchdog finish
#
# Statistic                          Text
#
# CPU 3. WR:        238 RD:        424 NOP:         68
#
# CPU 2. WR:        220 RD:        455 NOP:         58
#
# CPU 1. WR:        202 RD:        434 NOP:         50
#
# CPU 0. WR:         232 RD:        414 NOP:         57
#
# Total rd and wr accesses:        2619
#
# ** Note: $finish    : N:/mesi_isc_tb.v(315)
#    Time: 2000950 ns  Iteration: 1  Instance: /mesi_isc_tb
# 1
# Break in Module mesi_isc_tb at N:/mesi_isc_tb.v line 315

VSIM 3> c
```