QSPI IP Design Completion for RTL 0.5 Design Review

In the RTL 0.5 milestone, teams demonstrate an understanding of design requirements by completing most of the IP's RTL code, passing basic verification tests, and ensuring the code is synthesizable. Below are the detailed requirements and timeline for this milestone.

Requirements

1. RTL Code Development

Teams must complete the RTL code for the following components: Control/Status Registers (CSR), Chip Enable (CE), FIFO, QSPI Finite State Machine (QSPIFSM), and DMA units.

- XIP (Execute-In-Place): Optional. If implemented, ensure the logic connects the full IP model without disconnection and completes a synthesis run with representative gate counts.
- Component Connectivity: Connect all units as specified in the provided diagram.
- Configuration Consistency: Verify that all configuration bits (parameters) are implemented consistently across the design.

2. Verification

Conduct verification to ensure at least basic tests pass. Focus on repeatable, self-checking tests within the IP testbench.

a. Test 1: QSPI Read (Opcode 0x03, 4 Bytes, Command Mode, No DMA)

- Setup: Use the APB interface exclusively to configure the IP and trigger the command via APB writes.
- Execution: Perform a QSPI read at address 0x0 for 4 bytes.
- Verification:
    - Confirm that CE to QSPIFSM activity completes successfully, writing read data to the RX FIFO and setting the command status to "done."
    - Perform an APB read to retrieve the RX FIFO data in the testbench and verify all 4 bytes are 0xFFFFFFFF.

- Use a delay or trigger on Rx_fifo_empty to determine when to read the data.
- Inspect the waveform to ensure all internal signals return to an idle state, ready for the next command.

b. Test 2: QSPI Read with DMA

- Setup: Repeat Test 1 but enable DMA operation with appropriate CSR configuration.
- Execution: When data is available in the RX FIFO, the DMA unit reads it and writes to the AXI memory slave at the specified address.
- Verification:
  - Validate that the AXI memory slave address contains 0xFFFFFFFF.
  - Ensure the RX FIFO is not read via CSR to avoid disrupting the FIFO pointer.

c. Additional Tests

To demonstrate development progress, include the following tests:

- Additional read tests using multiple lanes for address and data.
- Tests with command lengths exceeding 4 bytes.
- Verify these tests function correctly in DMA mode.
- Perform write tests using the TX FIFO to pass data, ensuring a write enable command is issued first to enable the QSPI device for writing.
- Execute a read command to verify the expected data is returned.

3. Synthesis

Synthesize the IP design to obtain:

- Gate counts
- Area
- Operating speed (target: 200 MHz)

4. Presentation

Prepare a presentation using the provided template:

- Ensure all information is clear, accurate, and up to date.
- Assign at least three slides per team member.
- Rehearse to ensure the presentation is completed within 15 minutes, respecting each team member's allocated time.

Timeline

- September 3, 2025: Review with the instructor (30 minutes per team, consistent with prior reviews).
    - Teams can send the presentation to instructor via DM anytime for feedback.
- September 10, 2025: Final presentation for all five teams. Please arrive on time.
- Grading: The design accomplishments and presentation quality will determine the course grade per individual.