Opcode	15	14	13		11	10	9	8	7	6	5 4	3	2	1	0
LSL Rd, Rm, #	0	0	0	0	0			#			Rm			Rd	
LSR Rd, Rm, #	0	0	0	0	1	L		#			Rm		_	Rd	
ASR Rd, Rm, #	0	0	0	1	0			#	_		Rm			Rd	_
ADD Rd, Rn, Rm	0	0	0	1	1	0	0		Rm		Rn Rn	_		Rd Rd	_
SUB Rd, Rn, Rm	×	Ů	٥	1	1	1	0		##		Rn Rn	_		Rd	_
ADD Rd, Rn, # SUB Rd, Rn, #	0	0	0	1	1	1	1	Н	#		Rn	-		Rd	_
SUB Rd, Rn, # MOV Rd. #	0	0	1	0	0	Ė	Pd	H	*		PGI	_		Rü	
MOV KG, # CMP Rn, #	0	0	1	0	1		Rn		-	-	- 1			-	
ADD Rd, #	0	0	1	1	0		Rd		-	-	_			-	-
SUB Rd. #	0	0	1	1	1	Н	Rd		-	-	-	_		-	-
AND Rd. Rm	0	1	0	0	0	0	0	0	0	0	Rm			Rd	
EOR Rd, Rm	0	1	0	0	0	0	0	0	0	1	Rm			Rd	
LSL Rd, Rs	0	1	0	0	0	0	0	0	1	0	Rs			Rd	
LSR Rd, Rs	0	1	0	0	0	0	0	0	1	1	Rs			Rd	
ASR Rd, Rs	0	1	0	0	0	0	0	1	0	0	Rs			Rd	
ADC Rd, Rm	0	1	0	0	0	0	0	1	0	1	Rm			Rd	
SBC Rd, Rm	0	1	0	0	0	0	0	1	1	0	Rm			Rd	
ROR Rd, Rs	0	1	0	0	0	0	0	1	1	1	Rs			Rd	
TST Rm, Rn	0	1	0	0	0	0	1	0	0	0	Rn			Кm	
NEG Rd, Rm	0	1	0	0	0	0	1	0	0	1	Rn			Rd	
CMP Rm, Rn	0	1	0	0	0	0	1	0	1	0	Rn			Кm	
CMN Rm, Rn	0	1	0	0	0	0	1	0	1	1	Rn			Зm	
ORR Rd, Rm	0	1	0	0	0	0	1	1	0	0	Rm			Rd	
MUL Rd, Rm	0	1	0	0	0	0	1	1	0	1	Rm			Rd	
BIC Rm, Rd	0	1	0	0	0	0	1	1	1	0	Rn			Кm	
MVN Rd, Rm	0	1	0	0	0	0	1	1	1	1	Rm			Rd	
Unpredictable	0	1	0	0	0	1	0	0	0	0	x x	Х	х	×	×
ADD Rd, Rm	0	1	0	0	0	1	0	0	H1	H2	Rm			Rd	_
Unpredictable	0	1	0	0	_	_	0			0	х	Х	х		×
CMP Rm, Rn	0	1	0	0	0	1	1	1	H1	H2	Rn			₹m	_
Unpredictable	0	1	0	0	0	1	1	0	0	0 H2	x x	Х	х	×	×
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	^	4		1		_					-	-	^		^
BLX Rm	0	1	0	0	0	1	1	1	1	H2	Rm		0	0	0
Unpredictable	0	1		0	0	_	1				Rm x x	x	_		
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Unpredictable LDR Rd, [PC, #] STR Rd, [Rn, Rm] STRH Rd, [Rn, Rm]	0 0	1 1 1	0 0 0	0 0 1	0	1 1 0 0	1 1 Rd 0	1	1 x Rm	H2	x x C Relation	x /e C	1 Offse	×	
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Unpredictable LDR Rd, [PC, #] STR Rd, [Rn, Rm] STHR Rd, [Rn, Rm] STBB Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm]	0 0 0 0	1 1 1 1 1 1	0 0 0 0 0	0 0 1 1 1 1	0 0 1 0 0	1 0 0 1 1	1 1 Rd 0 1	1	Rm Rm Rm	H2 X	x x C Relation Rn Rn Rn Rn	x /e C	1 Offse	x et Rd	
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Umpredictable LDR Rd, [FC, #] STR Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] LDR Rd, [Rn, Rm] LDR Rd, [Rn, Rm] LDR Rd, [Rn, Rm] LDR Rd, [Rn, Rm] LDRSH Rd, [Rn, R0FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] LDR Rd, [SP, 80FF] LDR Rd, [SP, 80FF] ADD Rd, SP, 80FF ADD Rd, SP, 80FF Umpredictable PUSH {creg list>, <lr>} PUSH {creg list>, <lr>} PUSH {creg list>, <lr>} PUSH {creg list>, <lr>} POP {creg list>, <lr>}</lr></lr></lr></lr></lr>	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 0 0 0 1 1 1 0 0	0 0 0 0 0 1 1 1 0 1 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 0	1 1 0 0 1 1 1 1 0 0 0 1 1 1 0 0 0 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 1 1 8 6 8 6 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x P	x x x x Registative C Relativistic C Relativistic C Registration C Registration C Relativistic C	/e C	1 Diffsee Offsee Offsee Offsee Offsee ist x	x x x x x x x x x x	x
Unpredictable LDR Rd, [PC, #] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] LDR Rd, [Rn, Rm] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 90FF] STR Rd, [Rn, 90FF] LDR Rd, [Rn, 90FF] STR Rd, [Rn, 90FF] LDR Rd, [Rn, 90FF] LDR Rd, [SP, 80FF] LDR Rd, [SP, 80FF] LDR Rd, [SP, 80FF] LDR Rd, [SP, 80FF] STB SP, SP, 80FF Unpredictable PUSH {creg list>, <lr>) POP {creg list>, <lr>) POP {creg list>, <lr>) LDR LDR LSDR LSDR LSDR LSDR LSDR LSDR LS</lr></lr></lr>	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	0 0 1 1 1 1 1 1 1 0 0 1 1 1 0 0 1 1 1 1	0 0 0 0 0 1 1 1 0 1 0 1 0 0 1 0 0 1 0	1 1 0 0 1 1 1 1 0 0 0 1 1 1 1 0 0 0 1	1 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 8 0 8 8 8 8	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x p	x x x x x x x x x x x x x x x x x x x	ve Cove Cove Cove Cove Cove Cove Cove Co	1 Diffsee Offsee Offsee Offsee X x x	x et Rd	×
Unpredictable LDR Rd, [PC, #] STR Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LORSB Rd, [Rn, Rm] LORSB Rd, [Rn, Rm] LORSB Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, R0FF] LDR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [SP, 80FF] ADD Rd, SP, 80FF STB STR, Rd, SP, 80FF STB SP, SP, 80FF Unpredictable Unpredictable	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0	0 0 1 1 1 1 1 1 1 0 0 1 1 1 0 0 1 1 1 1	0 0 0 0 0 1 1 1 0 1 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 0	1 1 0 0 1 1 1 1 0 0 0 1 1 1 0 0 0 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 1 1 8 6 8 6 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x p	x x x x Register x x x x x x x x x x x x x x x x x x x	ve Cove Cove Cove Cove Cove Cove Cove Co	1 Diffsee Offsee Offsee Offsee X x x	x et Rd	×
Umpredictable LDR Rd, [PC, #] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] LDR Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRR Rd, [Rn, Rm] LDRSH Rd, [Rn, RM] STR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] LDR Rd, [SP, 80FF] ADD Rd, PC, 80FF ADD Rd, SP, 80FF MD Rd, SP, 80FF Umpredictable PUSH {creg list>, <lr>} Umpredictable EKPT # Umpredictable EKPT # Umpredictable EKPT # Umpredictable EKPT #</lr>	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 0 0 1 1 1 0 0 1 1 1 1	0 0 0 0 0 0 1 1 1 0 1 0 0 1 0 0 1 0 0 0 1 0	1 1 0 0 1 1 1 1 0 0 0 1 1 1 1 1 2 0 0 1 1 1 1	1 1 0 1 0 1 1 0 1 1 0 1 1 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x p	x x x x x x x x x x x x x x x x x x x	ve C	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	x et Rd	×
Unpredictable LDR Rd, [PC, #] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] LDR Rd, [Rn, Rm] STR Rd, [Rn, 80FF] LDR Rd, [SP, 80FF] SUB SP, SP, 80FF Unpredictable STMLA Rni, {creg list.} STMLA Rni, {creg list.}	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 0 0 1 1 1 0 0 1 1 1 1	0 0 0 0 0 1 1 1 0 1 0 1 0 0 1 0 0 1 0 0 0 1 0	1 1 0 0 1 1 1 1 0 0 0 1 1 1 1 1 2 0 0 1 1 1 1	1 1 0 1 0 1 1 0 1 1 0 1 1 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x p	x x x x x x x x x x x x x x x x x x x	ve Cove Cove Cove Cove Cove Cove Cove Co	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	x et Rd	×
Unpredictable LDR Rd, [PC, #] STR Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LORSH Rd, [Rn, Rm] LORSH Rd, [Rn, Rm] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] STR Rd, [SP, 80FF] ADD Rd, SP, 80FF ADD Rd, SP, 80FF ADD Rd, SP, 80FF ADD Rd, SP, 80FF STB SP, SP, 80FF Unpredictable Unpredictable Unpredictable Unpredictable STMIA Rni, {creg list>, cLR>} LDMIA Rni, {creg list>} CATarget Addr>	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 0 0 1 1 1 0 0 1 1 1 1	0 0 0 0 0 0 1 1 1 0 1 0 0 1 0 0 1 0 0 0 1 0	1 1 0 0 1 1 1 1 0 0 0 1 1 1 1 1 2 0 0 1 1 1 1	1 1 0 1 0 1 1 # (C Rtd C	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x P	x x x x x x x x x x x x x x x x x x x	ve Cove Cove Cove Cove Cove Cove Cove Co	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	x et	x
Unpredictable LDR Rd, [PC, #] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] STR Rd, [Rn, 80FF] LDRSR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] STR Rd, [SN, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [SN, 80FF] LDR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] UDPR (A, [SN, 80FF] STR Rd, [SN, 80FF] STR Rd, [SN, 80FF] LDR Rd, [SN, 80FF] LDR Rd, [SN, 80FF] LDR Rd, [SN, 80FF] LDR Rd, [SN, 80FF] STR STR Rd, [SN, 80FF] LDR Rd, [SN, 80FF] STR STR Rd, [SN, 80FF] STR Rd	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 0 0 1 1 1 1 0 0 1	0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 1 1 0	1 1 1 0 0 0 1 1 1 1 x 0 0 1 1 1 1 x 0 1 1 1 1	1 1 0 1 0 1 1 0 0 1 1 # (C Rud	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x P	x x x x x x x x x x x x x x x x x x x	ve Cove Cove Cove Cove Cove Cove Cove Co	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	x et	x
Unpredictable LDR Rd, [PC, #] STR Rd. [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] LDR Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] STR Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] STR Rd, [Rn, #0FF] LDR Rd, [R	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 1 1 1 1 0 0 0 1 0 0 0 1 1 0 0 1 0 0 0 1 1 0	1 1 0 0 1 1 1 1 0 0 0 1 1 1 1 1 2 0 0 1 1 1 1	1 1 0 1 0 1 1 # (C Rtd C	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Rm R	H2 x x P P S S S S S S S S X x x x x x x x x x x x	x x x x x x x x x x x x x x x x x x x	ve Cove Cove Cove Cove Cove Cove Cove Co	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	x et	x
Umpredictable LDR Rd, [PC, #] STR Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [SP, 80FF] ADD Rd, PC, 80FF ADD Rd, SP, 80FF Umpredictable TUSH {creg lists, <pc>} Umpredictable Umpredictable STMTA Rn1, {creg lists} LDMTA Rn1, {creg lists} B <-Caraget Addr> B <-Caraget Addr> B <-Caraget Addr></pc>	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 0 0 0 1	1 1 1 0 0 0 1 1 1 1 x 0 0 1 1 1 1 x 0 1 1 1 1	1 1 0 1 0 1 1 0 0 1 1 # (C Rud	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Remarks and the second	S S S S S S X X X X X	x x x x Regists x x x x x x x x x x x x x x x x x x	ve Cove Cove Cove Cove Cove Cove Cove Co	1 1 Offise Offis	x et	x
Unpredictable LDR Rd, [PC, #] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] STRR Rd, [Rn, Rm] LDR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [SP, 80FF] LDR Rd, [SP, 80FF] SUB SP, SP, 80FF LUMPredictable STMIA Rni, {-reg list-} B(-cond-) -Target Addr-> SMIA STARGET Addr-> SMIX -Target Addr-> SMX -Target Addr-> SMX -Target Addr->	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 1 1 1 0 0 0 1 0 0 0 1 1 0 0 0 0 1 1 1 0	1 1 1 0 0 0 1 1 1 1 x 0 0 1 1 1 1 x 0 1 1 1 1	1 1 0 1 0 1 1 0 0 1 1 # (C Rud	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Remarks and the second	H2 X X P	x x x x Registre of the control of t	ve Cove Cove Cove Cove Cove Cove Cove Co	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	x et	x
Umpredictable LDR Rd, [PC, #] STR Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSB Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] LDRSH Rd, [Rn, Rm] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [Rn, 80FF] LDR Rd, [Rn, 80FF] STR Rd, [SP, 80FF] ADD Rd, PC, 80FF ADD Rd, SP, 80FF Umpredictable TUSH {creg lists, <pc>} Umpredictable Umpredictable STMTA Rn1, {creg lists} LDMTA Rn1, {creg lists} B <-Caraget Addr> B <-Caraget Addr> B <-Caraget Addr></pc>	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 0 0 0 1	1 1 1 0 0 0 1 1 1 1 x 0 0 1 1 1 1 x 0 1 1 1 1	1 1 0 1 0 1 1 0 0 1 1 # (C Rud	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Remarks and the second	H2 X X P	x x x x Regists x x x x x x x x x x x x x x x x x x	ve C C C C C C C C C C C C C C C C C C C	Offsee Offsee Offsee Offsee Offsee Offsee offsee ist x x x ist x x ist x x	x et	x



rev	Mnemonic	Definition	Alternate Description
	ADC	Add with Carry	ADD numbers and Carry bit
	ADD	Add	ADD numbers
	AND	Logical AND	AND together numbers
	ASR	Arithmetic Shift Right	Signed Right Shift (>>)
	В	Branch	Jump to an address
	BIC	Bit Clear	AND's the compliment of a number
v5	BKPT	Breakpoint	Software Breakpoint
	BL	Branch with Link	Jump to an address, and set LR to return address
v5	BLX	Branch with Link and Exchange	Jump to an address, set LR to return address, switch operating modes
	BX	Branch and Exchange	Jump to an address, and switch operating modes
	CMN	Compare Negative	Compare numbers by addition
	CMP	Compare	Compare numbers by subtraction
	EOR	Logical Exclusive OR (XOR)	Exclusive OR together numbers
	LDMIA	Load Multiple, Increment After	Load Multiple registers at once
	LDR	Load Register (word)	Load an unsigned 32bit number into a register
	LDRB	Load Register (byte)	Load an unsigned 8bit number into a register
	LDRH	Load Register (halfword)	Load an unsigned 16bit number into a register
	LDRSB	Load Register (byte)	Load a signed 8bit number into a register
	LDRSH	Load Register (halfword)	Load a signed 16bit number into a register
	LSL	Logical Shift Left	Unsigned Left Shift (<<)
	LSR	Logical Shift Right	Unsigned Right Shift (>>)
	MOV	Move	Move a number
	MUL	Multiply	Multiply numbers
	MVN	Move Not	Compliment a number
	NEG	Negate	Negate a number
	ORR	Logical OR	OR together numbers
	POP	Pop multiple registers	Takes numbers off the stack
	PUSH	Push multiple registers	Puts numbers on to the stack
	ROR	Rotate Right Register	Shifts right (>>), and numbers shifted off are appended to top
	SBC	Subtract with Carry	Subtract numbers and ADD Carry bit
	STMIA	Store Multiple, Increment After	Store Multiple registers at once
	STR	Store Register (word)	Store a 32bit number into an address
	STRB	Store Register (byte)	Store an 8bit number into an address
	STRH	Store Register (halfword)	Store a 16bit number into an address
	SUB	Subtract	Subtract numbers
	SWI	Software Interrupt	Execute code/"bios" calls
	TST	Test	Checks if one of more bits are set
	Unused	Unused Opcode	Future revisions of the Architecture will not use this space

Opcode	Work	Notes	Z	С	N	٧
ADC Rd, Rm	Rd = Rd + Rm + C	-	х	х	х	х
ADD Rd, #	Rd = Rd + #	-	х	х	х	Х
ADD Rd, PC, #OFF	Rd = Rd + (PC + (#OFF << 2))	-				
ADD Rd, Rm	Rd = Rd + Rm	Rd or Rm must be a				
		high register				
ADD Rd, Rn, #	Rd = Rn + #	-	х	х	Х	х
ADD Rd, Rn, Rm	Rd = Rm + Rn	-	Х	Х	Х	х
ADD Rd, SP, #OFF	Rd = SP + (#OFF << 2)	-				
AND Rd, Rm	Rd = Rd & Rm		Х	Х	Х	Х
ASR Rd, Rm, #	Rd = Rm >> # Rd = Rm >> Rs	signed	Х	Х	Х	
ASR Rd, Rs	PC = PC + (#OFF << 1)	signed	Х	Х	Х	
B <target addr=""></target>	PC = PC + (#OFF << 1)	Market State of	_			
B{ <cond>} <target addr=""> BIC Rm, Rd</target></cond>	Rd = Rd & !(Rm)	If <cond> is true</cond>	х	х		
	` ,	v5 only. v4 it does	X	X	Х	
BKPT #	CALL Breakpoint with #	nothing				
BL <target addr=""></target>	See Branching Description	-				
BLX <target addr=""></target>	See Branching Description	-				
BLX Rm	LR = (PC + 2) 1; PC = Rm[311] << 1; T=Rm[0]	-				
BX Rm	PC = Rm[311] << 1; T = Rm[0]	-				_
CMN Rm, Rn	<flags> = Rm + Rn</flags>	-	x	x	x	х
CMP Rm, Rn	<flags> = Rm - Rn</flags>	-	×	×	x	X
	-	Rm or Rn must be a				
CMP Rm, Rn	<flags> = Rm - Rn</flags>	*high register*	х	х	х	х
CMP Rn, #	<flags> = Rm - #</flags>	-	х	х	х	х
EOR Rd, Rm	Rd = Rd ^ Rm	-	Х	Х	Х	х
LDMIA Rn!, { <reg list="">}</reg>	for each in <reg list=""> = [Rn+=4]</reg>	-				
LDR Rd, [PC, #OFF]	Rd = [PC + (#OFF << 2)]	Word				
LDR Rd, [Rn, #OFF]	Rd = [Rn + (#OFF << 2)]	Word				
LDR Rd, [Rn, Rm]	Rd = [Rn + Rm]	Word				
LDR Rd, [SP, #OFF]	Rd = [SP + (#OFF << 2)]	Word				
LDRB Rd, [Rn, #OFF]	Rd = [Rn + (#OFF << 2)]	Unsigned Byte				
LDRB Rd, [Rn, Rm]	Rd = [Rn + Rm]	Unsigned Byte				
LDRH Rd, [Rn, #OFF]	Rd = [Rn + (#OFF << 2)]	Unsigned Halfw ord				
LDRH Rd, [Rn, Rm]	Rd = [Rn + Rm]	Unsigned Halfw ord				
LDRSB Rd, [Rn, Rm]	Rd = [Rn + Rm]	Signed Byte				
LDRSH Rd, [Rn, Rm]	Rd = [Rn + Rm]	Signed Halfw ord				
LSL Rd, Rm, #	Rd = Rm << #	Unsigned/Signed	х	х	х	
LSL Rd, Rs	Rd = Rm << Rs	Unsigned/Signed	х	х	х	
LSR Rd, Rm, #	Rd = Rm >> #	Unsigned	Х	Х	Х	
LSR Rd, Rs	Rd = Rm >> Rs	Unsigned	Х	Х	Х	
MOV Rd, #	Rd = #	Rd or Rm must be a	Х		Х	
MOV Rd, Rm	Rd = Rm	*high register*				
MUL Rd, Rm	Rd = Rd * Rm	-	Х	Х	х	
MVN Rd, Rm	Rd = !(Rm)	-	Х		Х	
NEG Rd, Rm	Rd = -(Rm)	-	Х	Х	Х	Х
ORR Rd, Rm	Rd = Rd Rm	-	Х	Х	Х	Щ
POP { <reg list="">, <pc>}</pc></reg>	get <reg list=""> and/or <pc> from stack</pc></reg>	-	_	_		
PUSH { <reg list="">, <lr>}</lr></reg>	put <reg list=""> and/or <lr> on stack</lr></reg>	-				Щ
ROR Rd, Rs	Rd = Rd > > Rs	-	Х	Х	Х	Щ
SBC Rd, Rm	Rd = (Rd - Rm) + C	-	Х	Х	Х	Х
STMIA Rn!, { <reg list="">}</reg>	[Rn+=4] = for each in <reg list=""></reg>	-				Щ
STR Rd, [Rn, #OFF]	[Rn + (#OFF << 2)] = Rd	w ord				Щ
STR Rd, [Rn, Rm]	[Rn + Rm] = Rd	w ord	_			Щ
STR Rd, [SP, #OFF]	[SP + (#OFF << 2)] = Rd	w ord	_	_		
STRB Rd, [Rn, #OFF]	[Rn + (#OFF << 2)] = Rd	byte				Н
STRB Rd, [Rn, Rm]	[Rn + Rm] = Rd [Rn + (#OFF << 2)] = Rd	byte halfw ord	_	_	_	H
STRH Rd, [Rn, #OFF]	[Rn + (#OFF << 2)] = Rd [Rn + Rm] = Rd	halfw ord halfw ord				Н
STRH Rd, [Rn, Rm] SUB Rd, #	Rn + Rmj = Ra Rd = Rd - #	nairw ord	х	х	х	х
	Rd = Rn - #	-	X	X	X	X
SUB Rd, Rn, # SUB Rd, Rn, Rm	Rd = Rn - Rm	-	X	X	X	X
SUB SP, #OFF	SP = SP - (#OFF << 2)		Ĥ	^	^	_
SWI #	Run "bios" function	-	H	H	H	H
TST Rm, Rn	<flags> = Rn & Rm</flags>	-	х		х	
		Free for software	Ĥ		Ĥ	-
		use. Minimal risk of				
Unused Opcode	none	future CPU revisions				
		turning this into an				
		opcode.				

Meaning	Mnemonic		Opc	cod	е	Status Flags
Equal	EQ	0	0	0	0	z = 1
Not Equal	NE	0	0	0	1	z = 0
Carry Set	cs	0	0	1	0	c = 1
Carry Clear	CC	0	0	1	1	c = 0
Unsigned Higher or Same	HS	0	0	1	0	c = 1
Unsigned Lower	LO	0	0	1	1	c = 0
Minus/Negative	MI	0	1	0	0	n = 1
Plus/Positive or Zero	PL	0	1	0	1	n = 0
Overflow	vs	0	1	1	0	v = 1
No Overflow	VC	0	1	1	1	v = 0
Unsigned Higher	HI	1	0	0	0	c = 1; z = 0
Unsigned Lower or Same	LS	1	0	0	1	c = 0; z = 1
Signed Greater Than or Equal	GE	1	0	1	0	n = v
Signed Less Than	LT	1	0	1	1	n != v
Signed Greater Than	GT	1	1	0	0	z = 0; n = v
Signed Less Than or Equal	LE	1	1	0	1	z = 1; n != v
Always	AL	1	1	1	0	-
Never	NE	1	1	1	1	-

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

ADC Rd. Rm			13	12	3	10				1	5 4 3	
ADC Rd, Rm	0	1	0	0	0	0	0	1	0	1	Rm	Rd
ADD Rd, #	0	0	1	1	0		Rd				#	
ADD Rd, PC, #OFF	1	0	1	0	0	Н	Rd	-		-	C Polativo (Vifnat
	_	-			·	Н	_	_			C Relative (
ADD Rd, Rm	0	1	0	0	0	1	0	0	H1	H2	Rm	Rd
ADD Rd, Rn, #	0	0	0	1	1	1	0		#	T	Rn	Rd
	-	0	0	1	1	0	0	_	Rm		Rn	Rd
	U					٥		ш	raii			- 10
ADD Rd, SP, #OFF	1	0	1	0	1		Rd			S	P Relative (Offset
AND Rd, Rm	0	1	0	0	0	0	0	0	0	0	Rm	Rd
AND RG, RIII	_		-			٥	٥	-	•	٥		- 10
ASR Rd, Rm, #	0	0	0	1	0			#			Rm	Rd
ASR Rd, Rs	0	1	0	0	0	0	0	1	0	0	Rs	Rd
	1	1	1	0	0	-	-	-	÷		Offset	_
B <target addr=""></target>	1	1		١.	٥					# '		
B{ <cond>} <target addr=""></target></cond>	1	1	0	1		CO	nd				# Offse	t
BIC Rm, Rd	0	1	0	0	0	0	1	1	1	0	Rn	Rm
	÷		÷						÷	-		
BKPT #	1	0	1	1	1	1	1	0			#	
BL <target addr=""></target>	1	1	1	1	1			#	Off	et	(lower ha	lf)
BL{X} <target addr=""> (+)</target>	1	1	1	1	0			#	Off.	at	(upper ha	lf\
	÷	Ė	_			Н						
BLX <target addr=""></target>	1	1	1	0	1			#			(lower ha	lf)
BLX Rm	0	1	0	0	0	1	1	1	1	H2	Rm	0 0
BX Rm	0	1	0	С	С	1	1	1	0	H2	Rm	0 0
		1	U	•	•				-			
CMN Rm, Rn	0	1	0	0	0	0	1	0	1	1	Rn	Rm
CMP Rm. Rn	0	1	0	0	0	0	1	0	1	0	Rn	Rm
		÷										
CMP Rm, Rn	0	1	0	0	0	1	0	1	H1	H2	Rn	Rm
CMP Rn, #	0	0	1	0	1		Rn				#	
EOR Rd, Rm	0	4	0	0	0	0	0	٥	٥	1	Rm	Rd
	٥	-	٥	,	,				U			
LDMIA Rn!, { <reg list="">}</reg>	1	1	0	0	1		Rn				Register L	ist
LDR Rd, [PC, #]	0	1	0	0	1		Rd			Р	C Relative (Offset
, (10, #)	-	÷	÷			_			-	=		
LDR Rd, [Rn, #OFF]	0	1	1	0	1		# (Offs	et		Rn	Rd
LDR Rd, [Rn, Rm]	0	1	0	1	1	0	0		Rm		Rn	Rd
LDR Rd, [SP, #OFF]	4	0	0	1	1	г	Dd	-		0	P Relative (Vifnot
	Ľ	U	U			_	Nu			٠		
LDRB Rd, [Rn, #OFF]	0	1	1	1	1			Offs	et		Rn	Rd
LDRB Rd, [Rn, Rm]	0	1	0	1	1	1	0	П	Rm		Rn	Rd
DDRD RU, [RH, RH]	_	_	_			-						
LDRH Rd, [Rn, #OFF]	1	0	0	0	1		# (Offs	et		Rn	Rd
LDRH Rd, [Rn, Rm]	0	1	0	1	1	0	1		Rm		Rn	Rd
	0	1	0	1	0	1	1	_	Rm		Rn	Rd
LDRSB Rd, [Rn, Rm]	Ü		-		1	9	1					
LDRSH Rd, [Rn, Rm]	0	1	0	1	1	1	1		Rm		Rn	Rd
LSL Rd, Rm, #	0	0	0	0	0	г	_	#			Rm	Rd
				-	-			-	÷			
LSL Rd, Rs	0	1	0	0	0	0	0	0	1	0	Rs	Rd
LSR Rd, Rm, #	0	0	0	0	1			#			Rm	Rd
LSR Rd, Rs	0	1	0	0	0	0	0	n	1	1	Rs	Rd
						۰	۰	۰	-		-10	1.00
MOV Rd, #	0	0	1	0	0		Rd				#	
MOV Rd, Rm	0	1	0	0	0	1	1	0	H1	H2	Rm	Rd
MUL Rd, Rm	0	1	0	0	0	0	1	1	0	1	Rm	Rd
								9				
MVN Rd, Rm	0	1	0	0	0	0	1	1	1	1	Rm	Rd
NEG Rd, Rm	0	1	0	0	0	0	1	0	0	1	Rm	Rd
opp nd no	0	1	0	0	0	0	1	1	0	0	Rm	Rd
ORR Rd, Rm	_		-	•	•	-			U	U		
POP { <reg list="">, <pc>}</pc></reg>	1	0	1	1	1	1	0	PC			Register L	ist
PUSH { <reg list="">, <lr>}</lr></reg>	1	0	1	1	С	1	С	ΙR			Register L	
	0	1	0	0	0	٠.	0	1	1	1		Rd
ROR Rd, Rs	~		0	1	0	-			-		Rs	
SBC Rd, Rm	0	1	C					1	1	0	Rm	
				0	0	0	0					Rd
CTMIN Day [-room lints]	4		-			0					Renister I	
STMIA Rn!, { <reg list="">}</reg>	1	1	0	0	0	0	Rn				Register L	ist
STR Rd, [Rn, #OFF]	1		-				Rn				Register L	
STR Rd, [Rn, #OFF]	Ŀ	1	0	0	0	0	Rn					ist
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rm]	0	1	0 1 0	0	0		# 0		et Rm		Rn Rn	list Rd Rd
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rm] STR Rd, [SP, #OFF]	0	1	0	0 1 1	0 0		Rn #0	Offs	Rm	S	Rn Rn P Relative (Rd Rd Offset
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rm] STR Rd, [SP, #OFF]	0	1	0 1 0	0	0		Rn #0		Rm	S	Rn Rn	list Rd Rd
STR Rd, [Rn, #0FF] STR Rd, [Rn, Rm] STR Rd, [SP, #0FF] STRB Rd, [Rn, #0FF]	0	1	0 1 0	0 1 1	0 0		Rn #0	Offs	Rm	S	Rn Rn P Relative (Rd Rd Offset
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rm] STR Rd, [SP, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, #OFF]	0 0 1 0	1 1 0 1	0 1 0 0 1	0 1 1 1 1	0 0 0 0	0	Rn # 0 Rd # 0	Offs	et Rm	S	Rn Rn P Relative C Rn Rn	Rd Rd Offset Rd Rd
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rm] STR Rd, [SF, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Rm] STRH Rd, [Rn, #OFF]	0 0 1 0 0	1 1 0 1	0 1 0 0 1 0	0 1 1 1 1	0 0 0 0	0	Rn # 0 Rd # 0	Offs	et Rm	S	Rn Rn P Relative (Rn Rn Rn	Rd Rd Offset Rd Rd Rd Rd
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rm] STR Rd, [SF, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Rm] STRH Rd, [Rn, #OFF]	0 0 1 0	1 1 0 1	0 1 0 0 1	0 1 1 1 1	0 0 0 0	0	Rn # 0 Rd # 0	Offs	et Rm	S	Rn Rn P Relative C Rn Rn	Rd Rd Offset Rd Rd
STR Rd, [Rn, #0FF] STR Rd, [Rn, Rm] STR Rd, [SP, #0FF] STRB Rd, [Rn, #0FF] STRB Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF]	0 0 1 0 0	1 1 0 1	0 1 0 0 1 0	0 1 1 1 1	0 0 0 0	0	Rn # 0 Rd # 0	Offs	et Rm	S	Rn Rn P Relative (Rn Rn Rn	Rd Rd Offset Rd Rd Rd Rd
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rm] STR Rd, [SP, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Rm] STRH Rd, [Rn, #OFF] STRH Rd, [Rn, Rm]	0 0 1 0 0 1 0	1 1 0 1 1 0 1 0	0 1 0 0 1 0 0	0 0 1 1 1 1 0 1 1 1	0 0 0 0 0 0 1	1	Rn #(0 0 Rd #(0 1 1 Rd 1	Offs	et Rm et	S	Rn Rn PRelative (Rn Rn R	Rd Rd Offset Rd Rd Rd Rd Rd Rd
STR Rd, [Rn, #0FF] STR Rd, [SP, #0FF] STRB Rd, [SP, #0FF] STRB Rd, [Rn, #0FF] STRB Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF]	0 0 1 0 0 1 0	1 1 0 1 1 0 0	0 1 0 0 1 0 0 0	0 0 1 1 1 0 1 1 1 1	0 0 0 0 0 0	0 1 1	Rn #(0 0 Rd #(0 1 1 Rd 1	Offs	et Rm et Rm	S	Rn Rn Rn P Relative (Rn Rn Rn Rn Rn Rn Rn	Rd Rd Rd Pd Rd Rd Rd Rd Rd Rd Rd Rd Rd
STR Rd, [Rn, #0FF] STR Rd, [SP, #0FF] STRB Rd, [SP, #0FF] STRB Rd, [Rn, #0FF] STRB Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF] STRH Rd, [Rn, #0FF]	0 0 1 0 0 1 0	1 1 0 1 1 0 1 0	0 1 0 0 1 0 0	0 0 1 1 1 1 0 1 1	0 0 0 0 0 0 1	0 1 0	Rn #0 0 Rd #0 1 Rd 1 1	Offs	et Rm et	S	Rn Rn Rn P Relative (Rn Rn Rn Rn Rn Rn Rn Rn Rn	Rd Rd Offset Rd
STR Rd, [Rn, #0FF] STR Rd, [Rn, Rn] STR Rd, [Rn, #0FF] STRB Rd, [Rn, #0FF] STRB Rd, [Rn, Em] STRH Rd, [Rn, Em] SUB Rd, # [Rn, Rm] SUB Rd, # [Rn, Rm] SUB Rd, Rn, # [Rn]	0 0 1 0 0 1 0 0	1 1 0 1 1 0 0 0 0	0 1 0 0 1 0 0 0 1	0 0 1 1 1 1 0 1 1	0 0 0 0 0 0 0	0 1 0	Rn #0 0 Rd #0 1 Rd 1 1	Offs	Rm et Rm et Rm	S	Rn Rn Rn P Relative (Rn Rn Rn Rn Rn Rn Rn Rn Rn	Rd Rd Offset Rd
STR Rd, [Rn, #00FF] STR Rd, [SP, #00FF] STR Rd, [SP, #00FF] STRB Rd, [Rn, #00FF] STRB Rd, [Rn, Em] STRH Rd, [Rn, Em] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STR Rd, Rn, Rm SUB Rd, Rn, Rm	0 0 1 0 0 1 0	1 1 0 1 1 0 0	0 1 0 0 1 0 0 0 0	0 0 1 1 1 1 0 1 1 1	0 0 0 0 0 0 0 1 1	0 1 0 0 0	Rn #0 0 Rd #0 1 1 Rd 1 1 0	Offs Offs Offs	et Rm et Rm	S	Rn Rn P Relative (Rn	Rd Rd Offset Rd
STR RA, [RM, #00FF] STR RA, [RM, RM] STR RA, [RM, B0FF] STRB RA, [RM, B0FF] STRB RA, [RM, RM] STRH RA, [RM, RM] STRH RA, [RM, RM] SUB RA, RM, RM SUB RA, RM, RM SUB RA, RM, RM SUB RA, RM, RM SUB RB, RM, RM SUB RB, SP, SP, #0FF	0 0 1 0 0 1 0 0 0 0	1 1 0 1 1 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 1 1 1	0 1 0 0 1	Rn #(0 0 #(0 1 1 1 0 1 1 1 0 1 1 1 1 0 1 1 1 1 1 1	Offs Offs 0	et Rm et Rm		Rn R	Rd Rd Offset Rd
STR Rd, [Rn, #00FF] STR Rd, [SP, #00FF] STR Rd, [SP, #00FF] STRB Rd, [Rn, #00FF] STRB Rd, [Rn, Em] STRH Rd, [Rn, Em] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STR Rd, Rn, Rm SUB Rd, Rn, Rm	0 0 1 0 0 1 0 0	1 1 0 1 1 0 0 0 0	0 1 0 0 1 0 0 0 0	0 0 1 1 1 1 0 1 1 1	0 0 0 0 0 0 0 1 1	0 1 0 0 0	Rn #0 0 Rd #0 1 1 Rd 1 1 0	Offs Offs Offs	Rm et Rm et Rm	0	Rn Rn P Relative (Rn	Rd Rd Offset Rd
STR Rd, [Rn, #00FF] STR Rd, [Rn, Rn] STR Rd, [Rn, #00FF] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] SUB Rd, R, R, # SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB SP, SP, #0FF	0 0 1 0 0 1 0 0 0 0	1 1 0 1 1 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 1 1 1 0	0 1 0 0 1 0	Rn #0 0 Rd #0 1 1 1 1 1 1	Offs Offs Offs	et Rm et Rm f Rm 1	0	Rn Rn Rn P Relative C Rn	Rd R
STR Rd, [Rn, #OPF] STR Rd, [Rn, Rm] STR Rd, [SP, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRB Rd, Rn, Rm SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB SP, SP, #OFF SMI # TST Rm, Rn Unpredictable	0 0 1 0 0 1 0 0 0 0 1 1 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1	0 1 0 0 1 0 0 0 1 0 0 0	0 0 1 1 1 1 0 1 1 1 1 1 0 0	0 0 0 0 0 0 0 1 1 1 0	0 1 0 0 1 0	Rn #0 0 Rd #0 1 Rd 1 1 0 1 1	Offs Offs Offs Offs Offs Offs	et Rm et Rm # Rm 1	0	Rn R	Rd R
STR Rd, [Rn, #0FF] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, #0FF] STRB Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] SUB Rd, # SUB Rd, Rn, # SUB Rd, Rn, Rm SUB Rd, Rn, Rm UB Pd, Rn, Rm UB Pd, Rn, Rm UB Rd, Rn, Rm	0 0 1 0 0 1 0 0 0 0	1 1 0 1 1 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0	0 1 0 1 0 0 1	Rn #0 0 Rd #0 1 1 1 0 0 0	Offs Offs Offs Offs Offs Offs Offs Offs	et Rm et Rm 1	0 0	Rn Rn Rn P Relative C Rn	Rd R
STR Rd, [Rn, #OFF] STR Rd, [Rn, Rn] STR Rd, [Rn, BoFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Em] STRH Rd, [Rn, Em] STRH Rd, [Rn, Rm] SUB Rd, # SUB Rd, Rn, # SUB Rd, Rn, Em SUB Rd, Rn, Em SUB Rd, Rn, Em UB Rd, Em, Rn UB Rd, Rn, Rn	0 0 1 0 0 1 0 0 0 0 1 1 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1	0 1 0 0 1 0 0 0 1 0 0 0	0 0 1 1 1 1 0 1 1 1 1 1 0 0	0 0 0 0 0 0 0 1 1 1 0	0 1 0 0 1 0	Rn #0 0 Rd #0 1 Rd 1 1 0 1 1	Offs Offs Offs Offs Offs Offs	et Rm et Rm # Rm 1	0	Rn R	Rd R
STR Rd, [Rn, #OPF] STR Rd, [Rn, Rm] STR Rd, [SP, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRB Rd, Rn, Rm] SUB Rd, # SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB SP, SP, #OFF SMI # Unpredictable Unpredictable Unpredictable	0 0 1 0 0 1 0 0 0 0 0 1 1 1 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1 1 1	0 1 0 0 1 0 0 0 1 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 1 1 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0	0 1 0 0 1 0 1	Rn #0 0 Rd #0 1 1 0 0 1 1	Offs Offs Offs Offs Offs Offs Offs Offs	Rm et Rm et Rm 0 0 0	0 0 0	Rn R	Rd R
STR Rd, [Rn, #0FF] STR Rd, [Rn, Rm] STR Rd, [Rn, BOFF] STRB Rd, [Rn, Rm] STRB Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB RD, Rn, Rm SUB RD, Rn, Rm UND RD, SP, SP, #0FF SWI #4 TST Rm, Rn Unpredictable Unpredictable Unpredictable Unpredictable	0 0 1 0 0 0 1 0 0 0 0 1 1 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1 1 1	0 1 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0 0	0 1 0 0 1 0 1 1 1 1	Rn #(0 0 Rd #(0 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Offs Offs	Rm et Rm f Rm 0 0 0 x	0 0 0	Rn R	Rd R
STR Rd, [Rn, #OPF] STR Rd, [Rn, Rm] STR Rd, [SP, #OPF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STB Rd, # SUB Rd, # SUB Rd, Rn, Rm SUB SP, SP, #OFF SWI # STF RM, RM Unpredictable Unpredictable Unpredictable	0 0 1 0 0 1 0 0 0 0 0 1 1 1 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1 1 1	0 1 0 0 1 0 0 0 1 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 1 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0 0 0 0	0 1 0 0 1 0 0 1 1 1 1	Rn #(0 0 Rd #(0 1 1 1 0 0 1 1 1 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 1 0	Offs Offs Offs Offs Offs Offs Offs Offs	et Rm et Rm 1 0 0 0 0 x	0 0 0 0 x x	Rn R	Rd R
STR Rd, [Rn, #00FF] STR Rd, [Rn, Rm] STR Rd, [Rn, #00FF] STRB Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STHH Rd, [Rn, Rm] SUB Rd, R, Rm SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB Rd, Rn, Rm UND Rd, Rn, Rm Unpredictable Unpredictable Unpredictable Unpredictable Unpredictable Unpredictable	0 0 1 0 0 1 0 0 0 0 0 1 1 1 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1 1 1 1 1	0 1 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0 0	0 1 0 0 1 0 1 1 1 1	Rn #0 0 Rd #0 1 1 1 0 0 1 1 1 1	Offs Offs	Rm et Rm f Rm 0 0 0 x	0 0 0	Rn R	Rd R
STR Rd, [Rn, #00FF] STR Rd, [Rn, Rm] STR Rd, [SP, #00FF] STRB Rd, [Rn, #00FF] STRB Rd, [Rn, Em] STRH Rd, [Rn, Em] STRH Rd, [Rn, Em] STRH Rd, [Rn, Rm] STRH Rd, Rn, Rm] SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB SP, SP, #00FF SWI # Unpredictable Unpredictable Unpredictable Unpredictable Unpredictable Unpredictable Unpredictable Unpredictable Unpredictable	0 0 1 0 0 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0 0 0 0	0 1 0 1 0 1 1 1 1 1 1 0 x	#(0 0 #(0 1 1 1 0 0 1 1 0 1 1 0 1 1 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 1 1 0	Offs Offs Offs Offs Offs Offs Offs Offs	et Rm et Rm 0 0 0 x x	0 0 0 0 x x	Rn R	Rd R
STR Rd, [Rn, #0FF] STR Rd, [Rn, Rm] STR Rd, [Rn, Rm] STR Rd, [Rn, #0FF] STRB Rd, [Rn, Rm] STRH Rd, [Rn, Rm] STRH Rd, [Rn, Rm] SUB Rd, # SUB Rd, Rn, # SUB Rd, Rn, Rm SUB Rd, Rn, Rm Unpredictable	0 0 1 0 0 1 0 0 0 0 0 1 1 0 0 0 0 0 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1 1 1 1 1 1 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0	0 1 0 0 1 1 0 0 1 1 1 1 0 x	#0 0 #0 1 1 1 0 1 1 0 1 1 1 0	Offs Offs Offs 1 Offs 1 X X	et Rm et Rm 1 0 0 0 0 x x x x x	0 0 0 0 x x	Rn R	Rd R
STR Rd, [Rn, #OPF] STR Rd, [Rn, Rm] STR Rd, [SP, #OFF] STRB Rd, [Rn, #OFF] STRB Rd, [Rn, Em] SUB Rd, # SUB Rd, Rn, Rm SUB Rd, Rn, Rm SUB SP, SP, #OFF SMI # "TST Rm, Rn Unpredictable	0 0 1 0 0 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0	1 1 0 1 1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0 0 0 0	0 1 0 1 0 1 1 1 1 1 1 0 x	#(0 0 #(0 1 1 1 0 0 1 1 0 1 1 0 1 1 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 1 1 0	Offs Offs Offs Offs Offs Offs Offs Offs	et Rm et Rm 0 0 0 x x	0 0 0 0 x x	Rn R	Rd R