DIGITAL CLOCK DESIGN

24Hrs Format

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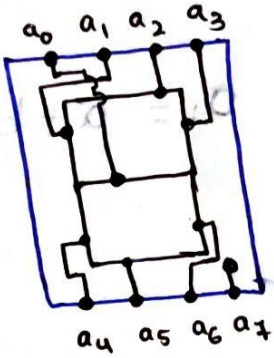
Objective:

To Design Digital clock in 24 Hrs Format (HH:MM:SS)

➡ The numbers should be displayed using 7-segment display.

Behaviour of 7-segment display in Logisim:

Displays the values of its eight one-bit inputs. When an input is 1, it colors the corresponding "segments" of the Component.



We have to design a decoder circuit such that when input is '0', the output should be in such a way that it displays '0' on the seven-segment display.

Truth table for the decoder circuit:

Inputs				Outputs						
a	b	c	d	a_0	a_1	a_2	a_3	a_4	a_5	a_6
0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	1	0	0	1
0	0	1	0	1	0	1	1	1	1	0
0	0	1	1	1	0	1	1	0	1	1
0	1	0	0	1	1	0	1	0	0	1
0	1	0	1	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	1	1	1
0	1	1	1	1	0	1	1	0	0	1
1	0	0	0	0	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x

Logical expressions for the inputs of seven segment display

K-Map for a_0:

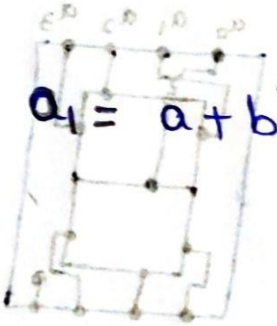
ab \ cd	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

$$a_0 = a + \bar{b}c + b\bar{c} + b\bar{d}$$

K-Map for a_1:

ab \ cd	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

$$a_1 = a + b\bar{d} + b\bar{c} + \bar{c}\bar{d}$$



K-Map for a_2:

ab \ cd	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

$$a_2 = a + bd + c + \bar{b}\bar{d}$$

K-Map for a_3:

ab \ cd	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	X	X	X	X
10	1	1	X	X

$a_3 = \bar{b} + \bar{c}\bar{d} + c \cdot d$

K-Map for a_4:

ab \ cd	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	X	X
10	1	0	X	X

$a_4 = \bar{b}\bar{d} + c\bar{d}$

K-Map for a_5:

ab \ cd	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	1	X	X

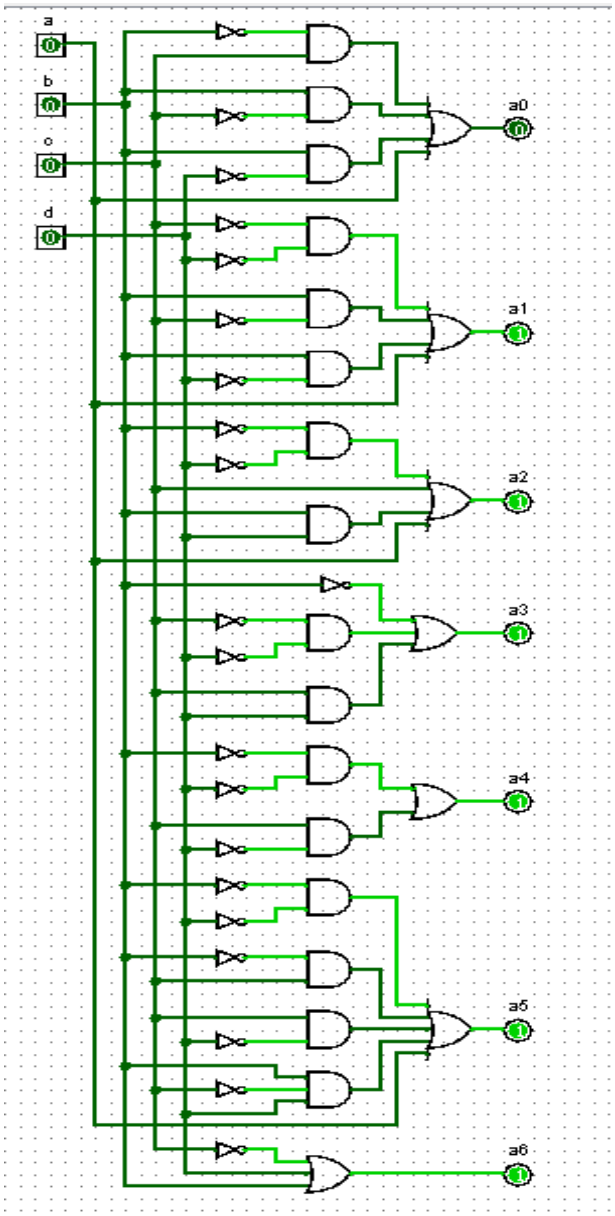
$a_5 = \bar{b}\bar{d} + \bar{b}c + c\bar{d} + b\bar{c}d +$
a

K-Map for a_6:

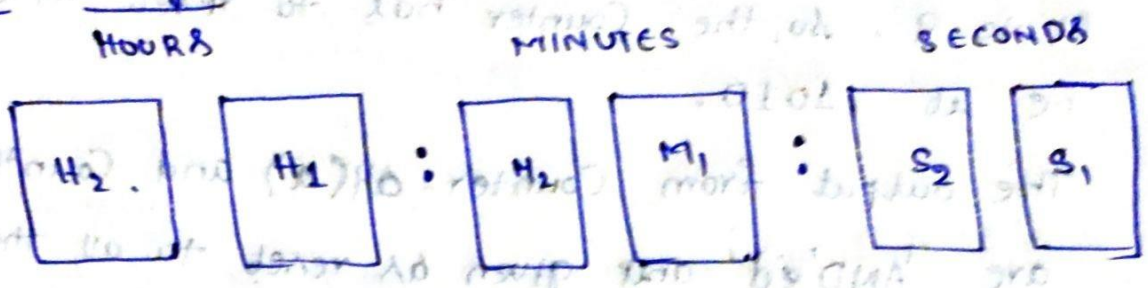
ab \ cd	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$a_6 = \cancel{b\bar{c}\bar{d}}\ b + \bar{c} + d$

Internal circuit for the decoder:

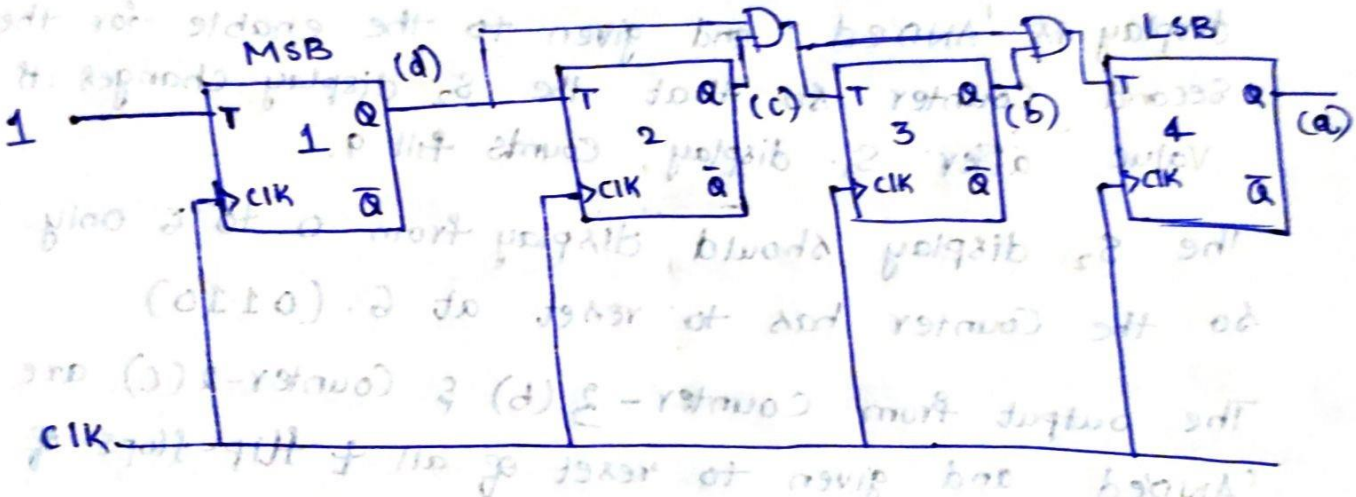


Clock design:



* The inputs for the decoder circuit are given from synchronous Counter.

Basic design for Counter: (using T flip-flop)



Toggle - flip flop:

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic table:

T	Q_{n+1}
0	$Q(t)$
1	$\overline{Q(t)}$

$$Q(t+1) = T \oplus Q(t)$$

$$= TQ' + T'Q$$

All flip-flops are triggered simultaneously by the clock inputs pulses.

After each cycle the output of Counter changes by one it goes from (0000 to 1111).

⇒ For the S_1 display we have to display from 0 to 9. So, the Counter has to reset after 9. i.e at 1010.

The output from Counter-4(a) and Counter-2(c) are 'AND'ed and given as reset to all the flip-flops

⇒ For the S_2 display it should change the value only when the S_1 display counts till 9. So, (1001)

The output from Counter-4(a) and Counter-1(d) of S_1 display is 'AND'ed and given to the enable for the second Counter so that the S_2 display changes its value after S_1 display counts till 9.

The S_2 display should display from 0 to 6 only. So the Counter has to reset at 6. (0110)

The output from Counter-3(b) & Counter-2(c) are 'ANDed and given to reset of all 4 flip-flops of S_2 display Counter.

⇒ For M_1 display the value should change only after 1 minute i.e after only when the seconds display show('5', '9').

↓ S_2 ↓ S_1

5 from S_2 (0101 → counter-1(d) & Counter-3(b) are 'ANDed)

& 9 from S_1 (1001 → Counter-4(a) & Counter-1(d) are 'ANDed)

are 'AND'ed and given as enable to M_1 display.

Just like S_1 display, M_1 display should also reset after 9.

⇒ Just like S_2 display, M_2 display should display from 0 to 6 only. So, Counter is resseted at 6 like S_2 and should change its value after M_1 has displayed & S_1 S_2 seconds display show ('5', '9'). The enable of S_1 & '9' from M_1 are 'AND'ed and given as

enable for M_2.

⇒ For H_1 display it should only changes value after 1 hour (i.e Minutes and seconds display show 59 & 59).
M_2 M_1 S_2 S_1

The Enable is given from the output of 'AND' gate whose inputs are Enable of M_2 display & 5 (0101) from M_2 (AND of Counter-1(d) & Counter-3(b)).

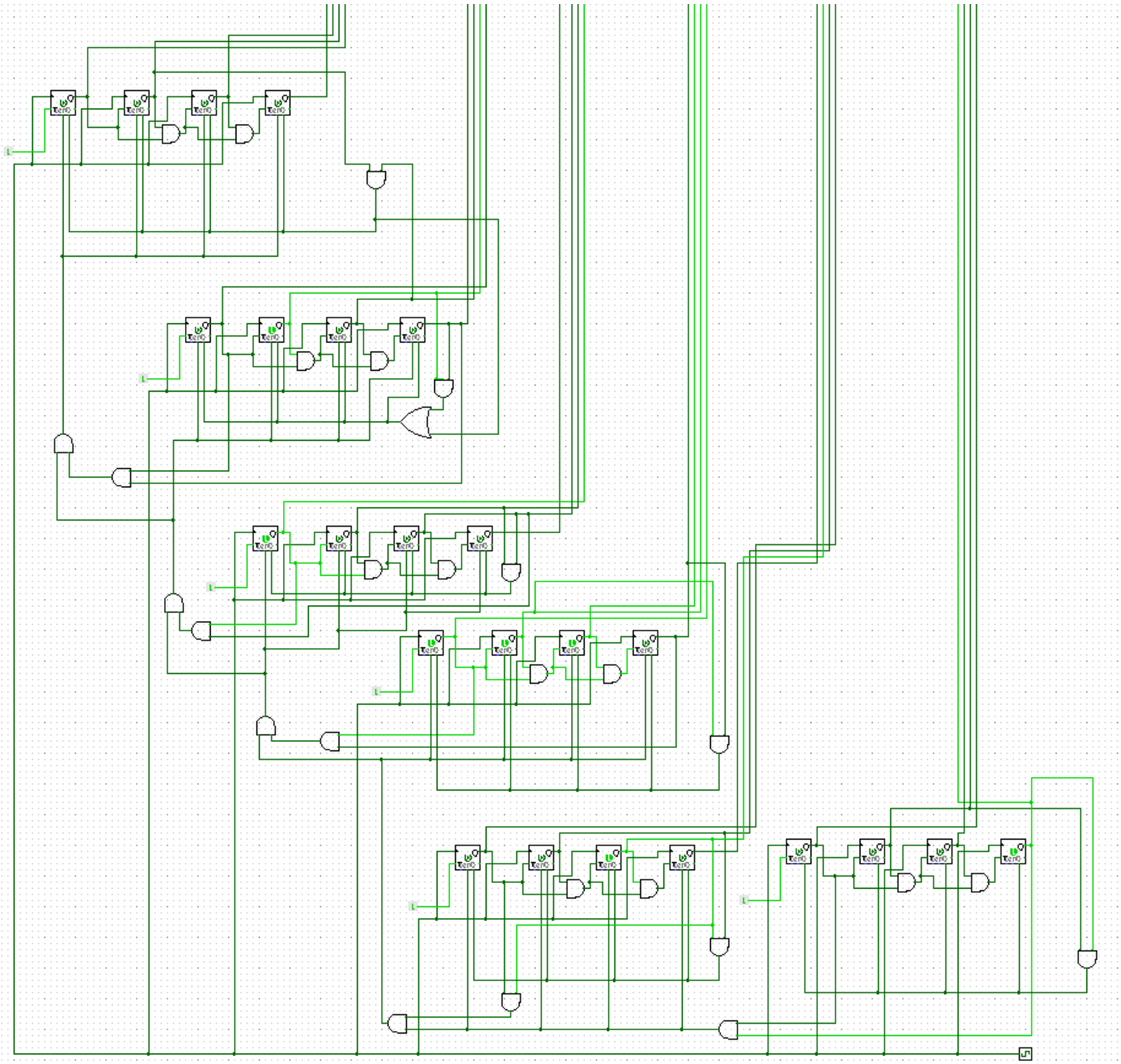
The reset for the H_1 display should be given after 9 also when the clock finishes one day (24). ie when H_2 displays shows '2' & H_1 shows '4'.

⇒ For H_2 display. it should change its only when H_1 shows 9 & minules shows 59 & seconds also show 59
M_2 M_1 S_2 S_1

So, the enable H_1 display and '9' from H_1 are 'ANDed and given to H_2 display enable.

The H_2 display should reset at 24. So, '2' from H_2 & '4' from M_2 are 'ANDed and given as reset to H_2.
H_2 H_1

⇒ Since we are designing a synchronous clock, the clock for the Counters should be same.



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