Soft Error Resilient 16T SRAM Arrays in45nm & 65nm CMOS for Aerospace Applications

A Project Work

Submitted in partial fulfillment of Requirements for the Award of the Degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS & COMMUNICATION ENGINEERING

BY

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CERTIFICATE

This is to certify that the project work entitled "**Grading Of Diabetic Retinopathy Using Deep Learning**" is a bonafide record of project work done jointly by K.Tulasi Ram (208T1A0476), V. Ram Karthik (218T1A04A)), K. Siva Rama Krishna (218T1A0473), P. Jeevan Kumar(218T1A0489) under my guidance and supervision and is submitted in partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology in Electronics & Communication Engineering by **Jawaharlal Nehru Technological University, Kakinada during the academic year 2024-2025**.

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We thank one and all who have rendered help directly or indirectly in the completion of this project successfully.

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DECLARATION

I declare that this project report titled "**Soft Error Resilient 16T SRAM Arrays in45nm & 65nm CMOS for Aerospace Applications"** is submitted in partial fulfilment of the degree of **B. Tech in Electronics and Communication Engineering** is a record of original work carried out by us under the supervision of **Mr. Ramesh Babu** and has not formed the basis for the award of any other degree or diploma, in this or any other Institution or University. In keeping with the ethical practice in reporting scientific information, due acknowledgments have been made wherever the findings of others have been cited.

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Soft-Error Aware SRAM with Multinode Upset Tolerance for Aerospace Applications

Base paper abstract:

As technology scales down, the critical charge (QC) of vulnerable nodes decreases, making SRAM cells more susceptible to soft errors in the aerospace industry. This article proposes a Soft-Error-Aware 16T (S8P8N) SRAM cell for aerospace applications to address this issue. The properties of S8P8N are evaluated and compared with 6T, DICE, QUCCE12T, WEQUATRO, RHBD10T, RHBD12T, S4P8N, SEA14T, and SRRD12T. Simulation results indicate that all vulnerable nodes and key node pairs of the proposed cell can recover to their original states when affected by a soft error. Additionally, it can recover from key multinode upsets. The write speed of the proposed cell is found to be reduced by 20.3%, 50.1%, 74.1%, 63.7%, and 50.41% compared to 6T, DICE, QUCCE12T, WEQUATRO, and RHBD10T, respectively. The read speed of the proposed cell is found to be reduced by 56.6%, 52.2%, 62.5%, and 35.2% compared to 6T, SRRD12T, RHBD12T, and S4P8N, respectively. It also shows that the hold power of the proposed cell is found to be reduced by 14.1%, 13.8%, 17.7%, and 23.4% compared to DICE, WEQUATRO, RHBD10T, and RHBD12T. Furthermore, the read static noise margin (RSNM) of the proposed cell is found to be enhanced by 157%, 67%, and 32% compared to RHBD12T, SEA14T, and SRRD12T. All these improvements are achieved with a slight area penalty.

Improvement of this project:

- To developed single bit 16T SRAM design using 45nm and 65nm CMOS Technology.
- To developed 8x8 array SRAM architecture which using 45nm and 65nm CMOS Technology and compare the parameters in terms of area, delay and power.

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DHANEKULA INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics & Communications Engineering

VISION-MISSION-PEOs

VISION/MISSION/PEOs

Institute Vision	Pioneering Professional Education through Quality
Institute Mission	• Providing Quality Education through state-of-art infrastructure, laboratories, and comm-[itted staff. • Moulding Students as proficient, competent, and socially responsible engineering personnel with ingenious intellect. • Involving faculty members and students in research and development works for the betterment of society.
Department Vision	Be a model in the arena of Electronics and Communication Engineering Education & Research to Elevate Rural Community

Departme nt Mission	• Imparting professional education endowed with ethics and human values to transform students to be competent and committed electronics engineers. • Adopting best pedagogical methods to maximize knowledge transfer. • Having adequate mechanisms to enhance understanding of theoretical concepts through practice. • Establishing an environment conducive for lifelong learning and entrepreneurship development. • To train as effective innovators and deploy new technologies for service of society.
Program Educational Objectives (PEO's)	PEO1: Shall have professional competency in electronics and communications with strong foundation in science, mathematics and basic engineering. PEO2: Shall design, analyze and synthesize electronic circuits and simulate using modern tools. PEO3: Shall Discover practical applications and design innovative circuits for Lifelong learning PEO4: Shall have effective communication skills and practice the ethics consistent with a sense of social responsibility.

DHANEKULA INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics & Communications Engineering

POs/PSOs

PROGRAM OUTCOMES

1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and engineering programs.
2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex Engineering problems reaching substantiated conclusions using first principles of Mathematics, natural sciences, and engineering sciences
3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, and societal considerations.
4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis, and synthesis of the information to provide valid conclusions.
5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6	**The engineer and society**: Apply to reason informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues, and the consequent responsibilities relevant to the professional engineering practice.
7	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9	**Individual and teamwork**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10	**Communication**: Communicate effectively on complex engineering activities with the Engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12	**Lite-long learning**: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO's)

PSO1: Make use of specified software tool for designing and developing VLSI and Embedded Systems.

PSO2: Innovate and Design application specific electronic circuits for modern wireless communication.

Project vs. POs Mapping

Project title	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
Soft Error Resilient 16T SRAM Arrays in45nm & 65nm CMOS for Aerospace Applications	2	3	3	3	3	2	3	-	3	3	3	3

3-High 2-Medium 1-Low

Justification of Mapping of Project with Program Outcomes:

1. The knowledge of mathematics, science, engineering fundamentals, and engineering Programs are strongly correlated to all course outcomes.
2. Application of Ethical principles is not correlated to all course outcomes.

Project vs. PSOs Mapping

Project Title	PSO 1	PSO 2
Soft Error Resilient 16T SRAM Arrays in45nm & 65nm CMOS for Aerospace Applications	2	3

Soft Error Resilient 16T SRAM Arrays in45nm & 65nm CMOS for Aerospace Applications

Abstract:

In this research, we present the **Soft Error Resilient 16T SRAM Arrays in45nm & 65nm CMOS for Aerospace Applications.** Aerospace environments are highly susceptible to radiation-induced soft errors, demanding the development of robust memory systems. We begin by designing a single-bit 16T SRAM cell optimized for multinode upset tolerance, incorporating advanced error correction and radiation-hardening techniques to enhance reliability. The single-bit cell design is then scaled to an 8x8 SRAM array architecture. Both the 45nm and 65nm versions of the array are developed and simulated to evaluate key performance metrics, including area, delay, and power consumption. The results indicate that while 45nm technology achieves better performance and area efficiency, 65nm technology excels in power savings and reliability. This comprehensive study underscores the importance of technology selection in optimizing SRAM design for high-reliability aerospace applications, offering a framework for future advancements in radiationhardened memory systems.

1.CHAPTER
Introduction to VLSI design

1.1 What is VLSI?

VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas. VLSI, circuits that would have taken board furls of space can now be put into a small space few millimeters across! VLSI circuits are everywhere ... your computer, your car, your brand new state-of-the-art digital camera, the cellphones, and what have you. All this involves a lot of expertise on many fronts within the same field, which we will look at in later sections.

1.1.1 Dealing with VLSI Circuits

The way normal blocks like latches and gates are implemented is different from what students have seen so far, but the behavior remains the same. All the miniaturization involves new things to consider. A lot of thought has to go into actual implementations as well as design.

Circuit Delays: Large complicated circuits running at very high frequencies have one big problem to tackle - the problem of delays in propagation of signals through gates and wire even for areas a few micrometers across! The operation speed is so large that as the delays add up, they can actually become comparable to the clock speeds.

Power: Another effect of high operation frequencies is increased consumption of power. This has two-fold effect - devices consume batteries faster, and heat dissipation increases. Coupled with the fact that surface areas have decreased, heat poses a major threat to the Stability of the circuit itself. electronics. What's so special in our case is that there are many possible ways to do this; **Layout:** Laying out the circuit components is task common to all branches of there can be multiple layers of different materials on the same silicon, there can be different arrangements of the smaller parts for the same component and soon. The choice between the two is determined by the way we chose the layout the circuit components. Layout can also affect the fabrication of VLSI chips, making it either easy or difficult to implement the components on the silicon.

1.2Introduction to VHDL

A digital system can be described at different levels of abstraction and from different points of view. An HDL should faithfully and accurately model and describe a circuit, whether already built or under development, from either the structural or behavioral views, at the desired level of abstraction. Because HDLs are modeled after hardware, their semantics and use are very different from those of traditional programming languages.

1.1.1 **Limitations of traditional programming languages**

There are wide varieties of computer programming languages, from Frontend to C to Java. Unfortunately, they are not adequate to model digital hardware. To understand their limitations, it is beneficial to examine the development of a language. A programming language is characterized by its syntax and semantics. The syntax comprises the grammatical rules used to write a program, and the semantics is the "meaning" associated with language constructs. When a new computer language is developed, the designers first study the characteristics of the underlying processes and then develop syntactic constructs and their associated semantics to model and express these characteristics.

Most traditional general-purpose programming languages, such as C, are modeled after a sequential process. In this process, operations are performed in sequential order, one operation at a time. Since an operation frequently depends on the result of an earlier operation, the order of execution cannot be altered at will. The sequential process model has two major benefits. At the abstract level, it helps the human thinking process to develop an algorithm step by step. At the implementation level, the sequential process resembles the operation of a basic computer model and thus allows efficient translation from an algorithm to machine instructions.

VHDL includes facilities for describing logical structure and function of digital systems at a number of levels of abstraction, from system level down to the gate level. It is intended, among other things, as a modeling language for specification and simulation. We can also use it for hardware synthesis if we restrict ourselves to a subset that can be automatically translated into hardware.

VHDL arose out of the United States government's Very High Speed Integrated Circuits (VHSIC) program. In the course of this program, it became clear that there was a need for a standard language for describing the structure and function of integrated circuits (ICs). Hence the VHSIC Hardware Description Language (VHDL) was developed. It was subsequently developed further under the auspices of the Institute of Electrical and Electronic Engineers (IEEE) and adopted in the form of the IEEE Standard 1076, Standard VHDL Language Reference Manual, in 1987. This first standard version of the language is often referred to as VHDL-87.

After the initial release, various extensions were developed to facilitate various design and modeling requirements. These extensions are documented in several IEEE standards:

i. IEEE standard 1076.1-1999, VHDL Analog and Mixed Signal Extensions (VHDL-AMS): defines the extension for analog and mixedsignal modeling.

ii. IEEE standard 1076.2-1996, VHDL Mathematical Packages: defines extra mathematical functions for real and complex numbers.

iii. IEEE standard 1076.3- 1997, Synthesis Packages: defines arithmetic operations over a collection of bits.

iv. IEEE standard 1076.4-1995, VHDL Initiative towards ASK Libraries (VITAL): defines a mechanism to add detailed timing information to ASIC cells.

v. IEEE standard 1076.6-1999, VHDL Register Transfer Level (RTL)
Synthesis: defines a subset that is suitable for synthesis.

vi. IEEE standard 1 164- 1993 Multivalve Logic System for VHDL Model Interoperability (std-logicJl64): defines new data types to model multivalve logic.

vii. IEEE standard 1029.1-1998, VHDL Waveform and Vector Exchange to Support Design and Test Verification (WAVES): defines how to use VHDL to exchange information in a simulation environment.

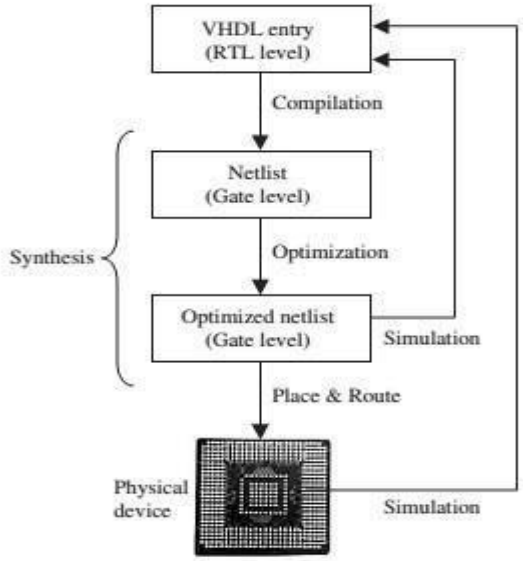


Figure 1 : Summary of VHDL design flow

1.3 Electronic Design Automation

There are several EDA (Electronic Design Automation) tools available for circuit synthesis, implementation, and simulation using VHDL. Some tools(place and route, for example) are ordered as part of a vendor's design suite (e.g., Altera's Quartus II, which allows the synthesis ofVHDL code onto Altera's CPLD/FPGA chips, or Xilinx's ISE suite, for Xilinx's CPLD/FPGA chips). Other tools (synthesizers, for example), besides being ordered as part of the design suites, can also be provided by specialized EDA companies (Mentor Graphics, Synopsis, Simplicity, etc.). Examples of the latter group are Leonardo Spectrum (a synthesizer from Mentor Graphics), Simplify (a synthesizer from Simplicity), and Modelsim (a simulator from Model Technology, a Mentor Graphics company). The designs presented in the book were synthesized CPLD/FPGA devices (appendix A) either from Altera or Xilinx. The tools used were either ISE combined with ModelSim, MaxPlus II combined with Advanced. Synthesis Software or Quartus II. Leonardo Spectrum was also used occasionally. Although different EDA tools were used to implement and test the examples presented in the design, we decided to standardize the visual presentation of all simulation graphs. Due to its clean appearance, the waveform editor of MaxPlus I was employed. However, newer simulators like ISE þ ModelSim and Quartus II, over a much

broader set of features, which allow, for example, a more refined timing analysis. For that reason, those tools were adopted when examining the fine details of each design.

1.4 Field-Programmable Gate Array

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

For any given semiconductor process, FPGAs are usually slower than their fixed ASIC counterparts. They also draw more power, and generally achieve less functionality using a given amount of circuit complexity. But their advantages include a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. Vendors can also take a middle road by developing their hardware on ordinary FPGAs, but manufacture their final version so it can no longer be modified after the design has been committed.

Field Programmable Gate Array (FPGA) devices were introduced by Xilinx in the mid-1980s. They differ from CPLDs in architecture, storage technology, number of built-in features, and cost, and are aimed at the implementation of high performance, large-size circuits.

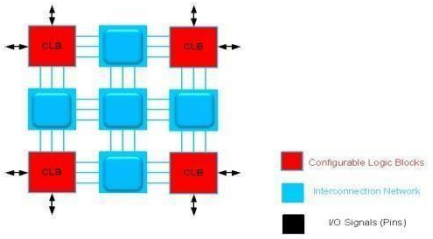


Figure 2 : FPGA Architecture

The basic architecture of an FPGA is illustrated in figure 2. It consists of a matrix of CLBs (Configurable Logic Blocks), interconnected by an array of switch matrices.

The internal architecture of a CLB is different from that of a PLD First, instead of implementing SOP expressions with AND gates followed by OR gates (like in SPLDs), its operation is normally based on a LUT (lookup table).

Moreover, in an FPGA the number of flip-flops is much more abundant than in a CPLD, thus allowing the construction of more sophisticated sequential circuits. Besides JTAG support and interface to diverse logic levels, other additional features are also included in FPGA chips, like SRAM memory, clock multiplication (PLL or DLL), PCI interface, etc. Some chips also include dedicated blocks, like multipliers, DSPs, and microprocessors.

Another fundamental difference between an FPGA and a CPLD refers to the storage of the interconnects. While CPLDs are non-volatile (that is, they make use of antifuse, EEPROM, Flash, etc.), most FPGAs use SRAM, and are therefore volatile. This approach saves space and lowers the cost of the chip because FPGAs present a very large number of programmable interconnections, but requires an external ROM. There are, however, nonvolatile FPGAs (with antifuse), which might be advantageous when reprogramming is not necessary.

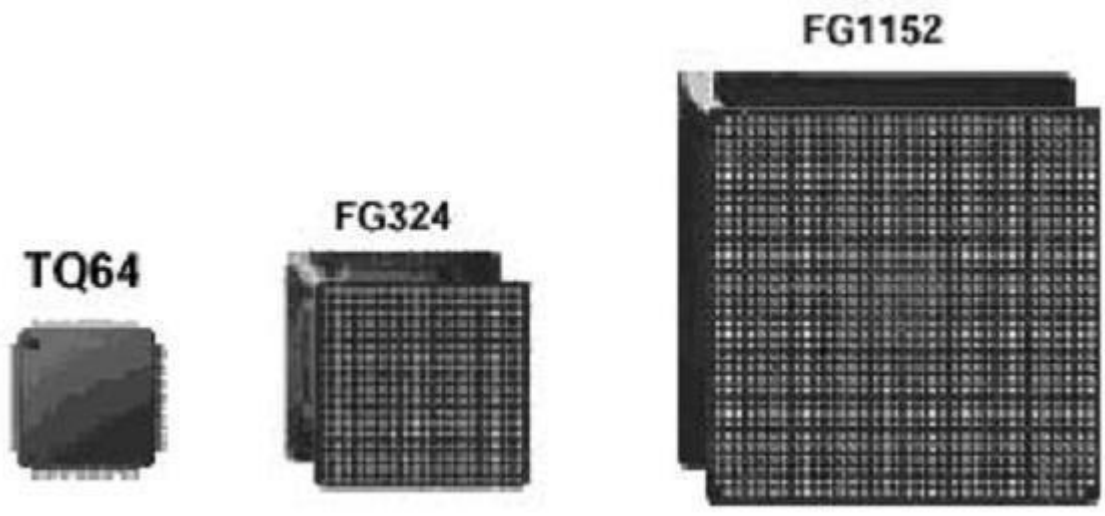


Figure 3 : Examples of FPGA Packages

FPGAs can be very sophisticated. Chips manufactured with stateoftheart0.09mmCMOS technology, with nine copper layers and over 1,000 I/O pins,

are currently available. A few examples of FPGA packages are illustrated in figure A6, which shows one of the smallest FPGA packages on the left (64 pins), a medium-size package in the middle (324 pins), and a large package
(1,152 pins) on the right. Several companies manufacture FPGAs, like Xilinx, Actel, Altera, and Quick Logic. Notice that all Xilinx FPGAs use SRAM to store the interconnects, so are reprogrammable, but volatile (thus requiring external ROM). On the other hand, ActelFPGAs are non-volatile (they use anti fuse), but are nonreprogrammable (except one family, which uses Flash memory). Since each approach has its own advantages and disadvantages, the actual application will dictate which chip architecture is most appropriate.

2.CHAPTER
CMOS Technology

2. Introduction to CMOS Technology

2.1 What is CMOS?

CMOS stands for **Complementary Metal-Oxide-Semiconductor**, a technology used for constructing integrated circuits (ICs) that utilize both p-type and n-type MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). This complementary arrangement allows for efficient logic functions with minimal power consumption, making CMOS the predominant technology in modern electronics.

2.2 Historical Background

The development of CMOS technology began in the 1960s, with significant advancements in the 1970s and 1980s. Its low power consumption and high noise immunity made it ideal for battery-powered devices, leading to widespread adoption in various applications, from calculators to smartphones.

2.3 Fundamental Principles of CMOS

MOSFET Basics

MOSFET stands for **Metal-Oxide-Semiconductor Field-Effect Transistor**. It is a type of transistor used for amplifying or switching electronic signals. The MOSFET is the fundamental building block of modern digital electronics and is used extensively in **integrated circuits (ICs), processors, memory, analog circuits**, and **power electronics**.

MOSFETs are of two major types based on the type of charge carriers:

- **N-type MOSFET (NMOS)**

  An N-type MOSFET (NMOS) is a type of MOSFET in which electrons are

the primary charge carriers. It turns ON when a positive voltage is applied to the gate terminal, relative to the source. NMOS transistors are faster than PMOS due to the higher mobility of electrons and are used extensively in logic circuits, memory elements, amplifiers, and switching applications.

- **P-type MOSFET (PMOS)**

  A P-type Metal-Oxide-Semiconductor Field-Effect Transistor (PMOS) is a type of MOSFET where holes are the majority charge carriers. It conducts when the gate voltage is lower than the source (typically a negative voltage relative to the source). PMOS transistors are the complementary counterpart to NMOS devices and play a vital role in CMOS (Complementary MOS) logic design.

These are further divided into:

- **Enhancement-mode MOSFETs**
- **Depletion-mode MOSFETs**

In CMOS technology, **enhancement-mode NMOS and PMOS** devices are primarily used.

2.4 CMOS Inverter

The CMOS inverter is the simplest and most fundamental CMOS circuit. It consists of a PMOS transistor connected to the power supply (V_DD) and an NMOS transistor connected to ground. The gates of both transistors are connected to the input, and their drains are connected together to form the output. When the input is high, the NMOS conducts, pulling the output low; when the input is low, the PMOS conducts, pulling the output high.

2.5 CMOS in Digital and Analog Design

2.5.1 Digital Design with CMOS

- **Logic Gates:** NAND, NOR, and XOR gates are efficiently implemented using CMOS.
- **Sequential Circuits:** Flip-flops, registers, and counters built with CMOS for storage and timing.
- **Datapath Components:** Adders, multiplexers, ALUs, and other critical elements use CMOS.

2.5.2 Analog Design with CMOS

- **Amplifiers:** CMOS is used to design operational and differential amplifiers.
- **Filters and Oscillators:** Implemented using CMOS transistors for signal processing.
- **Data Converters:** ADCs and DACs designed using CMOS are essential in mixed-signal applications.

2.6 Advantages of CMOS Technology

- **Low Power Consumption:** Power is only consumed during switching, making CMOS ideal for battery-powered devices.
- **High Noise Immunity:** CMOS circuits are less susceptible to noise, ensuring reliable operation.
- **High Density:** The small size of CMOS transistors allows for a high density of logic functions on a single chip.
- **Scalability:** CMOS technology scales well with advancements in lithography, enabling continued miniaturization.

2.7 Applications of CMOS Technology

CMOS technology is ubiquitous in modern electronics, including:

- **Microprocessors and Microcontrollers:** The brains of computers and embedded systems.
- **Memory Devices:** SRAM, DRAM, and flash memory utilize CMOS technology.
- **Analog Circuits:** Operational amplifiers, analog-to-digital converters, and other analog components.
- **Imaging Sensors:** CMOS image sensors are common in digital cameras and smartphones.
- **Communication Devices:** CMOS is used in RF circuits and transceivers.

2.8 Future of CMOS Technology

To address the challenges and continue scaling, several approaches are being explored:

- **FinFETs:** A 3D transistor structure that offers better control over the channel.
- **Gate-All-Around (GAA) FETs:** Transistors where the gate surrounds the channel on all sides, providing superior electrostatic control.
- **New Materials:** Incorporating materials like graphene or transition metal dichalcogenides to improve performance.
- **3D Integration:** Stacking multiple layers of circuits to increase density without reducing feature sizes.

3.CHAPTER
Software Requirement

Tanner tool is a Spice Computer Analysis Programmed for Analogue Integrated Circuits. Tanner tool consists of the following Engine Machines:

1. S-EDIT (Schematic Edit)
2. T-EDIT (Simulation Edit)
3. W-EDIT (Waveforms Edit)
4. L-EDIT (Layout Edit)

Using these engine tools, spice program provides facility to the use to design & simulate new ideas in Analogue Integrated Circuits before going to the time consuming & costly process of chip fabrication.

3.1 **Schematic edit tool (s-edit)**

S-Edit is hierarchy of files, modules & pages. It introduces symbol & schematic modes. S-Edit provides the facility of:

1. Beginning a design.
2. Viewing, drawing & editing of objects.
3. Design connectivity.
4. Properties, net lists & simulation.

Instance & browse schematic & symbol mode.

3.1.1 Beginning a design:

It explains the design process in detail in terms of file module operation and module.

Browser:

Effective schematic design requires a working knowledge of the S-Edit design hierarchy of files & modules. S-Edit design files consist of modules. A module is a functional unit of design such as a transistor, a gate and an amplifier.

Modules contain two components:

1. Primitives: Geometrical objects created with drawing tools.
2. Instances References to other modules in file. The instanced module is the original.

S-Edit has two viewing modes:

1. Schematic Mode: to create or view a schematic, we operate in schematic mode.
2. Symbol Mode: it represents symbol of a larger functional unit such as operational amplifier.

3.2 **T-spice pro circuit analysis**

An introduction to the integrated components of the T- Spice Pro circuit analysis suite:

Schematic data files **(.sdb)**: describes the circuits to be analyzed in graphical form, for display and editing by S- Edit" Schematic Editor.

Simulation input files **(.sp):**describes the circuits to be analyzed in textual form, for editing and simulation by T- Spice" Circuit Simulator.

Simulation output files **(.out):** containing the numerical results of the circuit analyses, form manipulation and display by W- Edit" Waveform Viewer.

3.2.1 Circuit simulator (t-spice):

T-Spice Pro's waveform probing feature integrates S- Edit, T- Spice, and W- Edit to allow individual points in a circuit to be specified and analyzed. A few analysis is described below: The heart of T-Spice operation is the input file (also known as the circuit description, the net list &the input deck). This is a plain text file that contains the device statement & simulation commands, drawn from the SPICE circuit description language with which T-Spice constructs a model of the circuit to be simulated. Input files can be created and modified with any text editor. T-Spice is a
tool used for simulation of the circuit. It provides the facility of

1. Design Simulation
2. Simulation Commands
3. Device Statements
4. User-Designed External Models
5. Small Signal & Noise Models

T- Spice uses Kirchhoff's Current Law (KCL) to solve circuit problems. To TSpice, a circuit is a set of devices attached to nodes. The voltage at all nodes represents the circuit state. T-Spice solves for a set of node voltage that satisfied KCL (implying that sum of currents flowing into each node is zero). In order to evaluate whether a set of node voltages is a solution, T-Spice computers and sums all the current flowing out of each device into nodes connected to it (its terminals). The relationship between the voltages at device terminals and the currents through the terminal is determined by the device model for a resistor of resistance R is $I=\Delta V/R$ Where, ΔV represents the voltage difference across the device. A few analyses are discussed below:

3.2.2 DC Operating Point Analysis:

DC operating point analysis finds a circuit's steady- state condition, obtained (in principle) after the input voltages have been applied for an infinite amount of time. The .include command causes T- Spice to read in the contents of the model file for the evaluation of NMOS and PMOS transistors. The technology file assigns values to MOSFET model parameters for both n - and p -type devices. When read by the input file, these parameters are used to evaluate MOSFET model equations, and the results are used to construct internal tables of current and charge values. Values read or interpolated from these tables are used in the computations called for by the simulation. Following each transistor name are the names of its terminals.

The required order of terminal names is: drain-gate -source -bulk. Then the model name (NMOS or PMOS in this example), and physical characteristics such as length and width, are specified. The .op command performs a DC operating point calculation and writes the results to the file specified in the Simulate > Start Simulation dialog. The output file lists the DC operating point information for the circuit described by the input file.

3.2.3 DC Transfer Analysis:

DC transfer analysis is used to study the voltage or current at one set of points in a circuit as a function of the voltage or current at another set of points. This is done by sweeping the source variables over specified ranges, and recording the output. A list of sources to be swept, and the voltage ranges across which the sweeps are to take place follow the .dc command, indicating transfer analysis. The transfer analysis will be performed as follows: add will be set at 5 volts and vin will be swept over its specified range; vdd will then be incremented and vin will be swept over its range; and so on, until vdd reaches the upper

limit of its range. The .dc command ignores the values assigned to the voltage sources vdd and vin in the voltage source statements, but they must still be declared in those statements. The results for nodes in and out are reported by the. print dc command to the specified destination.

3.2.4 Transient Analysis:

Transient analysis provides information on how circuit elements vary with time. The basic T-Spice command for transient analysis has three modes. In the default mode, the DC operating point is computed, and T- Spice uses this as the starting point for the transient simulation. The command specifies the characteristics of the transient analysis to be performed.

3.2.5 AC Analysis:

AC analysis characterizes the circuit's behaviour dependence on small- signal input frequency. It involves three steps:

(1) Calculating the DC operating point;

(2) Linear zing the circuit; and

(3) Solving the liberalized circuit for each frequency.

When ac voltage source is to be applied, then v diff sets the DC voltage difference between nodes the two nodes to -0. 0007 volts; its AC magnitude is 1 volt and its AC phase is 180 degrees. The .ac command performs an AC analysis. Following the .ac keyword is information concerning the frequencies to be swept during the analysis. In case, the frequency is to be swept logarithmically, by decades (DEC); 5 data points are to be included per decade is considered to be the standard The two .print commands write the voltage magnitude (in decibels) and phase (in degrees), respectively, for the node out to the specified file. The .ac model command writes the small- signal model parameters and operating point voltages and currents for all circuit devices.

3.2.6 Noise Analysis:

Real circuits, of course, are never immune from small, random fluctuations in voltage and current levels. In T- Spice, the influence of noise in a circuit can be simulated and reported in conjunction with AC analysis. The purpose of noise analysis is to compute the effect of the noise associated with various circuit devices on an output voltage or voltages as a function of frequency.

Noise analysis is performed in conjunction with AC analysis; if the .ac command is missing, then the noise command is ignored. With the .ac command present, the .noise command causes noise analysis to be performed at the same frequencies. The .noise command takes two arguments: the output at which the effects of noise are to be computed, and the input at which the .noise can be considered to be concentrated for the purposes of estimating the equivalent noise spectral density. The print command is used to print results.

3.3 **Waveform edit**

The ability to visualize the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding & improving these circuits. W-Edit is a waveform viewer that provides ease of use, power & speed in a flexible environment designed for graphical data representation. The advantages of W-Edit include:

1. W-Edit seamlessly integrates with T-Spice, the circuit-level simulator from Tanner EDA. It can directly chart data generated by T-Spice without requiring any modifications to the output text files. Additionally, W-Edit allows dynamic charting of data as it is produced during the simulation.Charts can automatically configure for the type of data being presented.
2. A data is treated by W-Edit as a unit called a trace. Multiple traces from different output file scan be viewed simultaneously in single or several windows; traces can be copied and moved between charts & windows. Trace arithmetic can be performed on existed tracing to create new ones.

3. Chart views can be panned back & forth and zoomed in & out, including specifying the exact X-Y co-ordinate range.

4. Properties of axes, traces, rides, charts, text & colors can be customized.

Numerical data is input to W-Edit in the form of plain or binary text files. Header & Comment information supplied by T-Spice is used for automatic chart configuration. Runtime update of results is made possible by linking WEdit to a running simulation in T-Spice. W-Edit saves data with chart, trace, axis & environment settings in files with the WDB (W-Edit Database).

3.4 Layout (l-edit):

It is a tool that represents the masks that are used to fabricate an integrated circuit. It describes a layout design in terms of files, cells & mask primitives. On the layout level, the component parameters are totally different from schematic level. So it provides the facility to the user to analyze the response of the circuit before forwarding it to the time consuming & costly process of fabrication. There are rules for designing layout diagram of a schematic circuit using which user can compare the output response with the expected one.

L- Edit: An Integrated Circuit Layout Tool :

In L- Edit, layers are associated with masks used in the fabrication process. Different layers can be conveniently represented by different colours and patterns. L- Edit describes a layout design in terms of files, cells, instances, and mask primitives. You may load as many files as desired into memory. A file may be composed of any number of cells. A file may be composed of any number of cells. These cells may be hierarchically related, as in a typical design, or they may be independent, as in a library file. Cells may contain any number or combination of mask primitive sand instances of other cells.

Cells: The Basic Building Blocks:

The basic building block of the integrated circuit design in L- Edit is a cell. Design layout occurs within cells. A cell can:

1. Contain part or all of the entire design.
2. Be referenced in other cells as a sub- cell, or instance.
3. Be made up entirely of instances of other cells.
4. Contain original drawn objects, or primitives.
5. Be made up entirely of primitives or a combination of primitives and instances of other cells.

3.4.3 Hierarchy:

L- Edit supports fully hierarchical mask design. Cells may contain instances of other cells. An instance is a reference to a cell; should you edit the instanced cell, the change is reflected in all the instances of that cell. Instances simplify the process of updating a design, and also reduce data storage requirements, because an instance does not need to store all the data within the instanced cell instead, only a reference to the instanced cell is stored, along with information on the position of the instance and on how the instance may be rotated and mirrored.

L-Edit does not use a “separated” hierarchy: instances and primitives may coexist in the same cell at any level in the hierarchy. Design files are self- contained. The pointer to a cell contained in an instance always points to a cell within the same design file. When cells are copied from one file to another, L- Edit automatically copies across any cells that are instanced by the copied cell, to maintain the self- contained nature of the destination file.

Design Rules

Manufacturing constraints can be defined in L- Edit as design rules. Layouts can be checked against these design rules.

3.4.4 Design Features:

L- Edit is a full- custom mask editor. Manual layout can be accomplished more quickly because of L Edit's intuitive user interface. In addition, one can construct special structures to utilize a technology without, worrying about problems caused by automatic transformations. Phototransistors, guard bars, vertical and horizontal bipolar transistors, static structures, and Schottky diodes, for example, are as easy to design in CMOS- Bulk technology as are conventional MOS transistors.

Floor plans

L- Edit is a manual floor planning tool. You have the choice of displaying instances in outline, identified only by name, or as fully fleshed- out mask geometry. When you display your design in outline, you can manipulate the arrangement of the cells in your design quickly and easily to achieve the desired floor plan. One can manipulate instances at any level in the hierarchy, with insides hidden or displayed, using the same graphical move/ select operations or rotation/ mirror commands that you use on primitive mask geometry.

Memory Limits

In L- Edit, one can make your design files as large as one like, given available RAM and disk space.

Hard Copy

L- Edit provides the capability to print hard copy of the design. A multi age option allows very large plots to be printed to a specific scale on multiple 8 1/ 2 x 11 inch pages.

An L- Edit macro is available to support large- format, high- resolution, color plotting on inkjet plotters.

Variable Grid L-Edit's grid options support lambda- based design as well as micron- based and mil- based design.

Error Recovery L-Edit's error- trapping mechanism catches system errors and in most cases provides a means to recover without losing or damaging data.

1. L- Edit Modules
2. L- Edit TM: a layout editor
3. L- Edit ¤ Extract TM: a layout extractor
4. L- Edit ¤ DRC TM: a design rule checker

L- Edit is a full- featured, high-performance, interactive, graphical mask layout editor. L-Edit generates layouts quickly and easily, supports fully hierarchical designs, and allows an unlimited number of layers, cells, and levels of hierarchy. It includes all major drawing primitives and supports 90°, 45°, and all- angle drawing modes.

Extract creates SPICE compatible circuit net lists from L- Edit layouts. It can recognize active and passive devices, sub circuits, and the most common device parameters, including resistance, capacitance, device length, width, and area, and device source and drain area. DRC features user

programmable rules and handles minimum width, exact width, minimum space, minimum surround, non- exist, overlap, and extension rules. It can handle full chip and region- only DRC. DRC offers Error Browser and Object Browser functions for quickly and easily cycling through rule- checking errors.

4.CHAPTER
Literature Survey

- P. E. Dodd and L. W. Massengill, “Basic mechanisms and modeling of singleevent upset in digital microelectronics,” - Physical mechanisms responsible for nondestructive single-event effects in digital microelectronics are reviewed, concentrating on silicon MOS devices and integrated circuits. A brief historical overview of single-event effects in space and terrestrial systems is given, and upset mechanisms in dynamic random access memories, static random access memories, and combinational logic are detailed. Techniques for mitigating single-event upset are described, as well as methods for predicting device and circuit single-event response using computer simulations. The impact of technology trends on single-event susceptibility and future areas of concern are explored.

- J. D. Black, P. E. Dodd, and K. M. Warren, “Physics of multiple-node charge collection and impacts on single-event characterization and soft error rate prediction,” - Physical mechanisms of single-event effects that result in multiple-node charge collection or charge sharing are reviewed and summarized. A historical overview of observed circuit responses is given that concentrates mainly on memory circuits. Memory devices with single-node upset mechanisms are shown to exhibit multiple cell upsets, and spatially redundant logic latches are shown to upset when charge is collected on multiple circuit nodes in the latch. Impacts on characterizing these effects in models and ground-based testing are presented. The impact of multiple-node charge collection on soft error rate prediction is also presented and shows that full circuit prediction is not yet well understood. Finally, gaps in research and potential future impacts are identified.

- M. Fazeli, S. N. Ahmadian, S. G. Miremadi, H. Asadi, and M. B. Tahoori, "Soft error rate estimation of digital circuits in the presence of multiple event transients (METs)," - In this paper, we present a very fast and accurate technique to estimate the soft error rate of digital circuits in the presence of Multiple Event Transients (METs). In the proposed technique, called Multiple Event Probability Propagation (MEPP), a four-value logic and probability set are used to accurately propagate the effects of multiple erroneous values (transients) due to METs to the outputs and obtain soft error rate. MEPP considers a unified treatment of all three masking mechanisms i.e., logical, electrical, and timing, while propagating the transient glitches. Experimental results through comparisons with statistical fault injection confirm accuracy (only 2.5% difference) and speed-up (10,000X faster) of MEPP.

- S. Lin, Y.-B. Kim, and F. Lombardi, "Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset,"- The occurrence of a single event with a multiple-node upset is likely to increase significantly in nanoscale CMOS due to reduced device size and power supply voltage scaling. This paper presents a comprehensive treatment (model, analysis, and design) for hardening storage elements (memories and latches) against a soft error resulting in a multiple-node upset at 32-nm feature size in CMOS. A novel 13T memory cell configuration is proposed, analyzed, and simulated to show a better tolerance to the likely multiple-node upset. The proposed hardened memory cell utilizes a Schmitt trigger (ST) design. As evidenced in past technical literature and used in this work, simulation of all node pairs by current sources results in an assessment similar to 3-D device tools; the simulation results show that the proposed 13T improves substantially over DICE in the likely and realistic scenarios of very diffused or limited charge sharing/collection. Moreover, the 13T cell achieves a 33% reduction in write delay and only a 5% (9%) increase in power consumption (layout area) compared to the DICE cell (consisting of 12 transistors). The analysis is also extended to hardened latches; it is shown that the latch with the highest critical charge has also the best tolerance to a multiple-node upset. Among the hardened latches, the ST designs have the best tolerance, and in particular, the transmission gate configuration is shown to be the

most effective. Simulation results are provided using the predictive technology file for 32-nm feature size in CMOS. Monte Carlo simulation confirms the excellent multiple-node upset tolerance of the proposed hardened storage elements in the presence of process, voltage, and temperature variations in their designs.

- E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," - Trends in terrestrial neutron-induced soft-error in SRAMs from a 250 nm to a 22 nm process are reviewed and predicted using the Monte-Carlo simulator CORIMS, which is validated to have less than 20% variations from experimental soft-error data on 180-130 nm SRAMs in a wide variety of neutron fields like field tests at low and high altitudes and accelerator tests in LANSCE, TSL, and CYRIC.
- The following results are obtained:

1) Soft-error rates per device in SRAMs will increase x6-7 from 130 nm to 22 nm process;

2) As SRAM is scaled down to a smaller size, soft-error rate is dominated more significantly by low-energy neutrons (<; 10 MeV); and 3) The area affected by one nuclear reaction spreads over 1 M bits and bit multiplicity of multi-cell upset become as high as 100 bits and more.

- R. C. Baumann, "Soft errors in advanced semiconductor devices-part I: The three radiation sources," - In this review paper, we summarize the key distinguishing characteristics and sources of the three primary radiation mechanisms responsible for inducing soft errors in semiconductor devices and discuss methods useful for reducing the impact of the effects in final packaged parts.
- S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," - We propose a quad-node ten transistor (10 T) soft

error robust SRAM cell that offers differential read operation for robust sensing. The cell exhibits larger noise margin in sub-0.45 V regime and 26% less leakage current than the traditional soft error tolerant 12 T DICE SRAM cell. When compared to a conventional 6 T SRAM cell, the proposed cell offers similar noise margin as the 6 T cell at half the supply voltage, thus significantly saving the leakage power. In addition, the cell exhibits 98% lower soft error rate than the 6 T cell in accelerated neutron radiation tests carried out at TRIUMF on a 32-kb SRAM implemented in 90nm CMOS technology.

- T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," - A novel design technique is proposed for storage elements which are insensitive to radiation-induced single-event upsets. This technique is suitable for implementation in high density ASICs and static RAMs using submicron CMOS technology.
- R. Rajaei, B. Asgari, M. Tabandeh, and M. Fazeli, "Design of robust SRAM cells against single-event multiple effects for nanometer technologies," - As technology size scales down toward lower two-digit nanometer dimensions, sensitivity of CMOS circuits to radiation effects increases. Static random access memory cells (SRAMs) that are mostly employed as high-performance and high-density memory cells are prone to radiation-induced single-event upsets. Therefore, designing reliable SRAM cells has always been a serious challenge. In this paper, we propose two novel SRAM cells, namely, RHD11 and RHD13, that provide more attractive features than their latest proposed counterparts. Simulation results show that our proposed SRAM cells as compared with some state-of-the-art designs have considerably higher robustness against single-event multiple effects. Moreover, they offer a sensible area overhead advantage so that our proposed RHD11 SRAM cell has 19.9% smaller area than the prominent dual-interlocked cell. The simulation results and analyses show that our proposed SRAM cells, particularly the proposed RHD13, have a considerable lower failure probability among the considered recent radiation-hardened SRAM cells.
- J. Guo, L. Xiao, and Z. Mao, "Novel low-power and highly reliable radiation hardened memory cell for 65 nm CMOS technology," - In this paper, a novel low-power and highly

reliable radiation hardened memory cell (RHM-12T) using 12 transistors is proposed to provide enough immunity against single event upset in TSMC 65 nm CMOS technology. The obtained results show that the proposed cell can not only tolerate upset at its any sensitive node regardless of upset polarity and strength, but also recover from multiple-node upset induced by charge sharing on the fixed nodes independent of the stored value. Moreover, the proposed cell has comparable or lower overheads in terms of static power, area and access time compared with previous radiation hardened memory cells.

- J. R. Ahlbin et al., "Effect of multiple-transistor charge collection on singleevent transient pulse widths, - Heavy-ion data from a 130-nm bulk CMOS process shows a counterproductive result in using a common singleevent charge collection mitigation technique. Guard bands, which are well contacts that surround individual transistors, can reduce single-event pulsewidths for normal strikes, but increase them for angled strikes. Calibrated 3-D TCAD mixed-mode modeling has identified a multiple- transistor charge collection mechanism that explains the experimental data, namely that angled strikes result in charge collection in the normally ON device that increases the restoring current on the struck device.

5.CHAPTER
Existing System

SRAM (Static Random Access Memory):

Introduction:

SRAM stands for **Static Random Access Memory**, a type of semiconductor memory widely used in digital systems such as microprocessors, microcontrollers, and cache memories. Unlike DRAM (Dynamic RAM), which needs to be refreshed periodically, **SRAM retains data as long as power is supplied**, hence the term "static."

Features of SRAM

- Faster access time compared to DRAM
- No refresh circuitry required
- Volatile memory – loses data when power is turned off
- Low density – takes more space per bit than DRAM
- Higher cost per bit
- Used primarily in caches, registers, and small memory arrays

SRAM Cell Design

The most common SRAM cell is the **6T SRAM cell**, which uses **6 transistors per bit**:

- **4 transistors (T1–T4)** form a pair of cross-coupled inverters that store the data.
- **2 access transistors (T5 and T6)** control access to the cell during read/write operations via the word line (WL) and bit lines (BL, $B\bar{L}$).

Operation of SRAM

Write Operation:

- The **bit lines (BL and $B\bar{L}$)** are driven with the desired value.
- The **word line (WL)** is asserted high.

- The access transistors connect the inverters to the bit lines, forcing the value into the cell.

Read Operation:

- Bit lines are precharged to Vdd.
- WL is asserted high.
- Depending on the stored value, one bit line will discharge, and the sense amplifier detects the logic level.

To improve human life and productivity, numerous electronic devices are placed in complex radiation environments, such as specific mines, unique medical environments, and primarily, space. These electronic devices heavily rely on microprocessors for operation. Enhancing microprocessor performance by increasing their working frequency or developing multicore processing technology is a priority. However, as the number of microprocessor cores increases, a faster cache becomes necessary. The SRAM-based cache memory constitutes approximately 70% of the processor area, and in some cases, it can be as high as 90%. Therefore, optimizing SRAM by reducing power consumption, minimizing area, and increasing frequency, among other methods, can enhance the microprocessor's performance.

Designing an SRAM that can function in these complex operating environments is a challenging task. An integrated circuit operating in a radiation environment can be hit by charged particles. Essentially, when a charged particle traverses a reversebiased p-n junction, the electric field within the depletion region of the reversebiased junction causes the separation of electron–hole pairs.

Consequently, the charge migrates toward the diffusion region, leading to the accumulation of excess charge. Once a specific quantity of charge is accumulated, it triggers a transient voltage pulse. As shown in Fig. 1, when a particle hits the pMOS of the inverter, a positive transient pulse appears. Similarly, when a particle hits the nMOS of the inverter, a negative transient pulse appears. In a logic circuit, if the threshold voltage is lower than

the voltage pulse, it reverses the data on the sensitive node, resulting in a single-event upset (SEU).

However, this error is short-lived as the next write operation overwrites the incorrect data, thus refreshing the correct data. Such errors, which can be restored to normal, are called soft errors. SEU is a type of soft error.

Although soft errors affect both memory cells and logic circuits, the memory cell's greater packing density makes it more susceptible to soft errors. Among memory cells, SRAM cells have lower node capacitance and a larger sensitive volume per bit, making them more vulnerable to the influence of SEUs. The situation becomes more challenging as the transistor spacing gets smaller with advanced node technologies.

Single event multinode upsets (SEMNUs) are known to occur in advanced technology nodes. These types of upsets arise due to a charge-sharing phenomenon, where a single charged particle can affect multiple nodes. It is worth noting that SEMNUs do not occur in older technology nodes [3]. A single-bit upset occurs when the affected nodes are in the same memory cell. Conversely, a multibit upset can occur when the affected nodes are in different memory cells.

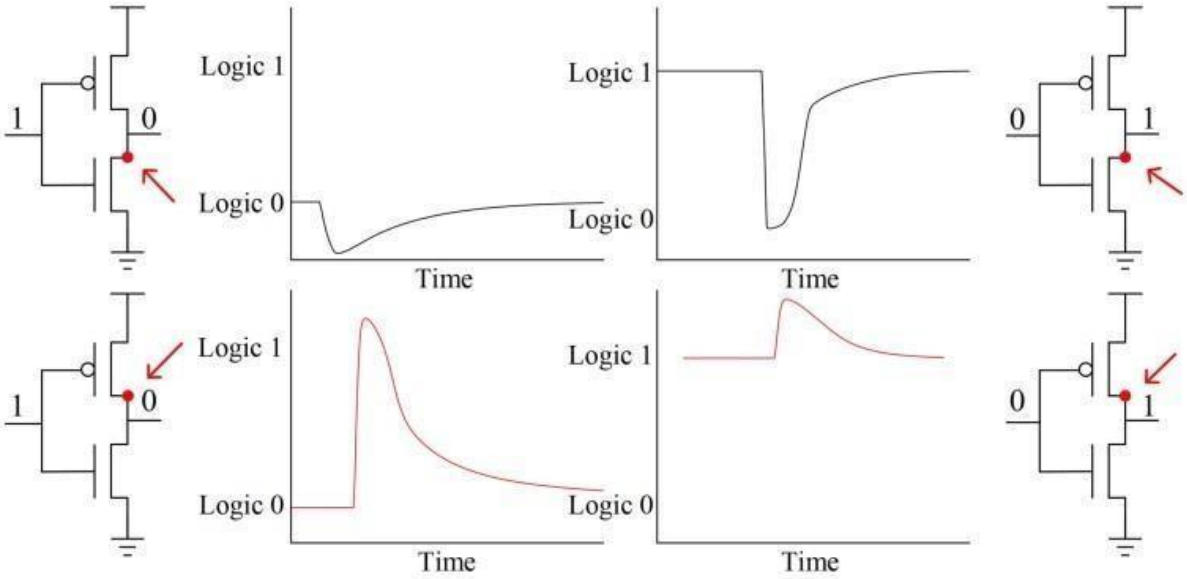


Figure 4 : Pulsed current is generated when the charged particles hit the PMOS.

Mitigating the effects of SEUs typically involves three methods. One such method is the use of error-correcting codes. However, this approach necessitates the use of both coding and decoding circuits, which results in significant losses in terms of area, power, and delay. The second approach involves the use of specialized processes. However, this can lead to increased production costs, complex production procedures, and a loss of device performance. The third approach involves decreasing the impact of soft errors by altering the topology design of the circuit. This reinforcement method is simple and effective, though it often requires an increase in area and power consumption to achieve better device performance.

In this article, the third method mentioned above is used to decrease the influence of SEUs. This article proposes a 16TSRAM (S8P8N), which consists of eight pMOS and eight nMOS transistors. S8P8N is capable of fully recovering from SEUs of both polarities induced at any single sensitive node. Regardless of which single sensitive node induces SEU of both polarities, S8P8N can be fully recovered. S8P8N also addresses the SEMNU problem, as it demonstrates that soft errors are self-recoverable in the internal nodes. In summary, S8P8N has two advantages that are listed in the following.

1) Every single node in the S8P8N can recover to its initial state after being affected by an SEU. S8P8N can even fully recover when a multinode upset occurs

at the internal node pair.

2) Compared to most comparison cells, the write time of S8P8N is significantly shorter. For write power consumption, S8P8N is superior to most compared cells.

5.1 Disadvantages:

- Power Consumption: Smaller transistors tend to have higher leakage currents, leading to increased power consumption, particularly in idle states.

- Complexity: The design and manufacturing processes are more complex, potentially increasing the risk of defects and reducing yields.

- Radiation Susceptibility: The smaller feature size makes the circuitry more susceptible to radiation induced soft errors, necessitating more advanced error correction and hardening techniques.
- Performance: Larger feature sizes can result in slower operating speeds, which may not be suitable for high-performance applications.
- Area Efficiency: The larger size of the transistors means that the same circuitry will occupy more space compared to 45nm technology, leading to less compact designs.
- Density: Lower transistor density can be achieved, which might limit the amount of functionality that can be integrated into a given area.

6.CHAPTER
Proposed System

In this research, we present the design and comparative analysis of soft-error-aware 16T SRAM arrays using 45nm and 65nm CMOS technologies, with a focus on aerospace applications. Aerospace environments are highly susceptible to radiationinduced soft errors, demanding the development of robust memory systems. We begin by designing a single-bit 16T SRAM cell optimized for multinode upset tolerance, incorporating advanced error correction and radiation-hardening techniques to enhance reliability. The single-bit cell design is then scaled to an 8x8 SRAM array architecture. Both the 45nm and 65nm versions of the array are developed and simulated to evaluate key performance metrics, including area, delay,
and power consumption.

The results indicate that while 45nm technology achieves better performance and area efficiency, 65nm technology excels in power savings and reliability. This comprehensive study underscores the importance of technology selection in optimizing SRAM design for high-reliability aerospace applications, offering a framework for future advancements in radiation-hardened memory systems.

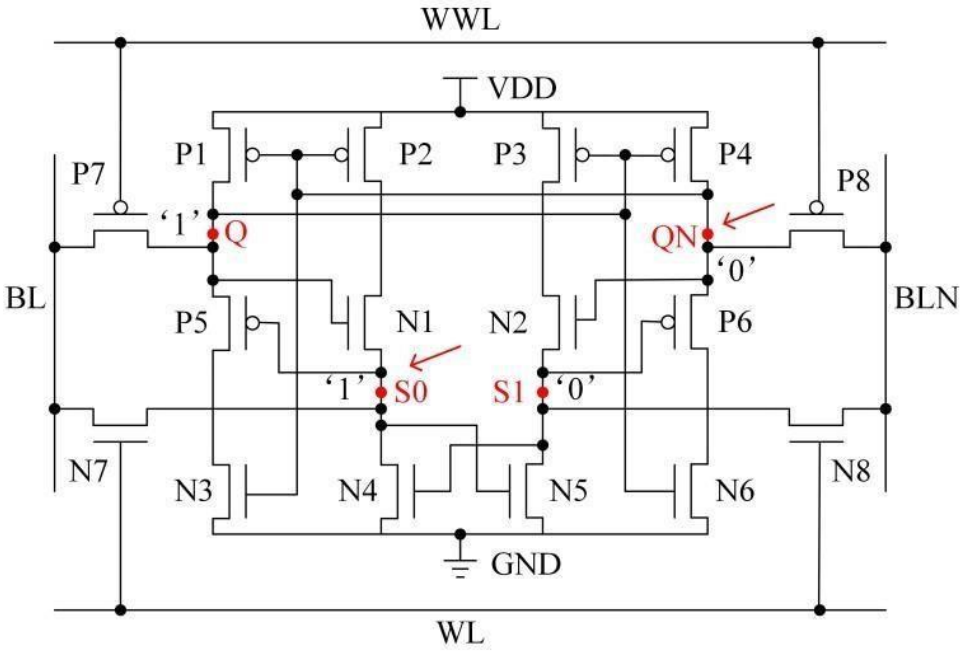


Figure 5 : Circuit diagram of the proposed 16T SRAM architecture

presents the specific design of the S8P8N cell, which includes two storage nodes (Q and QN) and two internal nodes (S0 and S1), and its layout is shown in Fig. 3. The internal node S0 is connected to the bitline (BL) through access transistors N7 when the word line (WL) is enabled. Similarly, the internal node S1 is connected to another bitline (BLN) through access transistors N8 when the WL is enabled. Transistors P7 and P8, controlled by the write word line (WWL), connect storage nodes Q and QN to bit lines BL and BLN, respectively. Assuming the S8P8N cell and all comparison cells stored the same value of "1," it implies that Q and QN store values of "1" and

"0," respectively. Consequently, the internal nodes S0 and S1 have store

values of "1" and "0," respectively.

1) Hold Mode: All access transistors are turned off in this mode, with WL and

WWL disabled and bit lines BL and BLN maintained at VDD to reduce wakeup time [3]. Specifically, transistors P1, P2, P6, N1, N5, and N6 remain on, while the others are switched off. As a result, the original stored data of the S8P8N remain unchanged.

2) Write Operation: The stored data in the cell change when the BL discharges to GND and the BLN charges to VDD. Subsequently, WL is charged to VDD and WWL is discharged to GND, keeping the access transistors on. As BLN is maintained at VDD, transistor P8 charges node QN, and transistor N8 charges node S1. As BL is maintained at GND, transistor P7 discharges node Q, and transistor N7 discharges node S0. By steadily increasing the gate voltages of P1, P2, P6, N3, and N4, the corresponding transistors can easily pull down nodes Q and S0. As the voltage of node S0 falls below the nMOS threshold voltage, transistor N5 turns off, causing node S1 to charge faster, completing the write operation.

3) Read Operation: At the start of a read operation, both bit lines BL and BLN and the WL must be precharged to VDD. The WWL can remain in a high state to deactivate the access transistors P7 and P8 in an upset-free read operation state. During this state, N5 and N8 can discharge the BLN when in the "ON" state. BL is first discharged through N4 and N7. As S1 discharges to a voltage lower than the nMOS threshold, N4 turns off and BL stops discharging. VDD is charged to BL through P2, N1, and N7. During the read operation, the sense amplifier detects the stored data based on the voltage difference between the

   BL and BLN. It is noteworthy that storage nodes Q and QN are not involved during the read operation.

6.1 Advantages:

- Performance: The smaller feature size allows for higher operating speeds, resulting in better overall performance.
- Area Efficiency: The reduced size of the transistors leads to a smaller footprint for the same circuitry, allowing for more compact designs.
- Density: Higher transistor density can be achieved, enabling more functionality in a given area.

- Power Consumption: Larger feature sizes generally have lower leakage currents, which can result in significant power savings, especially in standby modes.
- Reliability: The 65nm nodes are generally more robust against certain types of radiation effects, offering higher reliability in radiation-prone environments.
- Manufacturing Maturity: The 65nm process is more mature and wellunderstood, often leading to better yields and potentially lower costs.

7.CHAPTER
Result

We explored diverse modifications to the proposed soft-error-aware 16T SRAM architecture using 45nm and 65nm CMOS technologies, running many trials to examine critical performance metrics like area, speed, and power consumption. As a primary step, a lone-bit 16T SRAM cell enhanced for multi-node upset endurance was established. Its actions in authentic memory assemblies were consequently studied by broadening it into an 8x8 SRAM array infrastructure.

Tanner EDA tools were applied to conduct simulations, warranting the precision of the schematics and layouts. To assess the circuit's perseverance to radiation-induced defects, transient, DC, and noise investigations were performed. Additionally, the disparity in responses between single cells and complete arrays was notable, with certain failure modes more overt at larger scales. The primary cell concept translated well when expanded, demonstrating potential for utilization in dependable recollections required for extreme conditions.

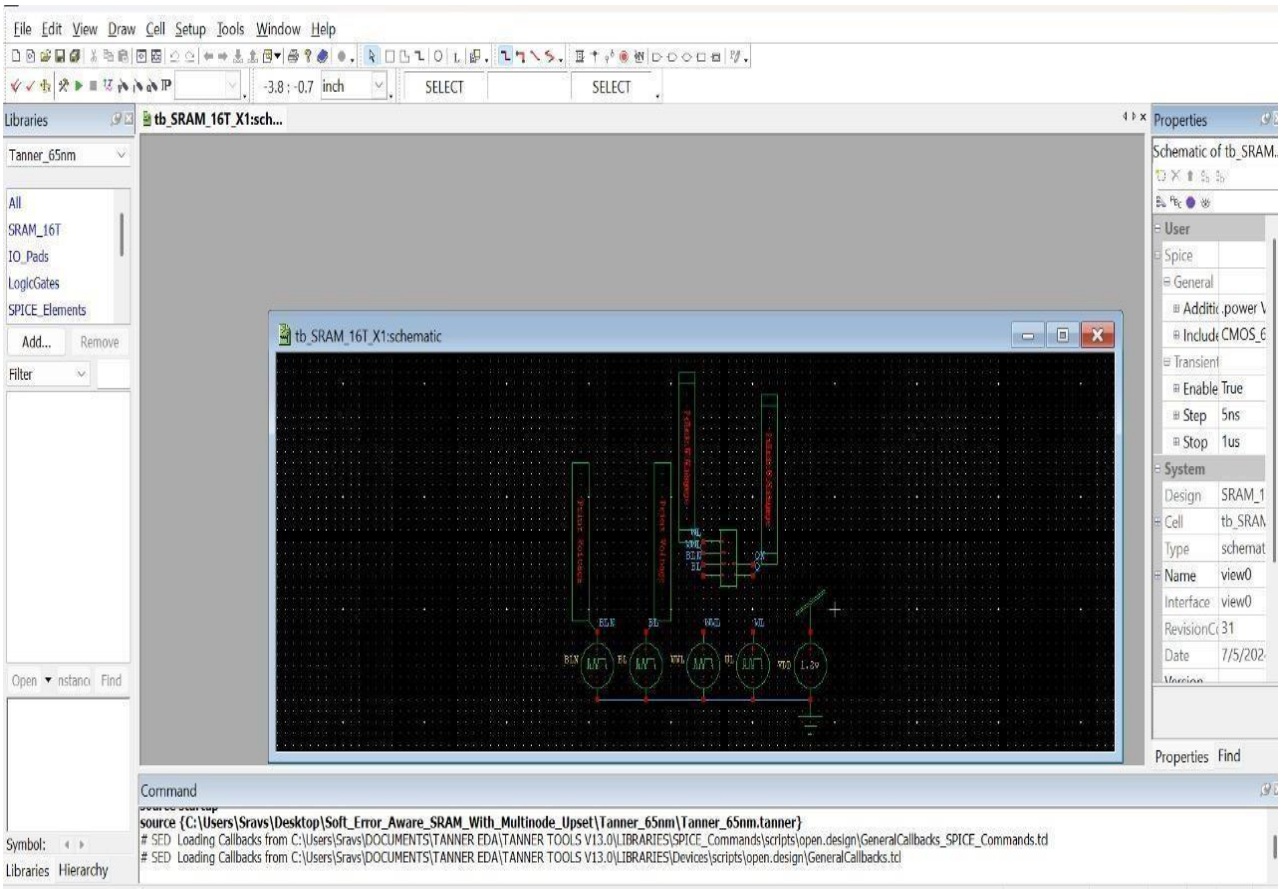
While the 45nm SRAM layout permitted enhanced throughput and area optimization owing to diminished feature measurements lowering latency and escalating velocity, the 65nm design architecture proved better fitted for prolonged space missions necessitating frugality since of its cut power usage and elevated dependability. Not unlike anticipated, when compared to the later 65nm application, preliminary statistical review uncovered the 45nm mechanism exhibited a slightly higher leakage of power but a shorter access duration.

The 65nm execution alternative is preferentially picked for environments anticipating sizeable radiation presentation since it supplies stronger to lerance to gentle mistakes despite requiring more room. This contrastive assessment underscores the criticality of judiciously opting for the proper process technology reliant on the necessities

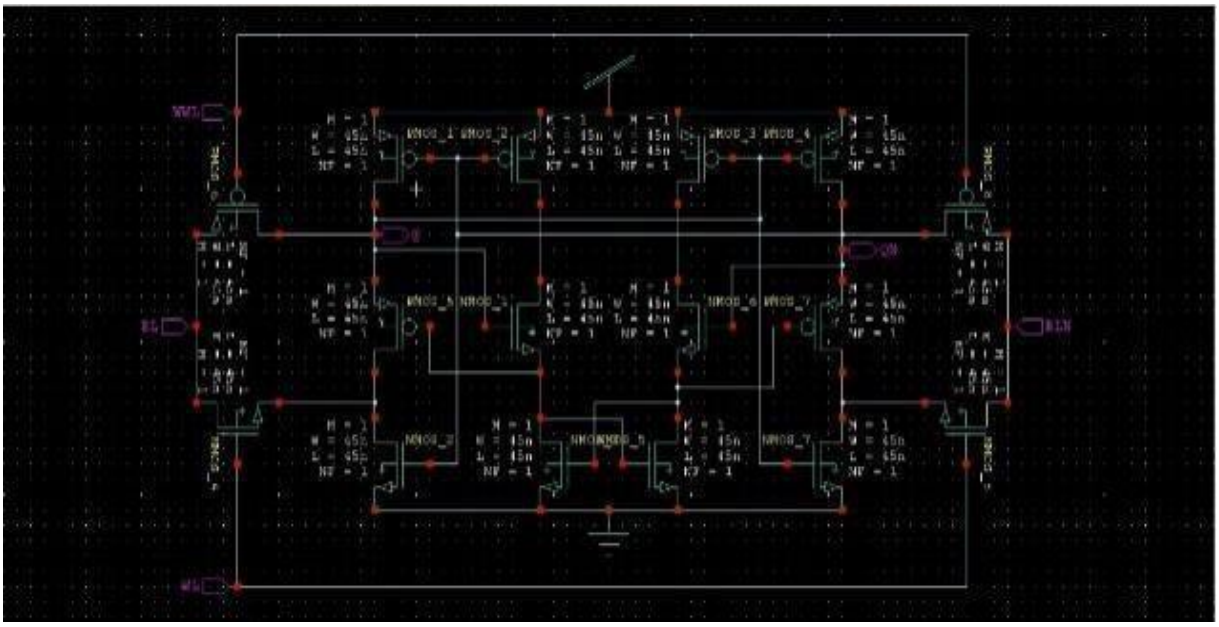
of aerospace memory frameworks. A variety of trade-offs exist between emerging strategies, highlighted by this examination.

Using 65nm:

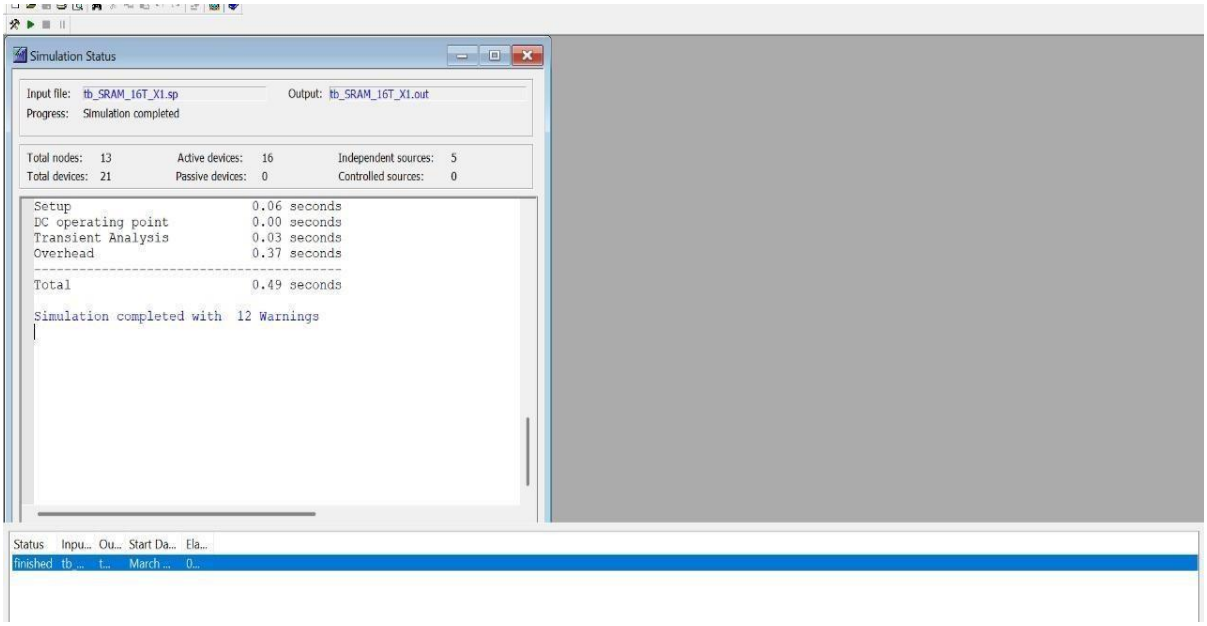
SRAM 16T_X1_SCHEMATIC:



SRAM ARCHITECTURE:

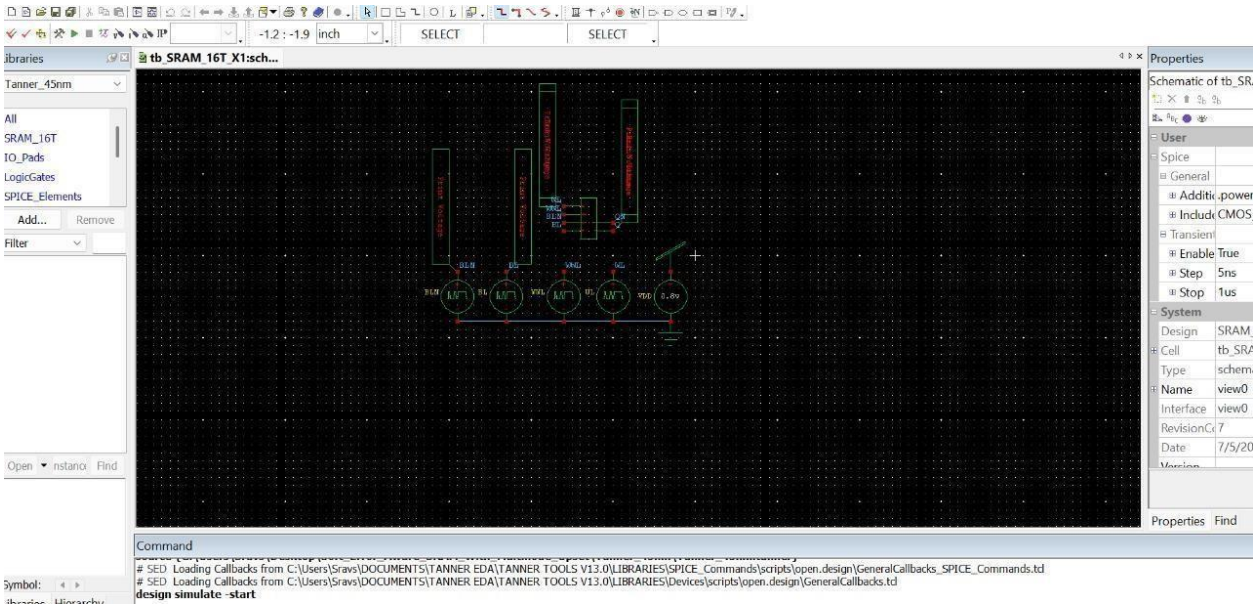


Simulation Status:

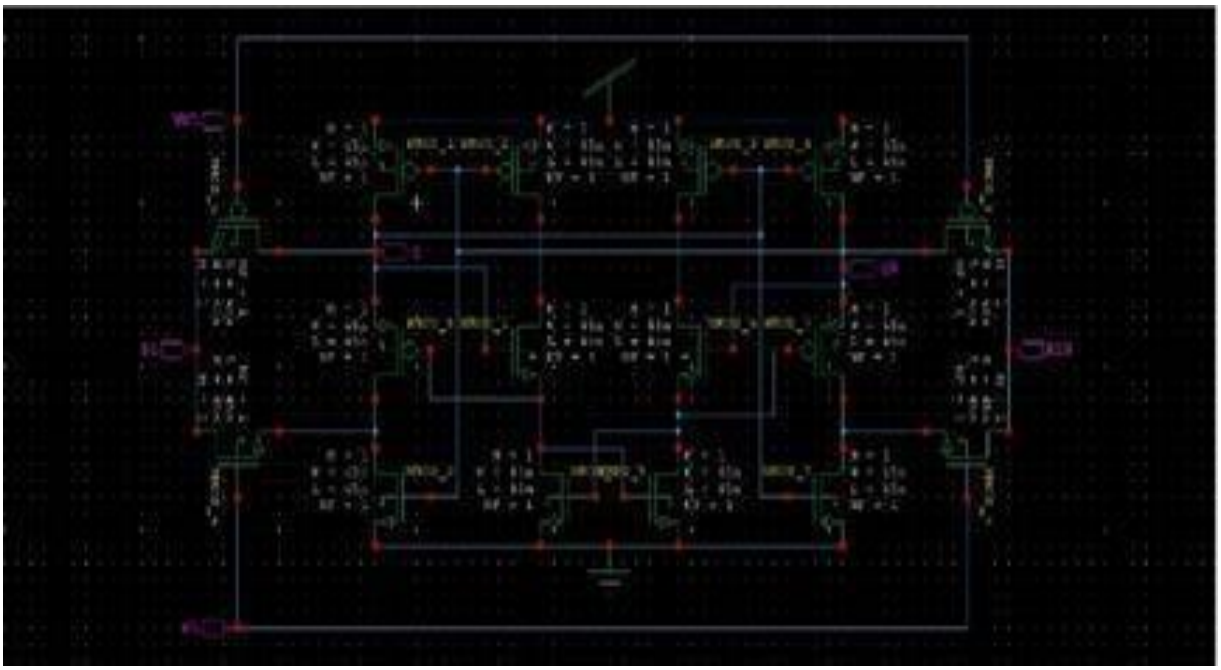


Using 45nm:

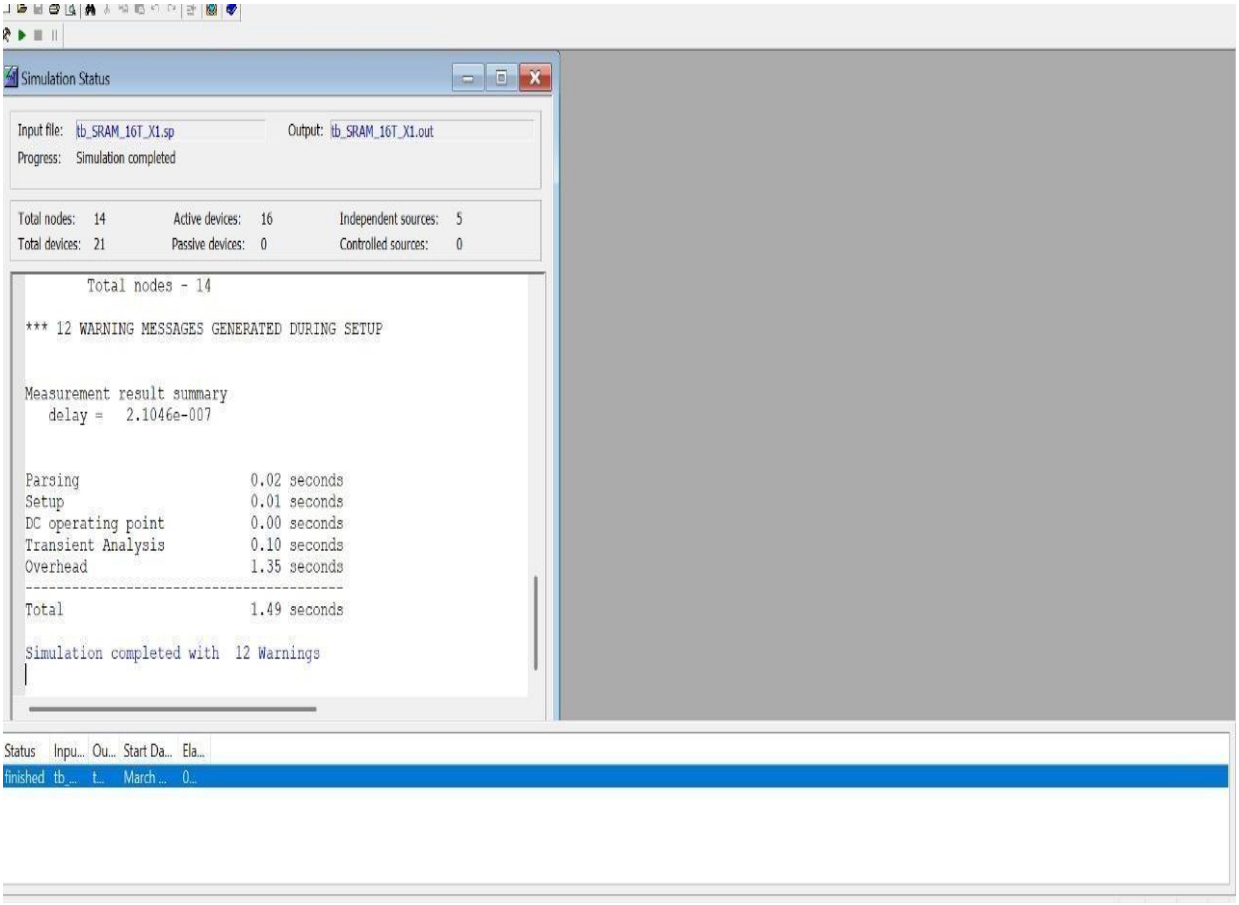
SRAM 16T_X1_SCHEMATIC:



SRAM ARCHITECTURE:

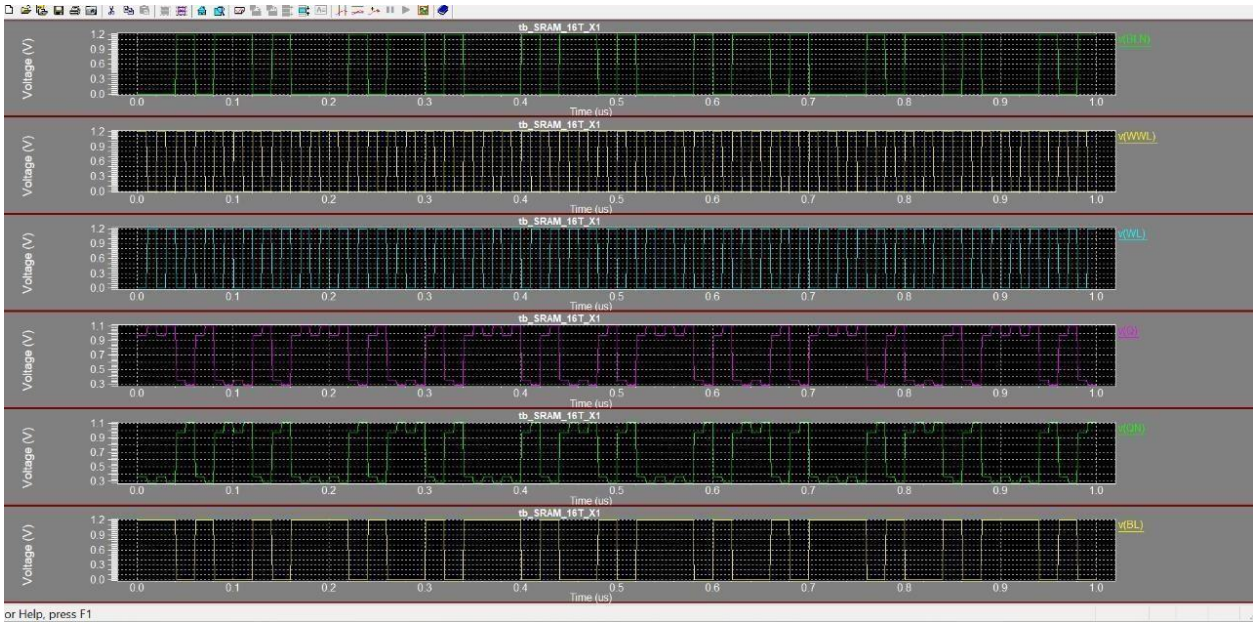


Simulation Status:

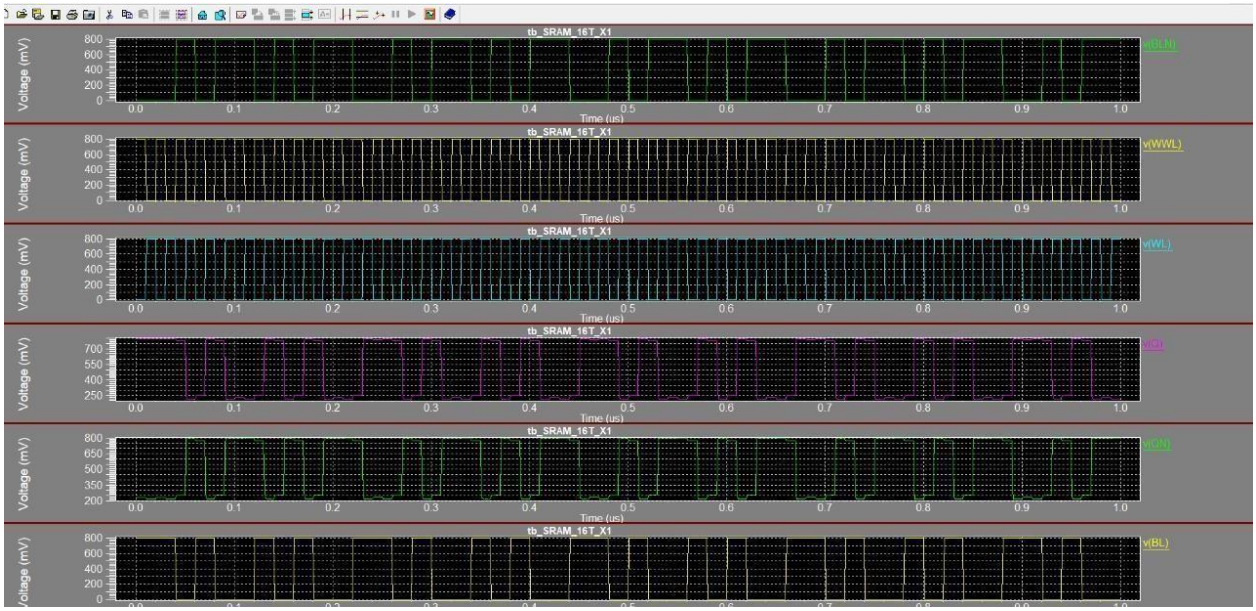


Wave forms:

Using 65nm:



Using 45nm:



8.CHAPTER
Performance Evaluation

The realized trade-offs between area efficiency, power and delay for two different CMOS technologies (i.e., 45nm and 65nm) using the soft-error-aware 16T SRAM arrays are greatly useful. The 45nm version achieves better area efficiency in that a single-bit cell is 0.720 μm^2 whereas the same cell for the 65nm is 1.040 μm^2 Similarly, the example 8×8 SRAM 45nm stack takes up 46.080 μm^2 of chip area, roughly 30.8% smaller than the same device in 65nm. As a result, logic components can take up less area, allowing for a greater density of transistors, and thus leading to smaller designs, an absolute necessity in resource-constrained situations like aerospace systems. Performance wise, the delay of single-bit SRAM cell in 45nm technology is 0.210 µs, which is substantially lower than the 0.329 µs delay exhibited by the 65nm implementation. However, as evidenced in the 8×8 array plot, both technologies exhibit almost identical delays, so it appears that such interconnect and architecture-level properties may have a larger impact on timing performance than technology at larger scales.

Power consumption goes some way in showing the disparity between the two technologies as well. At 45nm, the single-bit SRAM cell requires a mere 0.767 µW, in contrast, at 65nm the cell drew 138.68 µW, which means the 45nm design is approximately 180 times as power-efficient. The same trend can be seen in the 8×8 SRAM array, with the 45nm shifting at 49.097 µW, while the 65nm uses a considerably higher 8875.74 µW. This notable difference Also, the 55% improvement in power efficiency shows that 45nm technology better suits power constrained applications. 61Nevertheless, 65nm technology is often preferred for aerospace applications although it consumes more power than 90nm process technology since it exhibits much better resistance to soft errors due to radiation and has improved reliability. This comparative study emphasizes that the right technology node has to be chosen according to the needs of the design, weighing trade-offs in area, powergate (timing) efficiency, performance, and soft error resiliency in potential radiationprone environments.

Comparisons:

Parameters	45nm		65nm	
	Single Bit	8x8 Array	Single Bit	8x8 Array
Input Voltage(V)	0.8	0.8	1.2	1.2
MOSFETs	16	1024	16	1024
Area (um)	0.720	46.080	1.040	66.560
Power (uW)	0.767	49.097	138.68	8875.74
Delay (us)	0.210	0.390	0.329	0.389

Figure2 :Performance Graph displaying accuracy level.

The graphical rendering of the suggested 16T SRAM design exposes important considerations between 45nm and 65nm CMOS with regard to energy usage, space usage, access timing, and durability. The 45nm execution has quicker transit and minimized requirements owing to its scaled down traits and thus fits requests needing fleet manipulation and compact storage formats.

Nonetheless, this goes with expanded power utilization and fragility to radiation initiated delicate blunders, which risk hindering the long haul trustworthiness of the framework in aeronautics surroundings. Additionally, the 45nm design consumes more power due to

increased transistor switching activity and parasitic capacitance at the smaller scale. In contrast, the 65nm implementation uses less energy while maintaining reasonable access speeds, making it preferable for applications with long operational lifetimes where reliability is paramount. Overall, the optimal choice depends on priorities among speed, power, area and radiation hardness for a given memory design.

On the other hand, the 65nm design is smaller and slower than the 45nm counterpart, but consumes less power and is more resistant to radiation, which makes it suitable for space based applications where energy efficiency and fault tolerance are important.

These performance metrics show that the decision between these two technologies depends on application specific requirements:

1.45nm for high speed and integration or 65nm for reliability and power efficiency.

2.This analysis further supports the need to consider performance, power and reliability in the design of SRAM for aerospace systems, and thus informs the ongoing pursuit of fault tolerant memory architectures.

9.CHAPTER
CONCLUSION

This work introduces a novel 16T soft error-tolerant SRAM design suitable for aerospace systems operating in radiation-rich environments. Utilizing 45nm and 65nm CMOS processes, the proposed cell architecture enhances reliability through sophisticated error mitigation mechanisms tuned to address multi-node upsets caused by high-energy particle strikes. To demonstrate the efficacy of the approach, we compare the baseline memory's susceptibility to radiation-induced failures with that of the hardened implementation. Through a synthesis of advanced error correction, device-level hardening, and cell-topology adaptations, the proposed 16T cell meaningfully fortifies the memory against soft errors emanating from the harsh radiation conditions of orbital and interplanetary space. The evaluated prototypes validate this SRAM construction as a promising means of bolstering the fault resilience so vital for spaceborne applications vulnerable to transient upsets.

While the 45nm technology certainly provides greater swiftness with its compact construction, enabling aptness for time-sensitive tasks requiring limited real estate, the 65nm approach stands out with its parsimonious energy consumption and fortified resilience. The latter renders it remarkably suited to protracted exploratory missions wherein fault-tolerance and efficacious use of reserves are unsurpassable imperatives. This congruence among competence and dependability underscored the criticality of selecting a technique befitting particular necessities. Going ahead, investigations aiming to augment the robustness and potency of radiation-hardened memory frameworks must contemplate additional improvements like adaptive faultamendment tactics and nascent manufacturing technologies. The harmony between performance and reliability can significantly impact the success of ongoing and future space missions.

10.CHAPTER
FUTURE SCOPE

Integration with Emerging Technologies: Research into cutting-edge transistor technologies such as FinFET and FD-SOI could greatly augment functionality while also bolstering resilience against radiation.

Scalability to Larg er Memory Arrays: By expanding the proposed architecture to accommodate more substantial SRAM arrays while retaining immunity to soft errors, additional applications in reliable aerospace and computing platforms may become feasible.

Advanced Error Correction Mechanisms: To further strengthen protection against transient faults within SRAM structures, forthcoming analyses could leverage adaptive and AI-driven error amendment techniques

Low-Power Design Improvements: By optimizing vitality intake using dynamic voltage scaling and strategies to reduce leakage, energy efficiency for prolonged space missions may be extended considerably

11. CHAPTER

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