# Lab 2

## Files Provided:

RightShifter.bsv, TestShifterPipe.bsv, RightShifterTypes.bsv, and Gates.bsv.

## Introduction

This lab is to implement a sequential circuit version of your shifter and a pipelined version of your shifter.

**Part 1:**  Design and implement a pipelined version of Lab 1.

You do not need to use your combinational circuit design (you can use the >> shift feature within Bluespec if you like.) Try to maximize the performance of the shifter. The maximum throughput will be one full shift (from 0 to 31 bit shift) per cycle.

Question 1.1: A pipelined version cannot use the same interface as the combinational circuit. Explain why not. We’ve provided a new interface for you in RightShifterTypes.bsv.

In addition, a test file (TestShifterPipe.bsv) has been provided that uses the new interface. Be sure to write and/or port tests as needed.

Question 1.2: In the test file, the methods start and result of the shifter are being called from two different rules. Explain why there had to be two rules instead of one. (Hint: try to call both methods from the same rule).

To test your solution’s performance, implement a cycle counter in the mkTests module.

Question 1.3: What is the throughput of your shifter (throughput is the number of full shifts per cycle)? Depending on the conditions, you may get different results. For each throughput level, explain under what conditions you are able to achieve that throughput and what you needed to do in order to get that throughput.

## Submitting Your Solution

Provide all of the files that you changed, along with the answers to the Discussion Question in the same format as Lab 1 (but, of course, using Lab2 as the prefix to the directory.)