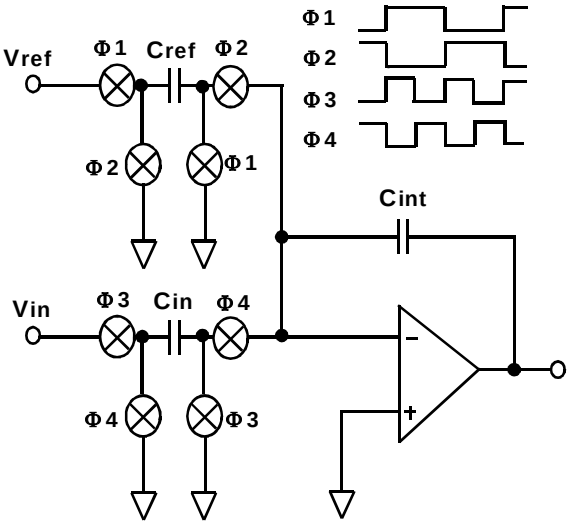
How is the programmable gain function implemented?

Programmable gain is implemented using a combination of multiple input sampling per modulator cycle and scaling of the ratio of reference capacitor to input capacitor. Programmable gain is implemented using switched capacitor techniques. This is achieved by altering the sample rate of the input capacitor in the analog modulator. This technique is shown in figure 3.



Programmable Gain Implementation.

In this circuit, the reference capacitor C*ref* is used to sample the reference voltage V*ref* using non-overlapping clocks ϕ1 and ϕ2 at the modulator sampling frequency f*mod*. The input capacitor C*in* samples the analog input voltage again using non-overlapping clocks ϕ3 and ϕ4 with a sampling frequency of f*in*. If f*mod* is equal to f*in*, the implemented gain is equal to the ratio of C*in* to C*ref*. With the timing shown in figure 3, f*in* = 2f*mod*, thereby implementing a gain of 2 when C*in* = C*ref*.

The datasheet mentions that the analog input of the ADC (all analog inputs of the AD7705/AD7706 and channels AIN1 and AIN2 of the AD7707) can accept bipolar inputs of +/-30mV centered around 0V when the buffer is not used. Can a 3/5V single supply part really do this?

Yes!! A basic outline of an analog input channel is shown in Figure 11 of the AD7705/AD7706 datasheet and Figure 12 of the AD7707 datasheet. Not shown in the figure are ESD protection diodes which are connected from each analog input to the power supply rails (VDD and GND). The input stage is truly differential so, in theory, it can tolerate negative input voltages. However, leakage through the ESD protection diodes limits the ability to handle negative voltages. The diodes are Schottky type and will turn on when approximately 300mV is across them. This turn on voltage is temperature dependant. The effect of leakage through these diodes is to increase the noise at the input and hence reduce the overall resolution.

Analog Devices guarantee full datasheet performance for analog inputs of ±30mV over the full industrial temperature range and, after performing some additional testing, guarantee performance for analog inputs of ±200mV at 25degC.

When the ADC is operated with the inputs shorted, different output codes are obtained depending on whether the part in operated in buffered or unbuffered mode. Is this normal?

If an internal offset and gain calibration is performed when the buffer is selected or de-selected, the same code should be obtained from the ADC in both buffered and unbuffered mode within the noise limit of the part. If a calibration is not performed, it is quite possible to see a different output code in buffered and unbuffered mode for the same input voltage. The buffer is similar to an opamp, therefore it will have an offset voltage. When the user switches between buffered and unbuffered mode, a calibration is essential to remove this offset.

It's important to remember that a calibration must be performed whenever the filter word, input range or the mode of the buffer is changed. The datasheet includes noise tables which list the expected noise and code spread for the various operating conditions.

I'm measuring the input leakage current in unbuffered mode. It is significantly higher than the 1nA typ. quoted in the datasheet. Why is this?

Static leakage current is specified in the datasheet. The leakage current is typically 1 nA in buffered mode or in unbuffered mode when the ADC is in idle mode. The dynamic leakage current (the leakage current when the ADC is converting) is not specified.

If you put the ADC into unbuffered mode and measure the input current, you will observe a combination of leakage current and the dynamic current charging and discharging the sampling capacitor. If the dynamic charging current is likely to be a problem in your application, for example, if you have a high source impedance, you can use the on-chip buffer to isolate the input from these dynamic charging currents. However, this will result in reduced input common mode voltage. The buffer input common mode range is 1.5V below VDD and 50mV above AGND compared to a common mode range of 30mV above VDD and 30mV below AGND for unbuffered mode.

The datasheet mentions that large external capacitors between the input and ground can affect measurement accuracy in unbuffered mode. Can you explain why this is the case? Does it only affect AC input signals or are DC input signals affected too?

If you use the ADC in unbuffered mode, large RC constants on the input can interact with the internal sampling capacitor, and effectively starve the sampling capacitor of charging current. This will cause gain errors in the ADC. The solution is either to use buffered mode or ensure that you respect the maximum RC values given in Table XIV on page 16 of the AD7705/06 datasheet and page 20 of the AD7707 datasheet.

The reference inputs are also unbuffered so, as with using the analog inputs in unbuffered mode, the RC loading on the reference inputs must be sufficiently low to avoid introducing errors into the conversion process.

How does switching between channels on the AD7705/06/07 effect throughput?

The output data rate, which is listed in the datasheet, is the rate at which valid conversions are available when continuous conversions are being performed on a single channel. When the user switches to another channel, additional time is required for the sigma delta modulator and digital filter to settle. The settling time associated with these converters is the time it takes the output data to reflect the input voltage following a channel change. To accurately reflect the analog input following a channel change, the digital filter must be flushed of all data pertaining to the previous analog input. The digital filter on these converters is a sinc^3 filter. Therefore, it takes three times the programmed update rate (conversion time) to clear the filter. Therefore, if the output data rate is 50 Hz, for example, the time required to generate a valid conversion after switching channels is (1/(3*50 Hz)).

When a channel change occurs, the digital filter and modulator are automatically reset, DRDY goes high and will remain high until a valid conversion is available from the 'new' analog input channel. Therefore, following a channel change, DRDY will remain high until the digital filter has calculated a valid conversion i.e. it will remain high for 3 conversion cycles.

When a step change occurs (on the analog input channel being converted), the ADC is not reset. The ADC continues to output conversions and DRDY continues to pulse when a conversion is valid. However, the conversions will not be valid as the digital filter will require 3 conversion periods to generate a digital word relevant to the altered analog input. If the step change occurs at the beginning of a conversion cycle, the ADC will output a valid word 3 conversion cycles later. However, if the step change occurs asynchronously so that it occurs in the middle of a conversion, the ADC needs to complete the present conversion and then perform 3 more conversions to generate an output valid to the 'new' analog input. Therefore, it may take 4 conversion cycles from the instant at which the step change occurs to the instant at which a valid conversion is available.

In summary, the channel switching speed is one third the data output rate. Therefore, in switching applications such as data acquisition systems, it is important to realise that the rate at which conversions are available is three times less than the conversion rate achieved when continuously sampling a single channel.

Is there any suggested protection schemes against ESD that should be considered with these products?

These converters are manufactured on a standard CMOS process and, therefore, all standard practices and protection schemes apply to these devices as with all other CMOS devices. There are ESD protection diodes on all the inputs which protect the device from possible ESD hits due to handling and production. These ESD protection diodes will act to clamp the voltage at any pin to within 0.5V of the supplies. They can carry quite high currents but only for a short period of time so, they can protect the IC from large pulses of short duration (the total energy is still quite low). The Latchup current is typically 100mA on all pins.

The maximum DC current which these protection diodes can withstand is 10mA. Therefore, the maximum current which can be applied to any input is 10 mA. If it is possible for a current in excess of 10 mA to be applied to a pin due to an overvoltage, external protection is required. Protection schemes that can be applied include transzorbs on the power supply lines, series resistors on digital input lines, and resistors and diodes on analog inputs. For example, the external protection could be a resistor in series with the input pin to limit the current into the pin to less than 10 mA. For example, if the maximum overvoltage applied to a pin will be 5V, a 1kOhm series resistor in each line will limit the current to 5 mA.

There are a number of application notes and seminar material etc available on this topic. These are available on the Analog Devices web site:

AN-202 : IC Amplifier User's Guide to Decoupling, Grounding and Making Things go Right for a Change.
http://www.analog.com/UploadedFiles/Application_Notes/135208865AN-202.pdf

2) AN-311 : How to reliably protect CMOS circuits against power supply overvoltage.
http://www.analog.com/UploadedFiles/Application_Notes/52614692AN311.pdf

3) AN-397 : Electrically Induced Damage to Standard Linear Integrated Circuits.
http://www.analog.com/library/applicationNotes/designTech/AN-397.pdf

4) Overvoltage Affects on Analog ICs
http://www.analog.com/UploadedFiles/Associated_Docs/334653243Section7.pdf

What about susceptibility to conducted and radiated electromagnetic emmissions?

Any sigma delta ADC will be susceptible to conducted RF into either the inputs, the power supply pins or into the reference. The reason is that spurious RF signals and their harmonics can be averaged by the sigma-delta modulator and show up as a DC offset or an increase in the noise floor. Radiated RF is a little more difficult to discuss but, similar problems can occur and, there are situations where it is necessary to shield the sigma-delta ADC in a system from large RF fields generated locally within the system.

The amount of protection required will depend on the strength of the local field. There are no hard and fast rules when designing for EMC compatibility as every system will be different but, there are general guidelines which can be followed. Consider the inputs, reference and power supply pins separately, and ensure that each of these lines are properly filtered up to the required maximum frequency. Decoupling capacitors on the power supply, mounted locally to the IC, possibly a small inductor between the analog and digital supplies, filtering on the Reference and the inputs is also critical. A solid low impedance ground plane, and separation of the analog and digital grounds - all the usual good practices with the ground plane running under the whole of the IC. The evaluation board provides a good starting point.

Occasionally it is necessary to provide a Faraday shield for an ADC if the part is operating in the presence of high EM fields such as next to a power supply or relay or RF transmitter but, this is an exceptional case.

As a component manufacturer, Analog Devices do not perform EMC testing as a general rule since EMC is a system level specification rather than a component specification. It is the responsibility of the PCB designer to ensure that sensitive parts of the circuitry are protected from spurious signals. We don't have guaranteed bullet proof EMC design that we can give to customers but if you use the evaluation board and follow standard practices for layout, grounding and decoupling, it is possible to design a system which meets the CE mark and beyond without expending too much design

effort. The final chapter in all our seminar books is dedicated to hardware design techniques and deals with such issues as grounding, decoupling, parasitic thermocouples and good PCB design.

http://www.analog.com/UploadedFiles/Associated_Docs/116618369Fsect10.PDF

Explain the converter noise with respect to the noise tables in the data sheets and the sources of this noise?

The noise tables in the data sheet show the output rms noise for the selectable notch and output data rate for the part. The numbers given are for the bipolar input ranges with a specified reference and VDD supply used. These noise numbers are typical and are generated at an analog input voltage of 0V based on 1000 conversion results at the specified update rate. The rms noise numbers are also converted to effective resolution in bits. These numbers can be represented as effective resolution in bits rms or bits peak-to-peak. Effective resolution in bits rms is defined as the magnitude of the output rms noise with respect to the input fullscale (2*Vref/Gain). *It is important to note that the peak-to-peak numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise.* Peak to peak noise is 6.6* Rms noise. Bits (peak-to-peak) = Effective Bits (rms)-2.5.

The numbers given are for bipolar input ranges. For the unipolar ranges, the rms noise numbers will be the same as the bipolar range but the peak to peak resolution is now based on half the signal range which effectively means loosing 1 bit of resolution.

The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

For example, consider the AD7705 operating with a 50 Hz update rate, a 5 V power supply and a 2.5V reference. With a gain of 128, the rms noise equals 0.6 uV as given in the datasheet.

When operated in bipolar mode, the fullscale analog input is 5V/128=39mV. The peak to peak noise is 6.6 * 0.6uV = 3.96 uV peak to peak. Therefore, the ratio of Fullscale input to peak to peak noise is 39 mV / 3.96 uV = 9848 which is the resolution in counts. Converting this to bits peak to peak, log (9848) / log 2 = 13.5 bits peak to peak rounded to the nearest 0.5 bit.

What is the peak to peak resolution if the ADC is interfaced to a Transducer which generates an analog output of 0 to 15 mV?

If the AD7705 is operated with a 5 V power supply, a 2.5 V reference and an output data rate of 50 Hz, the rms noise is 0.6 uV when the gain equals 128 ((fullscale range=0 to 20mV in unipolar mode). Since the transducer has an analog output range of 0 to 15 mV, the peak to peak resolution in the application is 15 mV / 6.6 * 0.6 uV = 3788 counts which equates to 12 bits peak to peak. Therefore there will be no code flicker at the ADC's digital output to the 12-bit level.

Are there benefits to post filtering the data from a converter?

Improvements in noise performance can be obtained using post filtering. The on-chip modulator of these converters provides samples at 19.2 kHz to the digital filter when $f_{CLK\ IN}$ is 2.4576 MHz. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed output rate of the filter. Since the output data rate is higher than the Nyquist criterion (which states that the output data rate must be at least twice the bandwidth), the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications that require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate will require some post-filtering following the digital filter.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the converter at the 100 Hz rate giving a -3dB bandwidth of 26.2 Hz. Post-filtering can then be applied to reduce the bandwidth and output noise to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post-filtering can also be used to reduce the output noise from the device for bandwidths below 13.1 Hz. At a gain of 128 and a bandwidth of 13.1 Hz, the output rms noise is 0.6 uV when using the AD7705 converter. This is essentially

device noise or white noise that has primarily a flat frequency response. By reducing the bandwidth below 13.1 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a reduction of approximately √2 in the output rms noise. This additional filtering will reduce the system throughput.

What output coding is used in unipolar and bipolar mode?

The output coding is straight binary in unipolar mode and offset binary in bipolar mode.

Unipolar mode (Binary Coding): With an analog input voltage of 0V, the output code is 0000Hex.

With an.analog input voltage of Vref/Gain, the output code is FFFFHex.

The output code for any analog input voltage can be represented as follows:

Code = (AIN * GAIN *2^n)/Vref

Where AIN is the analog input voltage and n = 16..

Bipolar mode (offset Binary Coding): With an analog input voltage of (-Vref/gain), the output code is 0000 Hex

With an analog input voltage of 0V, the output code is 8000Hex.

With an analog input voltage of (+Vref/gain), the output code is FFFFHex.

Note that the analog inputs are pseudo bipolar inputs and the absolute analog input voltage must remain within the common mode input range at all times.

The output code for any analog input voltage can be represented as follows:

Code = 2^{n-1}*[(AIN * GAIN/Vref)+1]

Where AIN is the analog input voltage and n =16.

What is the difference between fully- differential and pseudo-differential operation?

The analog inputs to the AD7705 are fully differential inputs. With fully differential inputs, the independent input channels are AIN1(+)/AIN(-) and AIN2(+)/AIN2(-). The input signal is represented by the difference between the two input terminals representing the input channel. The common mode voltage can sit anywhere within the range of the ADC and the converter will convert the signal seen between the two inputs. For example, if the AD7705 is converting the signal from a bridge transducer excited with 5V, the common mode voltage will typically be 2.5V with the displacement voltage usually a few mV sitting on this. The device will only convert the differential voltage and the common mode voltage is rejected. Channel AIN1(+)/AIN(-) and AIN2(+)/AIN2(-) can have a different common mode voltage and the AD7705 converts only the difference between the two input nodes.

The AD7706 has three pseudo-differential inputs: With this configuration, the three input channels AIN1, AIN2 and AIN3 are referred to the common input AINCOM. All channels operate in a differential fashion but, since they are all referenced to a single common point, they all must operate with the same common mode voltage.

The AD7707 has two low-level analog inputs AIN1 and AIN2 which are pseudo-differential inputs. With this configuration, AIN1 and AIN2 are referred to the common input LOCOM. Both channels operate in a differential fashion but, since they are all referenced to a single common point, they all must operate with the same common mode voltage.

The high level input AIN3 on the AD7707, which can accept i V is referenced to HICOM.

The user must ensure that the analog input voltage is within the nge for the ADC.

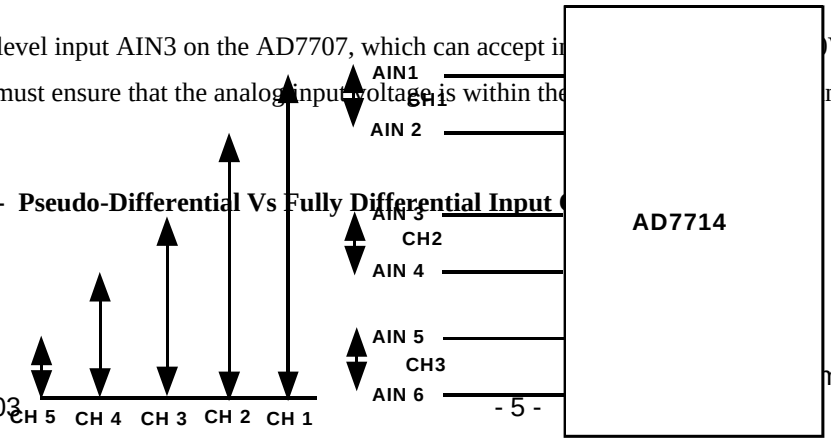


Figure 1 - Pseudo-Differential Vs Fully Differential Input C

What is the recommended common mode input range for the analog and reference inputs?

The common mode range for the reference input is from GND to VDD. The reference input is unbuffered and, therefore, the common mode input range includes the supplies. The recommended reference is 2.5V when the device is operated with a 5V supply and 1.225 V for 3V operation. *These ADCs will not operate with REFIN(+) at 5V and REFIN(-) at GND.*

For the analog inputs, the common mode range is GND – 30 mV to VDD + 30 mV in unbuffered mode. In buffered mode, there is a restriction on the maximum and minimum input voltage due to limitations on the input buffer. This restricts the absolute and common mode input voltage to GND + 50 mV to VDD - 1.5 V.

The common mode range for the AD7707's high level analog input is –10V to +10V when a 5V power supply is used and Vref equals 2.5V or –5V to +5V when a 3V power supply is used and Vref equals 1.225V.

How is the input range for the Low Level Analog Inputs set?

The input range is dependent on the reference voltage, unipolar /bipolar mode selection and the gain setting chosen.

In unipolar mode, the input range is given as [Vref(+) - Vref (-)] / GAIN.

In bipolar mode, the input range is given as ± [Vref(+) - Vref (-)] / GAIN.

With the AD7706 (AD7707), input AINCOM (LOCOM) is a common analog input and the voltages on inputs AIN1 to AIN3 (AIN1 and AIN2) are referenced to the voltage on AINCOM (LOCOM). Again, the common mode voltage can be varied provided the full-scale and zero-scale voltages for each channel remain within the absolute input voltages (between

Can an analog input range other than those specified in the datasheet be used?

Yes – the analog input range can be altered. There are two methods to do this:

A system calibration can be performed during which the user applies the user-specifed zeroscale and fullscale voltages to the ADC during the calibration process. The user must ensure that the fullscale value used is within 0.8VREF/gain and 1.05VREF/gain for specified operation. The ADC will then continue to meet the noise values listed in the datasheet for the original voltage range. For example, the AD7705 has an rms noise spec of 4.1 uV when operated with a 5V power supply, a 50 Hz update rate and a gain of 1 which results in a signal range of 0 to 2.5 V in unipolar mode. If the new fullscale value is within 0.8 * 2.5V and 1.05 * 2.5V, the rms noise will continue to be 4.1 uV.

2) The reference voltage can be altered. For example, if an analog input range of 0 to 1.5V is required, using a reference voltage of 1.5V will result in an analog input of 0 giving an output code of 0000Hex and an analog input of 1.5 V giving a code of FFFFHex. Following a self-calibration with the 1.5 V reference supplying the ADC, the rms noise will be the same as that for a 2.5 V reference which is given in the datasheet. Using the example above, the AD7705 has an rms noise of 4.1 uV when operated with a 50 Hz update rate, 5 V power supply and a 2.5 V reference. If the reference voltage is changed to 1.5 V and a self-calibration is performed, the rms noise will continue to be 4.1 uV assuming the update rate, power supply, etc remain unchanged. The peak to peak resolution equals 16 bits when operated with a 2.5V reference. With a 1.5 V reference, the peak to peak resolution equals log (1.5V / 6.6 * 4.1uV) / log 2 = 15.7. The reduction in peak to peak resolution is due to the reduced input signal span.

When I look at the output of the ADC, I don't get the full resolution; a few of the LSBs are flickering. Why is this happening?

While the ADC has a resolution of 16 bits, the accuracy of the part varies with update rate and gain. The datasheet lists the rms noise and achievable accuracy for different update rates and gains. For example, the AD7705 has a peak to peak resolution of 16 bits when the gain is 1 (analog input range of ±VREF), an update rate of 50Hz and operated in bipolar mode. If the update rate is changed to 250 Hz, the peak-to-peak resolution is reduced to 13 bits. If the gain is now changed to 128 (±20 mV input range), the peak-to-peak resolution is reduced to 12 bits.

The accuracy of an ADC is specified as effective resolution or peak-to-peak resolution. The effective resolution is calculated using the rms noise that is given in the datasheet. The effective resolution equals log (input span / rms noise) / Log 2. The peak-to-peak resolution is the number of bits which do not flicker and is calculated using the peak-to-peak noise which equals 6.6 * rms noise. Therefore, the peak-to-peak noise equals log (input span / (6.6 * rms noise)) / Log 2.

The datasheet rms noise values are measured with the chosen analog input channel shorted to some voltage such as VREF(both terminals of the analog input channel are connected to VREF). Therefore, the user should short the analog input on their system board using a similar method to ensure that the best performance is being obtained from the part. After performing a calibration, commence conversions. Using several thousand samples, the rms noise can be calculated and, from these,.the peak-to-peak resolution can be determined. The obtained value should be compared with the values given in the datasheet. If the accuracy specified in the datasheet is not obtained, this is due to noise on the circuit board, for example, ensure that ground loops do not exist and ensure that the power supply is adequately decoupled using a 10uF tantalum capacitor in parallel with a 0.1uF ceramic capacitor from each power supply to its respective ground. The capacitors should be placed as close as possible to the ADC's pins.

With a constant DC input, the output of the ADC drifts with temperature. Why?

The performance of any ADC varies with temperature. When a calibration is performed at a temperature, the offset error and gain error are minimized at the temperature at which the calibration is performed. However, the offset error and gain error vary with temperature. For example, if you short the analog inputs to some voltage such as the references voltage and perform a calibration, the peak to peak resolution given in the datasheet for the specific update rate and gain should be met. If the temperature varies, the ADC output will vary as the offset error and gain error have drifted with temperature. These drifts are specified in the datasheet.

There will also be drift in the remainder of the signal chain. For example, the reference voltage will vary with temperature also. This variation is specified in the voltage reference datasheet. Resistance values also will vary with temperature. Therefore, it is important to use an accurate reference that has low drift along with resistors with tight tolerances.

Solder joints on a circuit board will also have thermal qualities. Each solder joint connects two dissimilar metals that generate a small thermocouple. Therefore, signal paths for analog signals such as the analog inputs should be kept identical. This will ensure that affects outside the ADC on the analog input lines due to temperature variation are matched and will be removed as a common mode affect.

The integral non linearity is expressed as % of Full-scale. For what gain setting is this valid?

The INL spec refers to the ADC only (not the PGA) so this assumes a gain of 1.

What crystals do ADI recommend using with the sigma-delta ADCs and which parameters are important?

A low drift, high accuracy crystal should be used with these ADCs. With any sigma-delta ADC, the output data rate and –3 dB point are directly related to the master clock frequency. The initial accuracy determines the output data rate and, hence, the notch locations as the filter notches occur at integer multiples of the output data rate. Low drift ensures that the output data rate and, hence, the filter notch locations do not move considerably from the desired locations. A company such as CMAC manufacture low drift crystals with high initial accuracy. .

Can I use a ceramic resonator to drive a sigma delta ADC?

Resonators can be used but they.are a poor relation to crystals. The frequency accuracy and temperature drift is much worse on resonators. Also, all the filter notches scale in proportion to the master clock frequency. Therefore, if a notch is placed at 50Hz and the master clock frequency moves with temperature, the notch frequency will also move with temperature. However, some customers are using ADI's sigma delta converters with ceramic resonators and can live with the poor drift performance.

What is the link between random conversion noise, peak-peak and RMS noise given in the datasheet?

Assume that the noise is truly random and is described by a normal distribution (white noise). Then:

Vnoise (peak-to-peak) = Vnoise (rms) x 6.6; for 99.9% of the time.

Refer to the Technical Note 'Peak to Peak Resolution vs. Effective Resolution at

http://www.analog.com/UploadedFiles/Technical_Notes/236133016AN-615_0.pdf

for more detailed information.

Do I need an anti-alias filter for my sigma-delta converter?

Yes, an anti-alias filter is required. However, because a sigma-delta converter oversamples the analog input, the design of the anti-alias filter is greatly simplified compared to an ADC that samples at the Nyquist rate (Maximum signal Bandwidth * 2).

For example, the AD7705's modulator samples the analog input at a frequency of Master Clock / 64 for a gain of 1 which equals 38.4kHz for a Master Clock Frequency of 2.4576MHz (see table XV in the AD7705 datasheet).

These ADCs have a programmable low pass digital filter. Figure 12 in the AD7705/6 datasheet shows the frequency response for an output data rate of 60 Hz. As this is a digital filter, the frequency response is reflected around the sampling frequency. This means that the filter will provide 0dB of attenuation at frequencies which are integer multiples of the sampling frequency. Therefore, an anti-alias filter in the analog domain is required to adequately attenuate these frequencies; usually a single pole (possibly a 2 pole) RC filter is all that is required. For example, if the 3dB bandwidth of the AD7714 is set to 10Hz and the sampling frequency is at 10kHz, a single pole RC filter would give 60dB of attenuation at the sampling frequency.

When the sigma-delta converter is operated in unbuffered mode, the inputs look directly into the sampling capacitor of the modulator. The modulator is continually charging and discharging the sampling capacitor. If the time constant of the anti-aliasing filter is too large, the modulator may be unable to fully charge the sampling capacitor and gain errors will result. To prevent the R-C combination from introducing errors, the datasheet for each ADC specifies the maximum allowable R and C values that can be used for the different gain settings in unbuffered mode.

Which reference should be used with the ADC?

A low noise reference source is required to achieve the best performance from the ADC. When using the ADC with a 5V power supply, suitable references include the AD780, ADR421, ADR381, ADR291, REF43 and the REF192. When operating the ADC in 3V mode, the AD589 or AD1580 are suitable. It is recommended to decouple the output of these references to further reduce the noise level.

In applications such as pressure measurement systems or weighscales, the excitation voltage for the bridge can be used to derive the reference voltage for the ADC also. The excitation voltage can be divided using a resistor network to generate a 2.5V or 1.225V reference. In these applications, the affect of the noise in the excitation voltage will be removed as the application is ratiometric.