NeuroNoC: An Open Reconfigurable Neural Network Prototyping Platform

Data Packet

TYPE_WIDTH	SEQ_WIDTH	SOURCE_WIDTH	SOURCE_WIDTH	PAYLOAD_WIDTH
Type	Sequence Number	Index	Source	Input

Input Number & Bias

TYPE_WIDTH	SEQ_WIDTH	DEST_WIDTH	SOURCE_WIDTH	PAYLOAD_WIDTH
Type	Sequence Number	Destination	Input Number	Bias

Weight

TYPE_WIDTH	SEQ_WIDTH	DEST_WIDTH	SOURCE_WIDTH	PAYLOAD_WIDTH
Type	Sequence Number	Destination	Source(weight)	Weight

Forwarding Table

TYPE_WIDTH	NETWORK_SIZE	NETWORK_SIZE	3 bits	16 bits
Type	SwitchNumber	EntryNumber	Optional	Data

Fig. 1. PKTFORMAT

***Abstract*—**

***Index Terms*—**

I. Introduction

II. Background and Related Works

III. Architecture

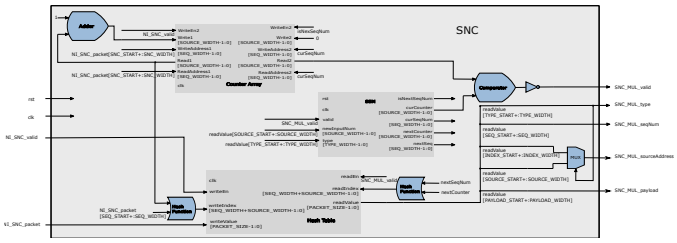

Fig. 2. SNC Architecture

IV. Results and Discussion

V. Conclusion and Future Works

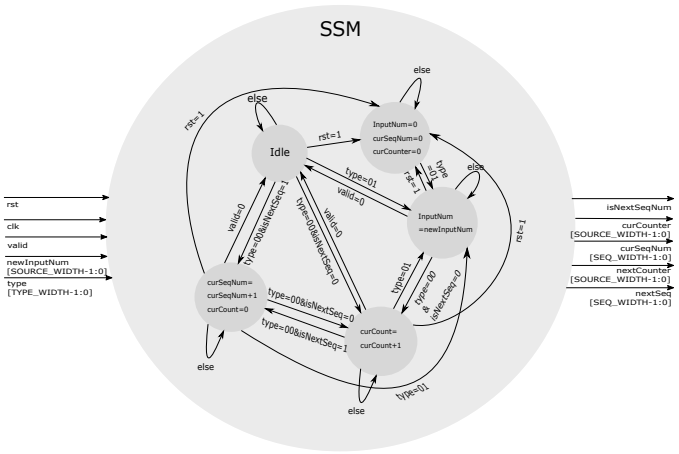

Fig. 3. SST

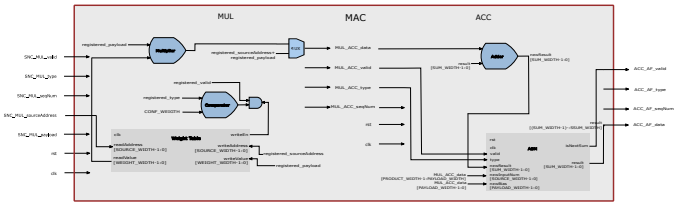

Fig. 4. MAC Architecture

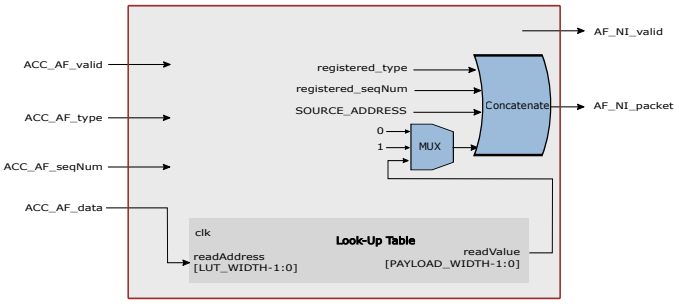

Fig. 5. AF Architecture

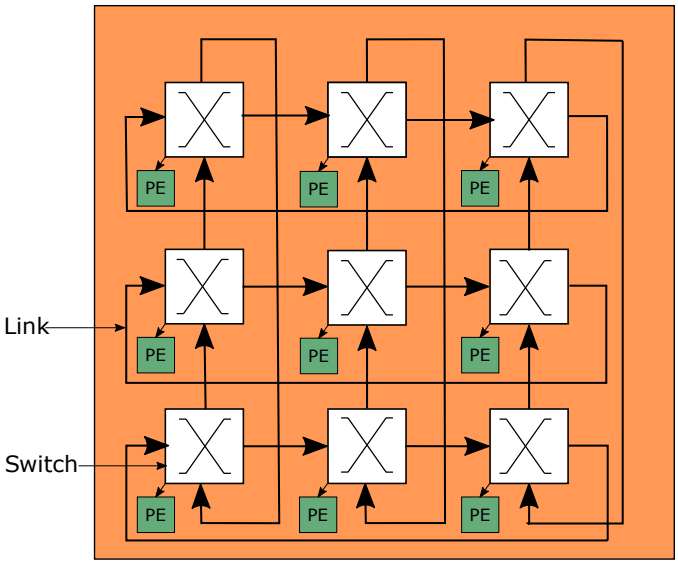

Fig. 6. MESH

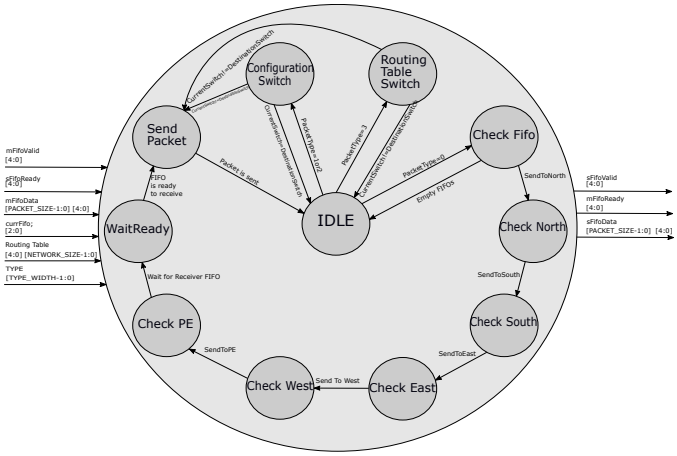

Fig. 8. FSM

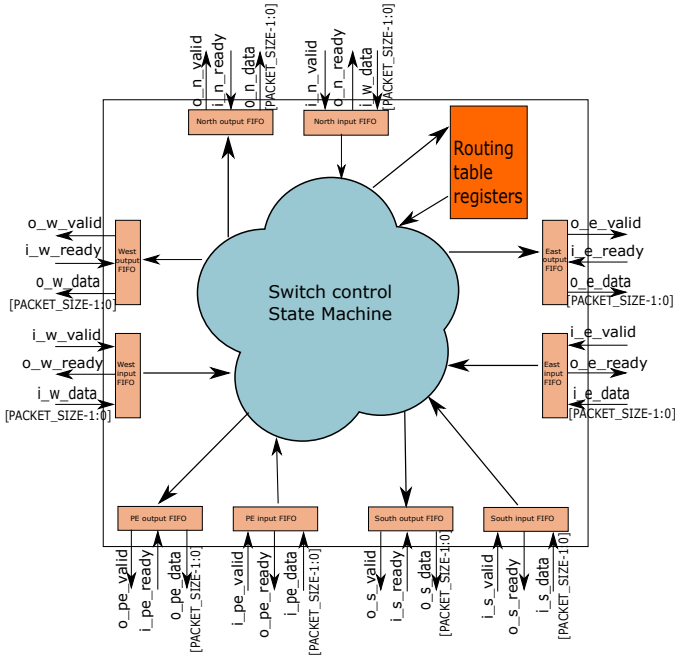

Fig. 7. Switch Architecture