

## Computer Architecture - Lab Assignment 2

# Performance evaluation of the memory hierarchy of a computer and reverse engineering of the data cache memory

The main objective of this lab assignment consists in handling different elements of the architecture of the *Basic Computer* that it is configured in the DE0-Nano board [1]. Some of these elements are responsible for implementing various levels of what we call *the Memory Hierarchy*. These levels of the memory hierarchy and their implementations on the DE0-Nano board are the following:

- The level called *the Main Memory* can be implemented with DE0-Nano using two different electronic technologies:
  - Using electronic circuits of type *SDRAM* that are located outside of the main FPGA chip of DE0-Nano board where the processor Nios II is integrated (see Figure 1) [3].
  - Using electronic circuits of type *SRAM*. In DE0-Nano exists one SRAM electronic device that is also used in this lab assignment to implement the main memory (see Figure 1). The on-chip SRAM memory is an external memory to the Nios II processor but that is integrated into the same FPGA chip.
- The level called *the cache memory*:
  - This level is implemented with electronics circuits of type SRAM that are in the same FPGA chip where is located the Nios II processor (see Figure 1).

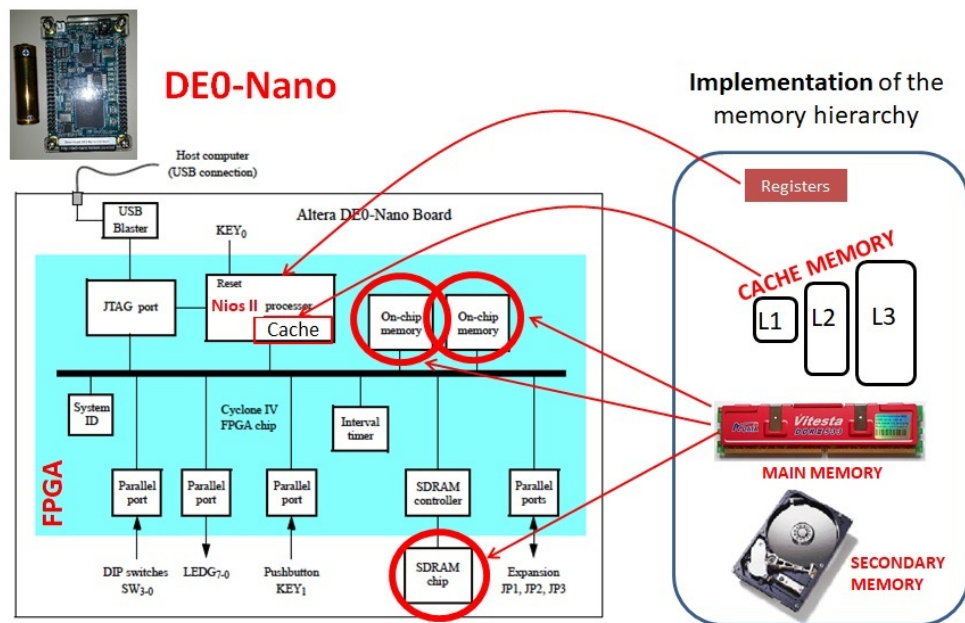


Figure 1: Implementation of the levels of the memory hierarchy of the architecture of the Basic Computer of the DE0-Nano board.

Additionally, two hardware versions of the Nios II processor will be used in this lab assignment, They are called **Nios II/e** (economy) and **Nios II/f** (fast), respectively [2, 4]. Each type of processor and memory cause the execution times of programs to be different.

In this lab experiment, you will measure the execution time of a same program called *Fibonacci* using different configurations of the architecture of the Basic Computer that are implemented in the same DE0-Nano Board. These configurations are distinguished by the type of processor configured: Nios II/e or Nios II/f, as well as in the type of the implementation activated for the levels of the memory hierarchy: cache and main memory (on-chip SRAM or external SDRAM).

The engineering methodology employed in this lab consists of four activities that involve the DE0-Nano board and the software tool called *Altera Monitor Program (AMP)*. There will be some questions that request you to justify the results that you will experimentally obtain.

## Part I. Access to the memory SDRAM with the Nios II/e economy soft processor

The objective of this first lab exercise consists in measuring the execution time of the Fibonacci program using the external SDRAM memory of the DE0-Nano board, in addition to the Nios II/e soft processor, and the Timer input/output controller. Memory controller for the SDRAM memory, processor and Timer are integrated into the FPGA circuit of the board (see Figure 1).

At the end of the execution of the Fibonacci program, the Nios II/e processor measures the number of 33-ms. intervals that have passed. When the Fibonacci program finishes, the terminal of the AMP tool shows the number of time intervals as you can see in Figure 2.

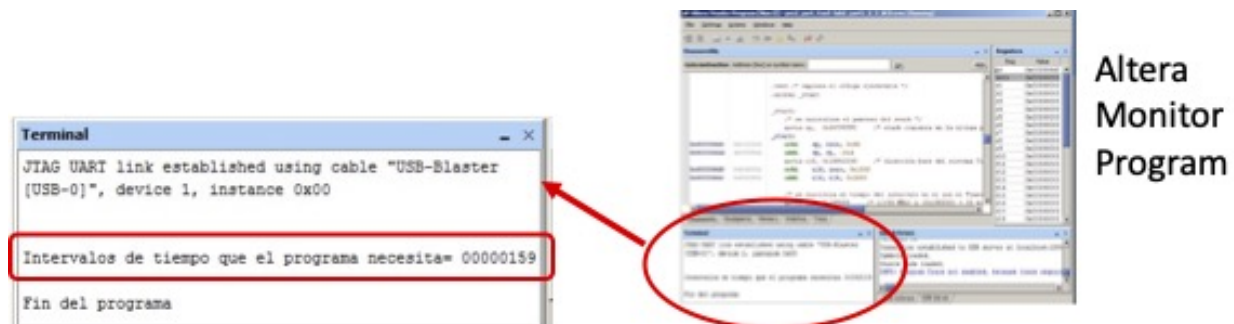


Figure 2: Visualization of the execution time of the Fibonacci program. The value of the number of 33 ms. intervals is shown in the terminal of AMP tool.

The assembly programs involved in this part of the lab assignment are:

- `lab2_part1_2_3_main.s`: main program (see Annex 1).
- `lab2_part1_2_3_fibo.s`: benchmark routine whose execution time is measured (see Annex 2).
- `lab2_part1_2_3_interrupts.s`: interrupt service routine that is invoked when the Timer indicates an interruption event requires attention because a 33 ms interval has ended (see Annex 3).
- `lab2_part1_2_3_excepciones.s`: routine that is called from `lab2_part1_2_3_interrupts.s` for increasing the counter of 33-ms. intervals (see Annex 4).
- `lab2_part1_2_3_JPEG.s`: routine that is called from `lab2_part1_2_3_main.s` to show in the terminal of AMP the number of 33-ms. intervals that have passed until the end of the execution of the benchmark program (see Annex 5).
- `lab2_part1_2_3_BCD.s`: routine that is called from `lab2_part1_2_3_JTAG.s` to transform a binary code into BCD format (see Annex 6).

- `lab2_part1_2_3.div.s`: routine that is called from `lab2_part1_2_3.BCD.s` to do the integer division (see Annex 7).

The flow diagram of the benchmark program that we will use to measure the execution time is shown in Figure 3. As we can see, the computer application invokes the interrupts service routine of the Timer in the main program (see `lab2_part1_2_3.main.s`).

The interrupt service routine allows to save a counter of 33-ms. intervals in one position of memory called `COUNTER` (see `lab2_part1_2_3.excepciones.s` file). Each event consist of the indication that has passed one interval of 33 ms. since the end of the previous time interval. So, `COUNTER` variable stores the numbers of 33-ms. intervals that have passed from the beginning to the end of the benchmark.

In parallel with the time measurement performed by the Timer, the main program executes the Fibonacci loop a number of times that is indicated by the constant called `ITERATIONS` (see `lab2_part1_2_3.main.s` file). When this loop ends, the content of the memory position `COUNTER` is read and its value is shown in the terminal of AMP tool (see `lab2_part1_2_3.JTAG.s` file). The binary code of `COUNTER` is transformed into BCD format and then, in an ASCII code. For generating the BCD code one or more divisions are needed. In these cases, one routine for divisions is invoked. This is required because the Nios II/e processor has not divisors (see `lab2_part1_2_3.JTAG.s` file).

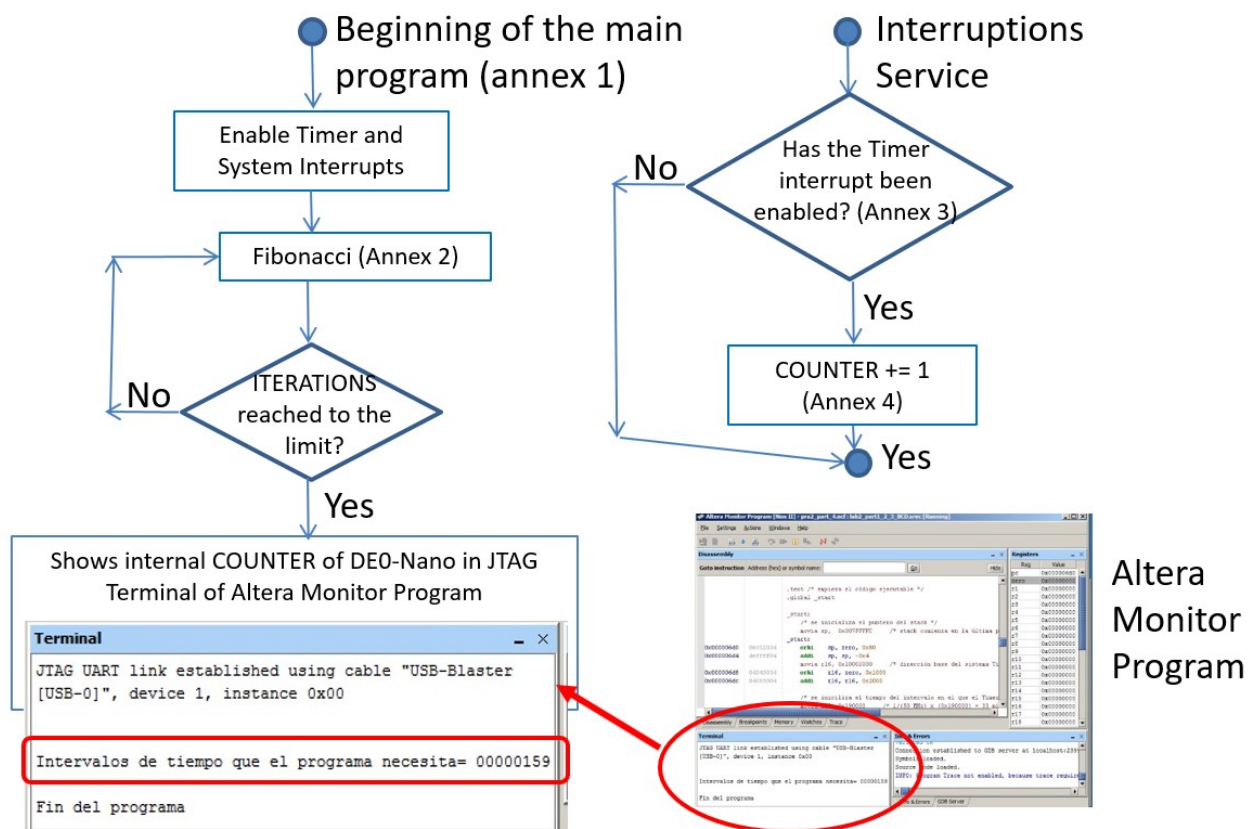


Figure 3: Flow diagram of the benchmark program for Part I.

### Lab Methodology

Begin a new project in the software tool called *Altera Monitor Program (AMP)* like it was done in the Lab Assignment 1. The FPGA configuration called *DE0-Nano Basic Computer* has to be selected. Additionally, the seven assembly files (`*.s`) indicated at the beginning of this lab activity must be included in the AMP project. Furthermore, it is needed to include in the AMP project that the programs and data are stored starting at the memory address `0x400` (`.start`). This is done as follows within the AMP tool:

## AMP software tool

```
[Step 1] Settings > System settings > Memory Settings >
.text { memory device = SDRAM/s1; start offset in device (hex) = 400
.data { memory device = SDRAM/s2; start offset in device (hex) = 400
```

Then, load the configuration into the FPGA of the DE0-Nano board:

```
[Step 2] Actions > Download System > Download
```

Afterwards, compile the programs and load the executable file into the memory:

```
[Step 3] Actions > Continue
```

Now, fill in Table 1 the value of time of the execution that is shown in the AMP terminal. This value for the execution time is the same value as the number of 33-ms. intervals that have elapsed during the Fibonacci program execution. The execution time will be compared to the time that will be obtained in the next two parts of this lab assignment. Please, focus on the `lab2_part1.2.3.main.s` program which initializes a constant: `ITERATIONS = 500000`.

Table 1: Execution time and Speed-up

| Processor & memory technology              | Execution time | Speed-up |
|--|----------------|----------|
| Nios II/e + SDRAM memory (Part I)          |                | 1x       |
| Nios II/e + on-chip SRAM memory (Part II)  |                |          |
| Nios II/f + SDRAM memory (Part III)        |                |          |
| Nios II/f + on-chip SRAM memory (Part III) |                |          |

Now, please, change `ITERATIONS` to 100000 in the `lab2_part1.2.3.main.s` file, and then, compile again the program and load it into the main memory of the computer configured in the board. Finally, execute the program and fill in the Table 1 with the value that is shown on the AMP terminal.

## Question 1

Is this new result of Speed-up reasonable? Justify your answer.

## Part II. Access to the on-chip memory with the Nios II/e economy soft processor

The goal of this second part consists in measuring real execution time of the Fibonacci program using the SRAM memory called *on-chip memory* that is located inside the chip in addition to the Nios II/e soft core. The main difference with Part I is that in this case, a SRAM memory is used. SRAM is built using another technology. Additionally, SRAM on-chip memory is physically located nearer the processor than the external SDRAM memory.

### Lab Methodology

Choose the previous project developed in Part I and the on-chip address memory space following the following steps:

**AMP software tool**

```
[Step 1] Settings > System Settings > Memory Settings >
.text - memory device = on-chip memory/s1(0x9000000 - 0x9001FFF)
.text { start offset in device (hex) = 400
.data { memory device = on-chip memory/s2 (0x9000000 { 0x9001FFF)
.data { start offset in device (hex) = 400
```

In the source code of the program (`lab2_part1.2.3_main.s`) the number of iterations must be 500000. Compile again the assembly files of the AMP project and load the executable file into the main memory of the computer configured in the DE0-Nano board. Then, run the program and fill in Table 1 with the value of the runtime displayed on the AMP terminal.

**Question 2**

Is this new result of temporary benefits reasonable? Justify your answer using the diagram shown in Figure 1 at the beginning of this document.

## Part III. Access to the cache memory of the fast Nios II/f soft processor

The goal of this part consists in measuring the real execution time of the Fibonacci program using the fast Nios II/f soft processor. This member of the Nios II soft processor family provides a higher performance level because it has a microarchitecture with hardware elements that the processor of the two previous activities does not have. The main relevant hardware characteristics of Nios II/f are:

- a six-stage pipelined data path
- first-level data cache memory
- first-level instruction cache memory
- dynamic branch predictor

### Lab Methodology

For this part, we will proceed to change the configuration of the board DE0-Nano to implement a new computer. Please, follow the step indicated below.

**AMP software tool**

```
[Step 1] Select the same AMP project used in Part II:
- Settings > System Settings >
[Step 2] Select a custom FPGA configuration:
- Select a system > <Custom System> >
[Step 3] Change the information file (nios_system.sopcinfo) and the FPGA
configuration file (DE0_Nano_Basic_Computer.sof) for the custom soft computer as
can be seen in Table 2 and Figure 4.
```

Table 2: Information and configuration files for Part III.

| Board    | Information file                  | Configuration file                       |
|----------|-----------------------------------|--|
| DE0-Nano | <code>nios_system.sopcinfo</code> | <code>DE0_Nano_Basic_Computer.sof</code> |

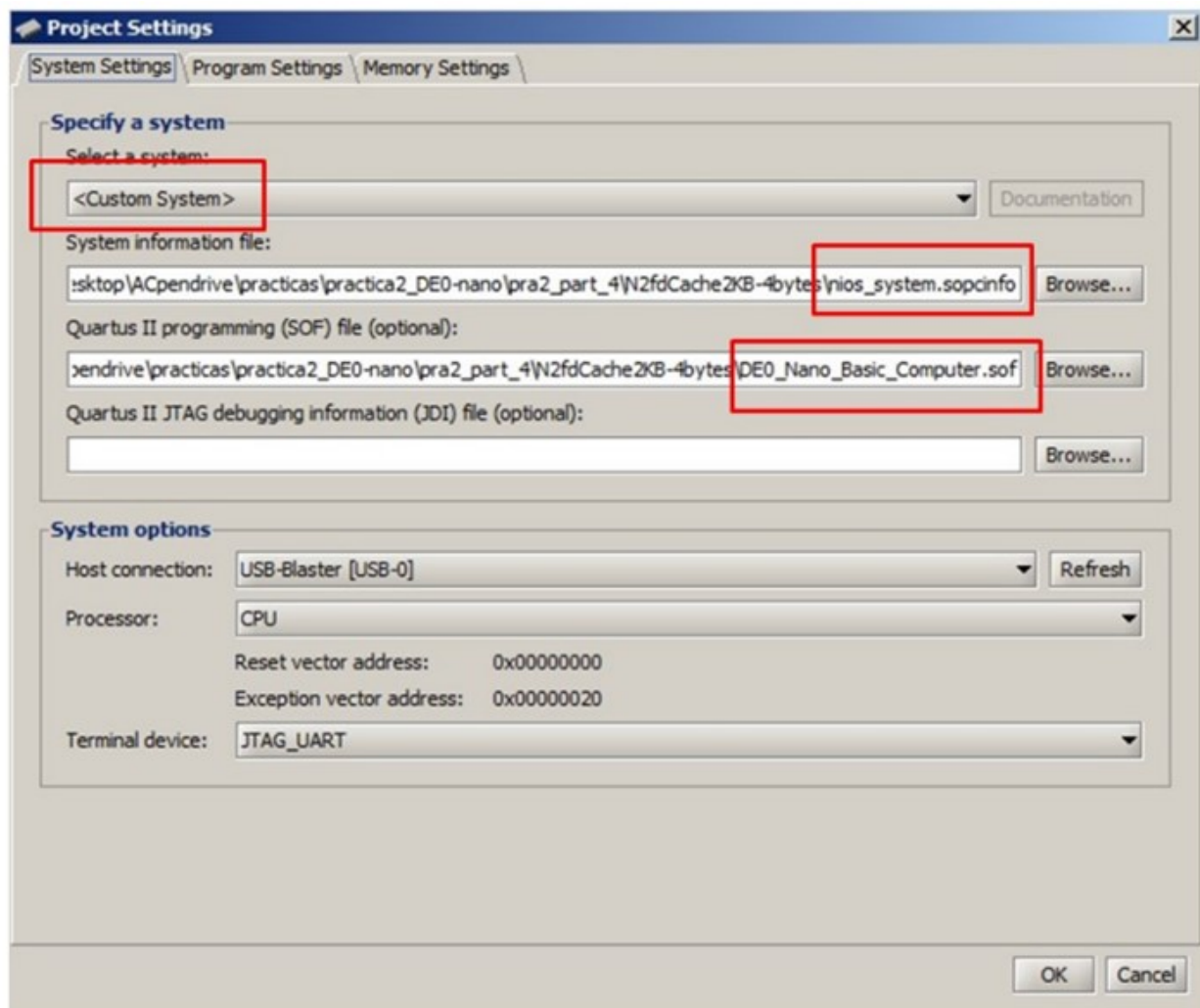


Figure 4: Part of the project where a custom computer architecture based on the Nios II/f is selected.

Additionally, one of the available memory address spaces must be selected from the two alternatives that can be chosen: on-chip or SDRAM. Furthermore, the code part (`.text`) and the data part (`.data`) must start from address `0x400`.

#### AMP software tool

```
Settings > System settings > Memory settings >
.text { start offset in device (hex) = 400
.data { start offset in device (hex) = 400
```

Fill in the Table 1 the number of 33 ms. intervals (execution time) that is shown on AMP terminal at the final of each execution of the program. Calculate the Speed-up that is obtained with the different versions of the Nios II processors using as benchmark the Fibonacci program. Take as base system (Speed-up = 1×) the Nios II/e processor with memory address space assigned to the external SDRAM memory of the DE0-Nano board. Finally, answer the following questions:

#### Question 3

Why do different versions of the Nios II/e processor provide such range of performance improvement?

## Question 4

Why the two computer configurations based on the Nios II/f processor need the same execution time?

## Question 5

Why the Nios II/e software core provides worse performance than Nios II/f core?

## Part IV. Discovery of the internal architecture of the cache memory of data

To discover the storage capacity and block size of the architecture from the data cache memory of the NIOS II/f processor we will use a simple program traversing a vector of bytes (V). The steps to follow in this practical activity are the following:

- Reduce the iterations number of the main program from 500000 to 50000 (file: lab2\_part1\_2.3-main.s)
- Modify by the way that is shown below the subroutine code of Fibonacci to limit simply to traversing a vector V of bytes.

```

...
movi r4, 0
movi r5, X
LOOP: bge r4, r5, END
      ldb r0, V(r4)
      addi r4, r4, P
      br LOOP
END:
...
.data
V:
.skip 65536
...
```

Observe that in the code above there are two parameters that need values: **X** and **P**. **X** represents the number of elements of the vector V that are going to be used to access them with a standard **P**. The standard **P** is the number of elements of the vector V that are in memory between two successive accesses with the `ldb` instruction. A new parameter is defined called **E** which represents the number of elements of the vector actually accessed with the `ldb` instruction. Thus,  $\mathbf{X} = \mathbf{P} \times \mathbf{E}$ .

- Then, Table 3 will be written with execution times values obtained in the same way as in the previous activities, measuring the execution times of the benchmark program. This time is mostly due to the one needed to traverse part of the elements of the vector V with a jump standard (**P**):
  - One to one ( $\mathbf{P} \rightarrow 1$ : `addi r4, r4, 1`)
  - Two to two ( $\mathbf{P} \rightarrow 2$ : `addi r4, r4, 2`)
  - Four to four ( $\mathbf{P} \rightarrow 4$ : `addi r4, r4, 4`)
  - Eight to eight ( $\mathbf{P} \rightarrow 8$ : `addi r4, r4, 8`)
  - Sixteen to sixteen ( $\mathbf{P} \rightarrow 16$ : `addi r4, r4, 16`)
  - Thirty-two to thirty-two ( $\mathbf{P} \rightarrow 32$ : `addi r4, r4, 32`)

The number of elements V that are necessary to make the **E** access will be **X** for each one of this standards. For example, for the first column of the table 3, the **X**, **E** and **P** values are the following:

- **X**→128 for **E**→128, **P**→1 (`movi r5, 128`)
- **X**→256 for **E**→128, **P**→2 (`movi r5, 256`)
- **X**→512 for **E**→128, **P**→4 (`movi r5, 512`)
- **X**→1024 for **E**→128, **P**→8 (`movi r5, 1024`)



- $X \rightarrow 2048$  for  $E \rightarrow 128$ ,  $P \rightarrow 16$  (movi r5, 2048)
- $X \rightarrow 4096$  for  $E \rightarrow 128$ ,  $P \rightarrow 32$  (movi r5, 4096)

Observe that, in all cases of  $X$ , the iterations number of the loop of the program is  $E=128$ . For this reason,  $X = P \times E$ . The number of access to the memory and the ldb instructions are also 128.

- Write the table 3 with the obtained data in the previous point and draw a graphic (see Figure 5). To write the table 3 follow the next procedure:

1. Execute AMP

2. New project

#### CHANGE CACHE

3. Settings > System Settings > System information file

+ browse > nios\_system.sopcinfo

4. Settings > System Settings > Quartus II Programming

file + browse > De0\_Nano\_Basic\_Computer.sof

5. Actions > Download system

#### CHANGE DATA

6. Modify the file of program: lab2\_part1\_2\_3\_main.s  
to establish new values of  $X$  and  $P$

7. Compile

8. Load

9. Execute the program wait for the time to appear in the AMP terminal and note it in the table 3.

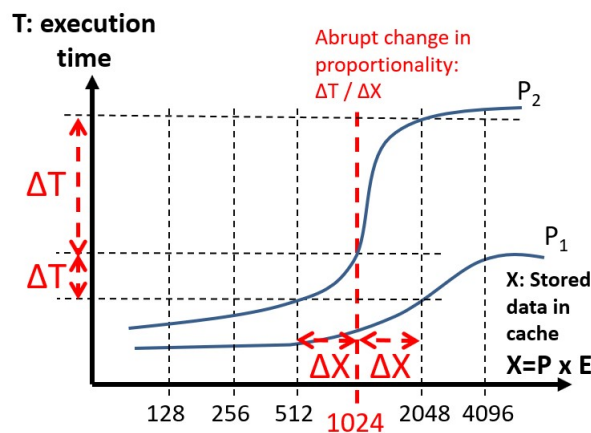
#### CONTINUE CHANGE DATA

#### CONTINUE CHANGE CACHE

**Table 3.** Table that is used in the Activity 4 to collect the times measures of execution

|                   | E: Bytes number of the vector V that are really accessed |     |     |      |      |      |
|-------------------|--|-----|-----|------|------|------|
| P: jump pattern   | 128  | 256 | 512 | 1024 | 2048 | 4096 |
| P= 1: from 1 to 1 |  |     |     |      |      |      |
| P= 2: from 2 to 2 |  |     |     |      |      |      |
| P= 4: from 4 to 4 |  |     |     |      |      |      |
| P= 8: from 8 to 8 |  |     |     |      |      |      |

- In base on the data obtained, deduce (discover) the total capacity of storage of the cache memory of data and size block of cache, thinking and justifying all the answers. Help: Remember that in theory classes we explained and calculated the concept access time average to memory:  $AMAT = \text{timeSuccess} + \text{failure frequency} \times \text{penalty}$



**Figure 5.** Graphic where is show the relationship between the execution time of the program and the number of elements accessed ( $E$ ) of the vector  $V$

These are the web pages used: [1, 2, 3, 4]



## References

- [1] Altera. Basic Computer System for the Altera DE-0 Nano Board, Altera Corporation - University Program. [ftp://ftp.intel.com/pub/fpgaup/pub/Intel\\_Material/12.1/Computer\\_Systems/DE0-Nano/DE0\\_Basic\\_Computer.pdf](ftp://ftp.intel.com/pub/fpgaup/pub/Intel_Material/12.1/Computer_Systems/DE0-Nano/DE0_Basic_Computer.pdf), 2012.
- [2] Intel. Introduction to Altera Nios II soft processor, Altera Corporation - University Program. [https://ftp.intel.com/Public/Pub/fpgaup/pub/Teaching\\_Materials/current/Tutorials/Nios2\\_introduction.pdf](https://ftp.intel.com/Public/Pub/fpgaup/pub/Teaching_Materials/current/Tutorials/Nios2_introduction.pdf), 2019.
- [3] Altera. Using the SDRAM Memory on Altera's DE2 Board with Verilog Design, Altera Corporation - University Program. [https://ftp.intel.com/Public/Pub/fpgaup/pub/Teaching\\_Materials/current/Tutorials/Nios2\\_introduction.pdf](https://ftp.intel.com/Public/Pub/fpgaup/pub/Teaching_Materials/current/Tutorials/Nios2_introduction.pdf), 2009.
- [4] Altera. Nios II Processor Reference Handbook, Altera Corporation. [https://ftp.intel.com/Public/Pub/fpgaup/pub/Teaching\\_Materials/current/Tutorials/Nios2\\_introduction.pdf](https://ftp.intel.com/Public/Pub/fpgaup/pub/Teaching_Materials/current/Tutorials/Nios2_introduction.pdf), 2014.

**Annex 1**

```
/* ***** * lab2_part1_2_3_main.s
*
* Main program of the Practice 3 of EC
*
* Initialize the Timer system of DE2
* Initialize and activate the interruptions system of the NIOS II processor
* Execute one loop of Fibonacci and show the number of intervals of 33 ms in HEX of * the DE2 board
*
* Subroutines: PRINT_JTAG (lab2_part1_2_3_JTAG.s), FIBONACCI (lab2_part1_2_3_fibo.s), * *****
.equ ITERATIONS, 500000
.text /*start the executable code*/
.global _start
_start:
    /* the stack pointer is initialized */
    movia sp, 0x007FFFFC /* stack starts in last memory position of SDRAM */
    movia r16, 0x10002000 /* base address of the internal Timer system */

    /*the time of the interval in which the timer generates an interrupt for
    performance analysis is started*/
    movia r12, 0x190000 /* 1/(50 MHz) x (0x190000) = 33 miliseconds */
    sthio r12, 8(r16) /* saves the half of the word from the initial value of timer*/
    srli r12, r12, 16 /* shifts the 16 bits value to the right */
    sthio r12, 0xC(r16) /* saves the word top half from the initial value of timer */

    /*the Timer is initialized, enabling its interrupts*/
    movi r15, 0b0111 /* START = 1, CONT = 1, ITO = 1 */
    sthio r15, 4(r16)

    /*NIOS II processor interrupt is enabled*/
    movi r7, 0b011 /* the interrupt bit mask is initialized for level 0 */
    wrctl ienable, r7 /* Timer) y nivel 1 (pushbuttons) */
    movi r7, 1
    wrctl status, r7 /* NIOS II interrupts are activated*/
```

```
    movia r14, ITERATIONS /* initializes the Fibonacci iteration counter */
    addi r17, r0, 0 /* initializes the interval counter of the program "r17" /

LOOP: beq r14, r0, END /* the Fibonacci loop is executed */

    call FIBONACCI
    addi r14, r14, -1
    br LOOP

END: movi r7, 0

    wrctl status, r7 /* interrupt processing is disabled in the NIOS II */
    call PRINT_JTAG /* the number of 33 ms intervals is displayed in the AMP
    terminal */
    IDLE: br IDLE /* the main program finish */

.data
.global COUNTER
COUNTER:
    .skip 4 /* memory position that saves the Timer interval counter */ .end
```

**Annex 2**

```
/****** * lab2_part1_2_3_fibo.s
*
* Subroutine: Executes the Fibonacci Series computation for 8 numbers
*
* Call from: lab2_part1_2_3_main.s
***** */
text
.global FIBONACCI
FIBONACCI:
    subi sp, sp, 24 /* reserve space for the Stack */
    stw r4, 0(sp)
    stw r5, 4(sp)
    stw r6, 8(sp)
    stw r7, 12(sp)
    stw r8, 16(sp)
    stw r9, 20(sp)

    movia r4, N /* r4 points N */
    ldw r5, (r4) /* r5 is the counter initialized with N */
    addi r6, r4, 4 /* r6 points to the first Fibonacci numbers */
    ldw r7, (r6) /* r7 contains the first Fibonacci number */
    addi r6, r4, 8 /* r6 points to the first Fibonacci numbers */
    ldw r8, (r6) /* r7 contains the second Fibonacci number */
    addi r6, r4, 0x0C /* r6 points to the first Fibonacci number result */
    stw r7, (r6) /* Save the first Fibonacci number */
    addi r6, r4, 0x10 /* r6 points to the second Fibonacci number result */
    stw r8, (r6) /* Save the second Fibonacci number */
    subi r5, r5, 2 /* Decrease the counter in 2 numbers already saved */
LOOP:
    beq r5, r0, STOP /* Finishes when r5 = 0 */
    subi r5, r5, 1 /* Decrement the counter */
    addi r6, r6, 4 /* Increment the list pointer */
```

```
add r9, r7, r8 /* adds two previous numbers */  
stw r9, (r6) /* saves the result */  
mov r7, r8  
mov r8, r9  
br LOOP
```

STOP:

```
ldw r4, 0(sp)  
ldw r5, 4(sp)  
ldw r6, 8(sp)  
ldw r7, 12(sp)  
ldw r8, 16(sp)  
ldw r9, 20(sp)  
addi sp, sp, 24 /* releases the reserved stack */  
ret
```

.data

N:

```
.word 8 /* Fibonacci Numbers */
```

NUMBERS:

```
.word 0, 1 /* First 2 numbers */
```

RESULT:

```
.skip 32 /* Space for 8 numbers of 4 bytes */
```

.end

**Annex 3**

```
/****** * subroutine: lab2_part1_2_3.int
*
* The program AMP (Altera Monitor Program) locates the section ".reset"
* in the direction of the memory of the rest that is specified in the Nios II configuration
* which is determined with SOPC Builder.
* "ax" is needed to indicate that this section is reserved and executed
*/
.section .reset, "ax"
movia r2, _start
jmp r2 /* jump to the main program */
/******
* The program AMP (Altera Monitor Program) located automatically the section ".exceptions"
* in the direction of the memory of the rest that is specified in the Nios II configuration
* which is determined with SOPC Builder.
* "ax" is needed to indicate that this section is reserved and executed
*
* Subroutines: INTERVAL_TIMER_ISR (lab2_part1_2_3_excepciones.s)
*/
.section .exceptions, "ax"
.global EXCEPTION_HANDLER
EXCEPTION_HANDLER:
    subi sp, sp, 16 /* reserve the Stack */
    stw et, 0(sp)
    rdctl et, ctl4
    beq et, r0, SKIP_EA_DEC /* interruption is not external */
    subi ea, ea, 4 /* ea must be decreased in 1 instruction */
    /* for external interruptions, so that */
    /* the interrupted instruction will be executed after eret (Exception Return) */

SKIP_EA_DEC:
    stw ea, 4(sp) /* save registers to the Stack */
    stw ra, 8(sp) /* is required if a call has been used */
```

```
    stw r22, 12(sp)

    rdctl et, ctl4

    bne et, r0, CHECK_LEVEL_0 /* the exception is an external interrupt */

NOT_EI: /* exception for not implemented instructions or TRAPs */

    br END_ISR

CHECK_LEVEL_0: /* Timer has Level 0 interrupts */

    call INTERVAL_TIMER_ISR

    br END_ISR

END_ISR:

    ldw et, 0(sp) /* restore previous registers values */

    ldw ea, 4(sp)

    ldw ra, 8(sp)

    ldw r22, 12(sp)

    addi sp, sp, 16

eret

.end
```



**Annex 4**

```
/******  
* lab2_part1_2_3_excepciones.s  
*  
* Subroutine that increases an interval counter of the Timer  
*  
* Call from: lab2_part1_2_3_interrupts.s  
***** /  
  
.extern COUNTER  
  
.global INTERVAL_TIMER_ISR  
  
INTERVAL_TIMER_ISR:  
  
    subi sp, sp, 8 /* reserved space in the stack */  
  
    stw r10, 0(sp)  
  
    stw r11, 4(sp)  
  
    movia r10, 0x10002000 /* base address of Timer */  
  
    sthio r0, 0(r10) /* initialize to 0 the interruption */  
  
    movia r10, COUNTER /* base address of the Timer interval counter */  
  
    ldw r11, 0(r10)  
  
    addi r11, r11, 1 /* adds the timer interval counter */  
  
    stw r11, 0(r10)  
  
    ldw r10, 0(sp)  
  
    ldw r11, 4(sp)  
  
    addi sp, sp, 8 /* release the stack */  
  
    ret  
  
.end
```

**Annex 5**

```
/******  
* file lab2_part1_2.3_JTAG.s  
* AC - Practice 2 - Exercise 1  
* Subroutines related to the display of a character in the terminal  
* input parameters:  
* r10 = ascii value of the character to be processed  
* output parameters: none  
*****/  
  
.extern COUNTER /* variable defined in the main program */  
  
/*  
Subroutine: PRINT_JTAG  
Displays in AMP JTAG terminal the contents of the external memory position COUNTER  
*/  
  
.global PRINT_JTAG  
PRINT_JTAG:  
    subi sp, sp, 24 /* stack management */  
    stw r2, 4(sp)  
    stw r3, 8(sp)  
    stw r4, 12(sp)  
    stw r10, 16(sp)  
    stw r17, 20(sp)  
    stw ra, 24(sp)  
  
    movia r3, TEXT  
    call WRITE_TEXT_JTAG /* write in JTAG terminal fixed text */  
  
    movia r17, COUNTER /* base address of the Timer interval counter */  
    ldw r4, 0(r17)  
    call BCD /* r4= binary value, r2= BCD value */  
  
    call WRITE_VALUE_JTAG /* writes to JTAG terminal BCD value */  
    movia r3, TEXT_FIN  
    call WRITE_TEXTTO_JTAG /* write in JTAG terminal fixed text */  
  
    ldw r2, 4(sp) /* stack management */
```

```
    ldw r3, 8(sp)

    ldw r4, 12(sp)

    ldw r10, 16(sp)

    ldw r17, 20(sp)

    ldw ra, 24(sp)

    addi sp, sp, 24

    ret

/*
Subroutine: WRITE_TEXT_JTAG
write a string of characters by jtag terminal
parameters: r3, string pointer
*/

.global WRITE_TEXT_JTAG
WRITE_TEXT_JTAG:
    subi sp, sp, 12

    stw r3, 4(sp)

    stw r10, 8(sp)

    stw ra, 12(sp)

BUC:
    ldb r10, 0(r3) /* loads 1 byte from character string address */
    beq r10, r0, WITH /* if reads a 0 it means that have reached the end of the chain
and goes out of the loop
*/

    call WRITE_JTAG /* subroutine that shows the byte by JTAG-UART */

    addi r3, r3, 1 /* next byte */

    br BUC /* close the loop */

WITH:
    ldw r3, 4(sp)

    ldw r10, 8(sp)

    ldw ra, 12(sp)

    addi sp, sp, 12

    ret

/*
```

Subroutine: WRITE\_VALUE\_JTAG

writes a value to BCD by JTAG terminal

parameters: r2, BCD value

\*/

.global WRITE\_VALUE\_JTAG

WRITE\_VALUE\_JTAG:

subi sp, sp, 16

stw r2, 4(sp)

stw r4, 8(sp)

stw r10, 12(sp)

stw ra, 16(sp)

addi r4, r0, 8 /\* 8 nibles BCD counter \*/

VALUE:

andhi r10, r2, 0xf000 /\* extracts the 4 more significant bytes BCD \*/

srli r10, r10, 28 /\* r10 result is shifted to the right 28 bits \*/

addi r10, r10, 0x30 /\* addition 0x30: BCD -> ASCII \*/

call ESCRIBIR\_JTAG /\* shows ASCII \*/

subi r4, r4, 1 /\* counter of nibble - \*/

slli r2, r2, 4 /\* next nibble BCD \*/

bne r4, r0, VALUE

ldw r2, 4(sp)

ldw r4, 8(sp)

ldw r10, 12(sp)

ldw ra, 16(sp)

addi sp, sp, 16

ret

global WRITE\_JTAG

WRITE\_JTAG:

subi sp, sp, 12 /\* the used registers are stored in the stack \*/

stw r3, 4(sp)

stw r22, 8(sp)

stw ra, 12(sp)

```
        movia r22, 0x10001000 /* base address of JTAG */
AGAIN: /* survey: check if there is space to write */
        ldwio r3, 4(r22) /* read register of JTAG-UART port */
        andhi r3, r3, 0xffff /* selects the 16 bits more significant */
        beq r3, r0, AGAIN /* ¿WSPACE=0? */

WRT: /* sends the character by writting in JTAG-UART */
        stwio r10, 0(r22)

END: ldw r3, 4(sp) /* retrieve the logs from the stack and return */
        ldw r22, 8(sp)
        ldw ra, 12(sp)
        addi sp, sp, 12

        ret

/*
* Data zone
*/ TEXT: .asciz " _n_nTime intervals that the program needs= "
TEXT_END:
.asciz " _n_nEnd of the program "
.end
```

**Annex 6**

```
/******  
* lab2_part1_2_3_BCD.s  
*  
* Subroutine: transform the binary code to BCD  
*  
* Call from: lab2_part1_2_3_JTAG.s  
* Subroutine: DIV (lab2_part1_2_3_div.s)  
*  
* arguments: r4= binary value  
* results: r2= BCD value  
*  
*****/  
  
.text  
  
.global BCD  
  
BCD:  
  
    subi sp, sp, 24 /* memory reserve in the Stack */  
  
    stw r3, 0(sp)  
  
    stw r4, 4(sp)  
  
    stw r5, 8(sp)  
  
    stw r6, 12(sp)  
  
    stw r10, 16(sp)  
  
    stw r31, 20(sp) /* by possible nested call */  
  
    beq r4, r0, END /* if binary == 0 goto END */  
  
    addi r5, r0, 10 /* r5 = 10 for divide BCD */  
  
    add r6, r0, r0 /* i = 0 */  
  
    add r10, r0, r0 /* r10 = 0 */  
  
LOOP2: bge r0, r4, END /* while binary value > 0 */  
  
    call DIV /* calls division with r4 = dividend, r5 = divisor; returns r3= quotient,  
    r2= rest */  
  
    sll r2, r2, r6 /* shifts the result 4 bits to the left except for the first number */  
  
    or r10, r10, r2 /* accumulates the result in r10 */
```

```
    addi r6, r6, 4 /* updated r6 += 4 */

    bgt r5, r3, END /* if quotient < 10 goto END */

    add r4, r3, r0 /* r4 = previous quotient, */

    jmp LOOP2 /* if quotient >= 10 goto LOOP2 */

END: sll r3, r3, r6 /* shifts the final quotient various 4 bits to the left */

    or r10, r10, r3 /* accumulates the result in r10 */

    add r2, r10, r0 /* puts the result in the output register r2 */

    ldw r3, 0(sp)
    ldw r4, 4(sp)
    ldw r5, 8(sp)
    ldw r6, 12(sp)
    ldw r10, 16(sp)
    ldw r31, 20(sp)

    addi sp, sp, 24 /* releases the reserved stack */

    ret

.end
```



**Annex 7**

```
/******  
* lab2_part1_2_3_div.s  
* Entire division for NIOS II that is required when the processor does not have  
* hardware of one divisor  
*  
* Reference:  
* http://stackoverflow.com/questions/938038/assembly-mod-algorithm-on-processor-with-no-division-operator  
*  
* Call from: lab2_part1_2_3_JTAG.s  
*  
* arguments: r4= dividend, r5= divisor  
* results: r2= rest, r3= quotient  
*  
*****/  
.text  
.global DIV  
DIV:  
    subi sp, sp, 16 /* reserve space in the Stack */  
    stw r6, 0(sp)  
    stw r7, 4(sp)  
    stw r10, 8(sp)  
    stw r11, 12(sp)  
  
    beq r5, r0, END /* if divisor == 0 goto END */  
  
START:add r2, r4, r0 /* rest = dividend */  
    add r6, r5, r0 /* r6 = next_multiple = divisor */  
    add r3, r0, r0 /* quotient = 0 */  
  
LOOP: add r7, r6, r0 /* r7 = multiple = next_multiple */  
    slli r6, r7, 1 /* next_multiple = left_shift(multiple,1) */  
    sub r10, r2, r6 /* r10 = resto - next_multiple */  
    sub r11, r6, r7 /* r11 = next_multiple - multiple */  
  
    blt r10, r0, LOOP2 /* if r10 < 0 goto LOOP2 */
```

```
    bgt r11, r0, LOOP /* if r11 > 0 goto LOOP */

LOOP2: bgt r5, r7, END /* while divisor <= multiple */

    slli r3, r3, 1 /* quotient << 1 */

    bgt r7, r2, MOVE /* if multiple <= rest */

    sub r2, r2, r7 /* then rest = rest - multiple */

    addi r3, r3, 1 /* quotient += 1 */

MOVE:

    srli r7, r7, 1 /* multiple = right_shift(multiple, 1) */

    jmp LOOP2

END: ldw r6, 0(sp)

    ldw r7, 4(sp)

    ldw r10, 8(sp)

    ldw r11, 12(sp)

    addi sp, sp, 16 /* releases the reserved stack */

    ret

.end
```