Lab assignment 4:

Nios V multiprocessor implementation, parallel programming, and performance evaluation

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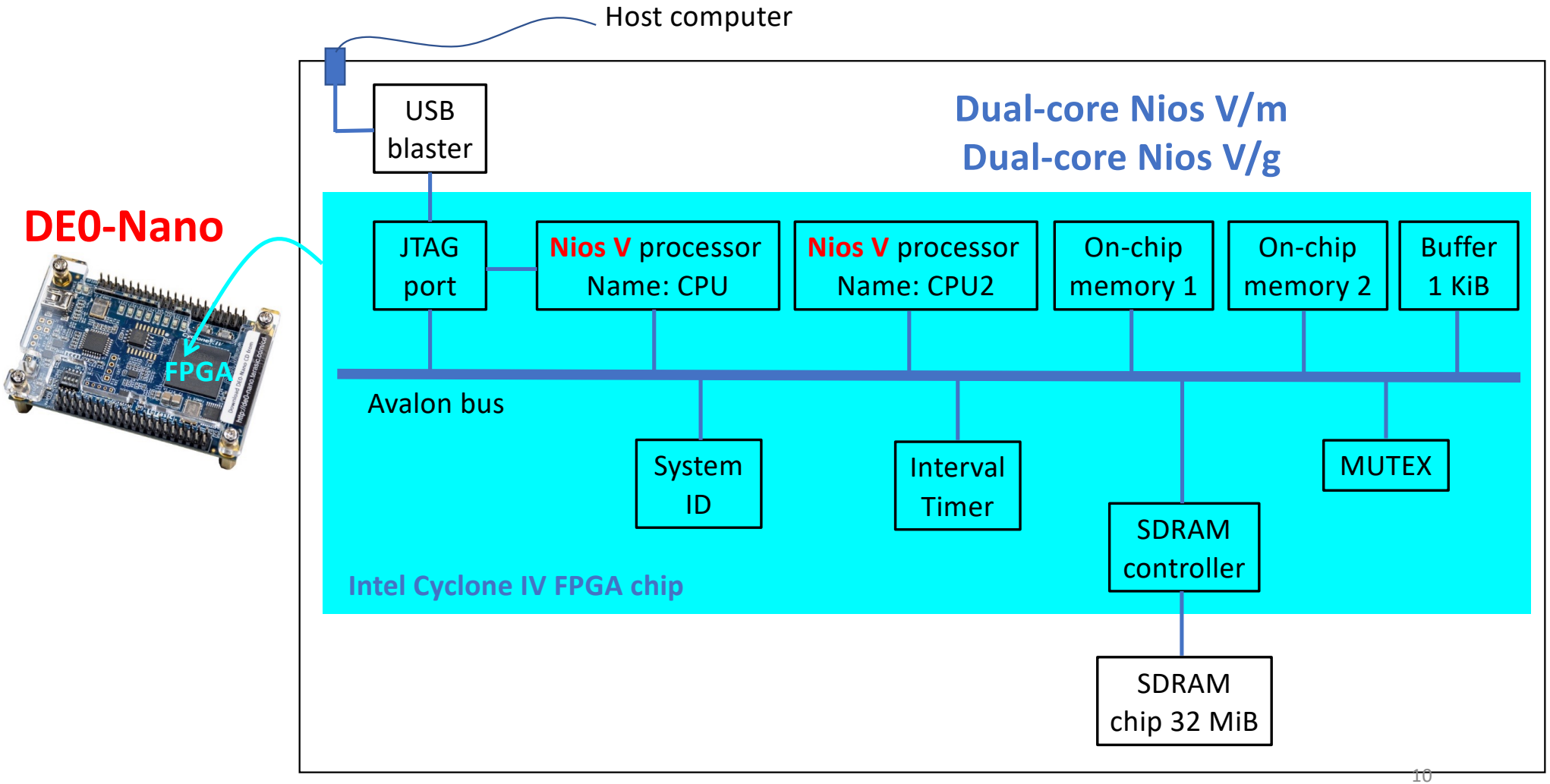
Main goals

- Implement parallel programs on two Nios V multiprocessors with the goal of significantly reducing the execution time of the programs.
- Measure and compare the execution times of the parallel programs with the corresponding sequential versions using the DE0-Nano board.
- Evaluate the performance of the Nios V multiprocessors for different amounts of processed data.
- Compare the performance of the various Nios V multiprocessors.
- Implement the parallel programs on the DE0-Nano board.
- Keywords: multithreaded programming, parallelism, multiprocessors, thread synchronization, performance evaluation, Nios V, DE0-Nano.

Scheduling: 3 sessions, 1 session/week

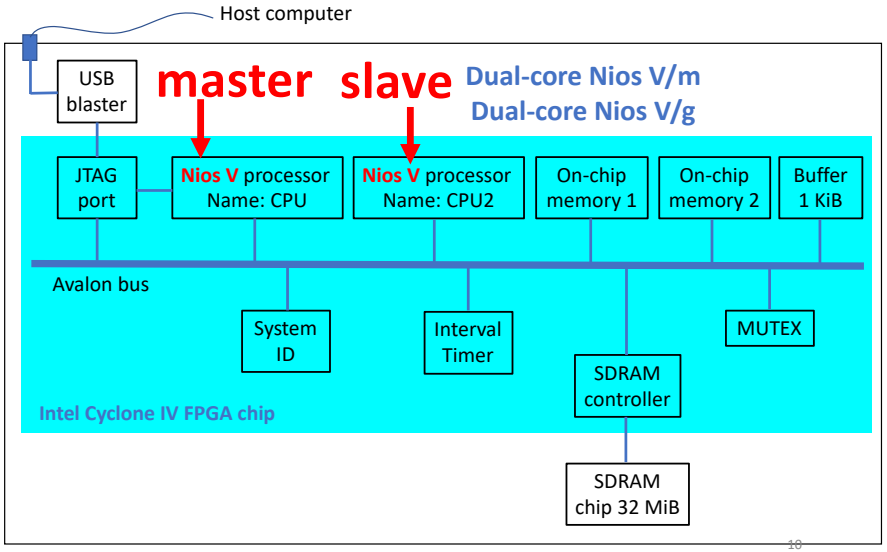
- Session 1:
  - Microarchitecture of Nios V-based parallel SoC computer + memory hierarchy + software
- tools + Nios V Command Shell.
  - Tutorial 1: Hi_guys (0.5 h).
  - Tutorial 2: Hi_mutex (0.5 h).
- Session 2:
  - Tutorial 3: Matrix × Vector. • Proposal: Matrix × Matrix.
- Session 3:
  - Implementation of Matrix × Matrix algorithm using dual-core Nios V/m and Nios V/g multiprocessors

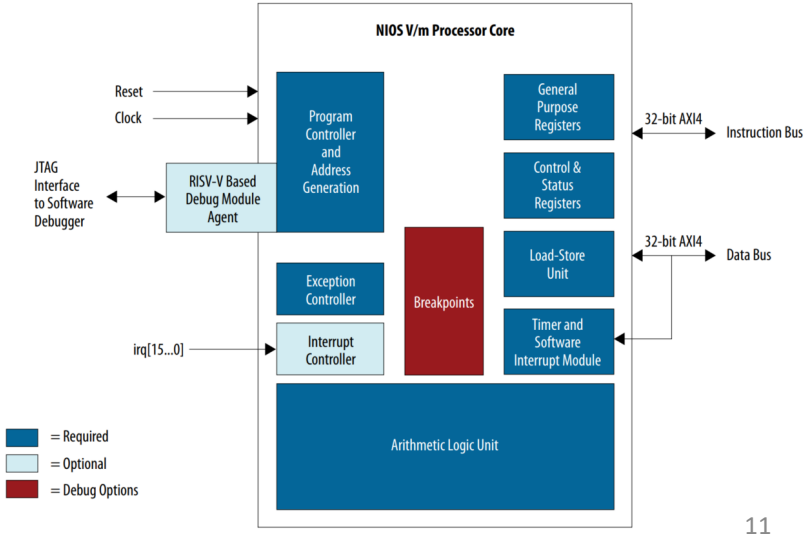
Soft SoC based on Nios V dual-core multiprocessors



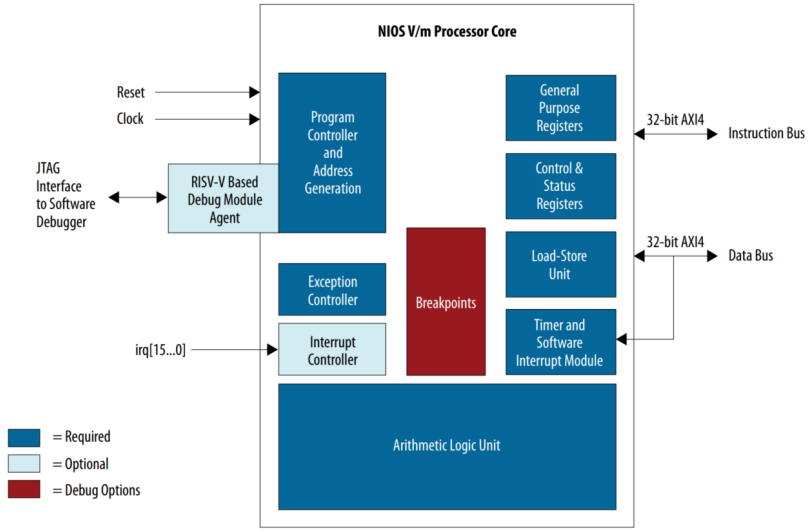
Implementation of Nios V dual-core multiprocessors on DE0-Nano board

- FPGA desing: Intel Quartus Prime Standard Edition Design Suite 24.1
- Two different Nios V dual cores (cores: **master** & **slave**)
  - 2 x Nios V/m (DualCoreNiosVm): pipelined, without cache
  - 2 x Nios V/g (DualCoreNiosVg): pipelined, iCache (4 KiB) + dCache (4 KiB) + hardware multiplier





Memory addresses for Nios V cores



32 bits architecture

32 bits address