

Computer Architecture - Lab Assignment 1

RISC-V instruction set architecture and programming of Nios V/m processor

This is an introductory exercise that involves Intel/Altera's Nios V/m soft processor and its RISC-V assembly language. It uses a simple computer hardware system, called the *DE0-Nano Basic Computer*, which includes the Nios V/m processor. The hardware system is implemented as an electronic circuit that is downloaded into the FPGA device on the *Terasic DE0-Nano* board ([1]). This exercise illustrates how programs written in the RISC-V assembly language can be executed on the DE0-Nano board.

To prepare for this exercise you have to know the Nios V/m processor architecture and its RISC-V assembly language ([2, 3]). This lab assignment consists of four parts. Part I below describes the procedure for compiling, linking RISC-V architecture assembler programs, and running the programs on the DE0-Nano board.

Part I. Executing an example program

In this part we will use the **Nios V Command Shell** to download the DE0-Nano Basic Computer SoC circuit into the FPGA device and execute a sample program. This tool is part of the *Intel/Altera Quartus Prime Standard 23.1 Design Suite* ([3]).

Perform the following:

1. Turn on the power to the DE0-Nano board.
2. Open the Nios V Command Shell, which leads to the window in Figure 1.

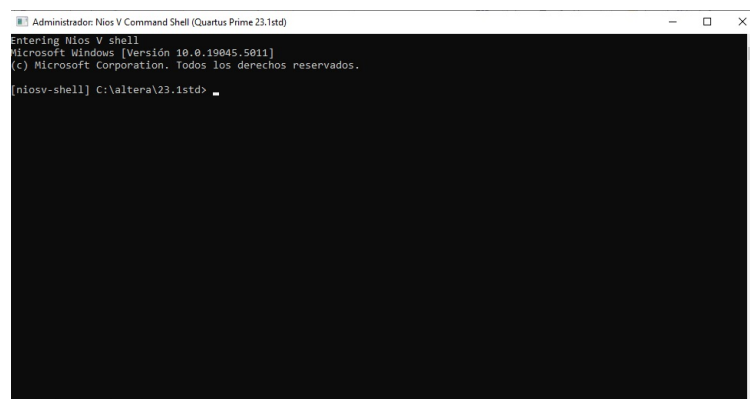


Figure 1: The Nios V Command Shell window.

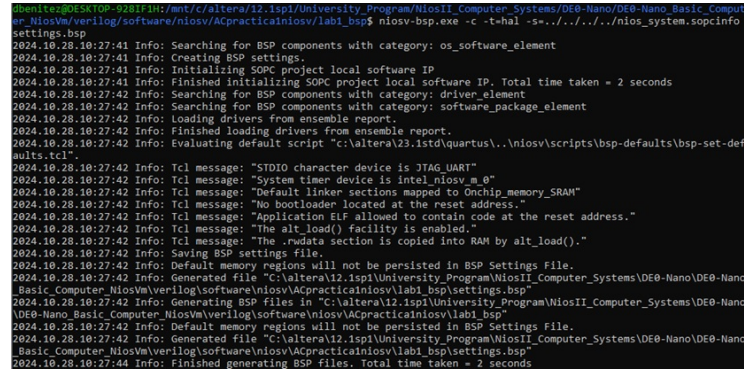
To run an application program it is necessary to create a new **BSP project**.

3. Create a new BSP directory called for example: `lab1_bsp`.

4. Select a predesigned *System-on-Chip* file: `nios_system_22jul24.sopcinfo`. This file was obtained by using the *Platform Designer* tool ([3]). The computer hardware system integrates a Nios V/m soft processor and a 8 KB on-chip SRAM memory, in addition to an I/O controller for the LEDs available in the board.
5. Execute the following command in the Nios V Command Shell window.

```
$ cd lab1_bsp
$ bash
$ niosv-bsp.exe -c -t=hal -s=nios_system_22jul24.sopcinfo settings.bsp
```

The output provides two files called: `settings.bsp` and `linker.x`. Figure 2 shows the messages displayed in the Nios V Command Shell window.



```

C:\Users\DE0-Nano\Documents\NiosII Computer Systems\DE0-Nano\DE0-Nano Basic Computer\NiosV\verilog\software\niosv\ACPractical\niosv\lab1_bsp> niosv-bsp.exe -c -t=hal -s=.../nios_system.sopcinfo settings.bsp
2024.10.28.10:27:41 Info: Searching for BSP components with category: os_software_element
2024.10.28.10:27:41 Info: Creating BSP settings.
2024.10.28.10:27:41 Info: Initializing SOPC project local software IP
2024.10.28.10:27:41 Info: Finished initializing SOPC project local software IP. Total time taken = 2 seconds
2024.10.28.10:27:42 Info: Searching for BSP components with category: driver_element
2024.10.28.10:27:42 Info: Searching for BSP components with category: software_package_element
2024.10.28.10:27:42 Info: Loading drivers from ensemble report.
2024.10.28.10:27:42 Info: Finished loading drivers from ensemble report.
2024.10.28.10:27:42 Info: Evaluating default script "c:\altera\23.1std\quartus\..niosv\scripts\bsp-defaults\bsp-set-defaults.tcl".
2024.10.28.10:27:42 Info: Tcl message: "STDIO character device is JTAG_UART"
2024.10.28.10:27:42 Info: Tcl message: "System timer device is intel_nios_m_0"
2024.10.28.10:27:42 Info: Tcl message: "Default linker sections mapped to Onchip_memory_SRAM"
2024.10.28.10:27:42 Info: Tcl message: "No bootloader located at the reset address."
2024.10.28.10:27:42 Info: Tcl message: "Application ELF allowed to contain code at the reset address."
2024.10.28.10:27:42 Info: Tcl message: "The alt_load() facility is enabled."
2024.10.28.10:27:42 Info: Tcl message: "The .rwdata section is copied into RAM by alt_load()."
2024.10.28.10:27:42 Info: Saving BSP settings file.
2024.10.28.10:27:42 Info: Default memory regions will not be persisted in BSP Settings File.
2024.10.28.10:27:42 Info: Generated file "C:\altera\12.isp1\University Program\NiosII Computer Systems\DE0-Nano\DE0-Nano Basic Computer\NiosV\verilog\software\niosv\ACPractical\niosv\lab1_bsp\settings.bsp"
2024.10.28.10:27:42 Info: Generating BSP files in "C:\altera\12.isp1\University Program\NiosII Computer Systems\DE0-Nano\DE0-Nano Basic Computer\NiosV\verilog\software\niosv\ACPractical\niosv\lab1_bsp"
2024.10.28.10:27:42 Info: Default memory regions will not be persisted in BSP Settings File.
2024.10.28.10:27:42 Info: Generated file "C:\altera\12.isp1\University Program\NiosII Computer Systems\DE0-Nano\DE0-Nano Basic Computer\NiosV\verilog\software\niosv\ACPractical\niosv\lab1_bsp\settings.bsp"
2024.10.28.10:27:44 Info: Finished generating BSP files. Total time taken = 2 seconds

```

Figure 2: Messages displayed after executing the `niosv-bsp.exe` command.

6. Now, create a new directory for the RISC-V assembler program written in RISC-V assembly language and its building, for example: `lab1_bin`.
7. Copy the sample program `lab1_part1.s` to this directory.
8. The source file `lab1_part1.s` contains the application program. This file specifies the starting point in the selected application program. The default symbol is `start`, which is used in the selected sample program.
9. Execute the following command in the Nios V Command Shell window for assembling the source code.

```
$ cd lab1_bin
$ riscv32-unknown-elf-as.exe lab1_part1.s -o lab1_part1.s.obj
```

If no error are encountered, the assembler provides an output file called: `lab1_part1.s.obj`.

10. Execute the following command in the Nios V Command Shell window for linking and reporting the program.

```
$ riscv32-unknown-elf-ld.exe -g -T ../lab1_bsp/linker.x -nostdlib
-e _start -u _start --defsym __alt_stack_pointer=0x08001F00 --defsym
__alt_stack_base=0x08002000 --defsym __alt_heap_limit=0x8002000 --defsym
__alt_heap_start=0x8002000 -o lab1_part1.elf lab1_part1.s.obj
$ niosv-stack-report.exe -p riscv32-unknown-elf- lab1_part1.elf
```

If no error are encountered, the linker provides an output file called: `lab1_part1.elf`. Figure 3 shows the messages displayed in the Nios V Command Shell window.

11. Execute the following command in the Nios V Command Shell window for generating a disassembled RISC-V program.

```
$ riscv32-unknown-elf-objdump.exe -Sdtx lab1_part1.elf > lab1_part1.elf.objdump
```

```

doemitez@DE0-Nano:~/Nios11/University_Program/Nios11_Computer_Systems/DE0-Nano/DE0-Nano_Basic_Computer$ riscv32-unknown-elf-ld.exe -g -I ../practical_bsp/linker.x -nostdlib -e start -u start -defsym __alt_stack_pointer=0x00001f00 -defsym __alt_stack_base=0x00002000 -defsym __alt_heap_limit=0x00002000 -defsym __alt_heap_start=0x00002000 -o lab1_part1.elf lab1_part1.s.obj
riscv32-unknown-elf-ld.exe: warning: lab1_part1.elf has a LOAD segment with R/W permissions
niosv-stack-report.exe -p riscv32-unknown-elf- lab1_part1.elf
lab1_part1.elf
* 184 B - Program size (code + initialized data).
* 256 B - Free for stack.
* 0 B - Free for heap.
niosv-stack-report.exe -sdtx lab1_part1.elf > lab1_part1.elf.objdump
riscv32-unknown-elf-objcopy.exe -O binary lab1_part1.elf lab1_part1.hex

```

Figure 3: Messages displayed after executing the `riscv32-unknown-elf-ld.exe` and `niosv-stack-report.exe` commands.

The output file is called: `lab1_part1.elf.objdump`. Figure 4 shows the RISC-V machine instructions, addresses and disassembled instructions that are included in the `lab1_part1.elf.objdump` file.

```

3 lab1_part1.elf
4 architecture: riscv:rv32, flags 0x0000112:
5 EXEC_P, HAS_SYMS, D_PAGED
6 start address 0x00000000
7
8 Program Header:
9 0x70000003 off 0x000010b8 vaddr 0x00000000 paddr 0x00000000 align 2**0
10 filesz 0x0000002e memsz 0x00000000 flags r--
11 LOAD off 0x00001000 vaddr 0x00000000 paddr 0x00000000 align 2**12
12 filesz 0x00000004 memsz 0x00000004 flags r-x
13 LOAD off 0x000010b4 vaddr 0x000000b4 paddr 0x000000b8 align 2**12
14 filesz 0x00000004 memsz 0x00000004 flags rw-
15 LOAD off 0x000000bc vaddr 0x000000bc paddr 0x000000bc align 2**12
16 filesz 0x00000000 memsz 0x00000000 flags rw-
17
18 Sections:
19 Idx Name Size VMA LMA File off Align
20 0 .exceptions 00000000 00000000 00000000 000010b8 2**0
21
22 1 .text 00000004 00000000 00000000 00001000 2**2
23 CONTENTS, ALLOC, LOAD, READONLY, CODE
24 2 .rodata 00000000 000000b4 000000bc 000010b8 2**0
25 CONTENTS, ALLOC, LOAD, DATA
26 3 .rwdata 00000004 000000b4 000000b8 000010b4 2**0
27 CONTENTS, ALLOC, LOAD, DATA
28 4 .bss 00000000 000000bc 000000bc 000010bc 2**0
29 ALLOC
30 5 .Onchip_memory_SRAM 00000000 000000bc 000000bc 000010b8 2**0
31 CONTENTS
32 6 .Onchip_memory 00000000 00000020 00000020 000010b8 2**0
33 CONTENTS
34 7 .riscv.attributes 0000002e 00000000 00000000 000010b8 2**0
35 CONTENTS, READONLY
36
37 SYMBOL TABLE:
38 00000000 l d .exceptions 00000000 .exceptions
39 00000000 l d .text 00000000 .text
40 000000b4 l d .rodata 00000000 .rodata
41 000000b4 l d .rwdata 00000000 .rwdata
42 000000bc l d .bss 00000000 .bss
43 000000bc l d .Onchip_memory_SRAM 00000000 .Onchip_memory_SRAM
44 00000020 l d .Onchip_memory 00000000 .Onchip_memory
45 00000000 l d .riscv.attributes 00000000 .riscv.attributes
46 00000000 l df *ABS* 00000000 lab1_part1.s.obj
47 000000b4 l .rwdata 00000000 LEDG_bits
48 00000024 l .text 00000000 DO_DISPLAY
49 00000032 l .text 00000000 DO_BUTTON
50
51 Disassembly of section .text:
52 00000000 <start>:
53 00000000: 10000037 lui a6,0x10000
54 00000004: 01000013 addi a6,a6,16 # 10000010 <_alt_mem_Onchip_memory+0x7000010>
55 00000008: 10000077 lui a5,0x10000
56 0000000c: 04078793 addi a5,a5,64 # 10000040 <_alt_mem_Onchip_memory+0x7000040>
57 00000010: 10000007 lui a7,0x10000
58 00000014: 05008893 addi a7,a7,80 # 10000050 <_alt_mem_Onchip_memory+0x7000050>
59 00000018: 00000997 auipc s3,0x0
60 0000001c: 09c09993 addi s3,s3,156 # 80000064 <_tdata_end>
61 00000020: 0009a303 lw t1,0(s3)
62
63 00000024 <DO_DISPLAY>:
64 00000024: 0007a203 lw tp,0(a5)
65 00000028: 0008a283 lw t0,0(a7)
66 0000002c: 04028663 bgez t0,00000078 <NO_BUTTON>
67 00000030: 00020313 mv t1,tp
68 00000034: 00405333 add a0,zero,tp
69 00000038: 00000593 li a1,8
70 0000003c: 0040004f jal ra,800000a0 <retl>
71 00000040: 00050233 add tp,a0,zero
72 00000044: 00436333 or t1,t1,tp
73 00000048: 00405333 add a0,zero,tp
74 0000004c: 00000593 li a1,8
75 00000050: 0040004f jal ra,800000a0 <retl>
76 00000054: 00050233 add tp,a0,zero
77 00000058: 00436333 or t1,t1,tp
78 0000005c: 00405333 add a0,zero,tp
79 00000060: 00000593 li a1,8
80 00000064: 01c0004f jal ra,800000a0 <retl>
81 00000068: 00050233 add tp,a0,zero
82 0000006c: 00436333 or t1,t1,tp
83
84 00000070 <WAIT>:
85 00000070: 0008a283 lw t0,0(a7)
86 00000074: fe029ee3 bnez t0,80000070 <WAIT>
87
88 00000078 <NO_BUTTON>:
89 00000078: 00682023 sw t1,0(a6)
90 0000007c: 00000533 add a0,zero,t1
91 00000080: 00100593 li a1,1
92 00000084: 01c0004f jal ra,800000a0 <retl>
93 00000088: 00050333 add t1,a0,zero
94 0000008c: 00025307 lui t2,0x25
95 00000090: 9f038393 addi t2,t2,-1552 # 249f0 <_start-0x7fdb610>

```

Figure 4: Content of the disassembled file called: `lab1_part1.elf.objdump`.

Now, it is needed to download the soft SoC system associated with this program onto the DE0-Nano board. Make sure that the power to the DE0-Nano board is turned on.

- Execute the following command in the Nios V Command Shell window to test if the USB connection is established between the host computer and DE0-Nano board.

```
$ jtagconfig.exe
```

The following message must appear in the Nios V Command Shell window. In the case the message does not show, repeat again the command.

Output message

```
1) USB-Blaster [USB-0]
020F30DD 10CL025(Y|Z)/EP3C25/EP4CE22
```

- Execute the following command in the Nios V Command Shell window for programming the FPGA circuit that is integrated in the DE0-Nano board using the `.sof` configuration file.

```
$ quartus-pgm.exe -c 1 -m JTAG -o "p;DE0-Nano-Basic-Computer_22jul24.sof@01"
```

Note the change in state of the blue LEDs on the DE0-Nano board that correspond to info messages *LOAD* and *GOOD*. These LEDs will blink as the `.sof` file is being downloaded into the FPGA. Figure 5 shows the messages displayed on the screen.

```

C:\Users\DE054TOP-9281F1H>mnt/c/altera/12.1sp1/University_Program/NiosII_Computer_Systems/DE0-Nano/DE0-Nano_Basic_Computer
er_NiosVm/verilog/software/niosv/ACpracticainiosv/lab1_bin$ quartus_pgm.exe -c 1 -m JTAG -o "p;../../../../DE0-Nano_Basi
c_Computer.sof@1"
Info: ****
Info: Running Quartus Prime Programmer
Info: Version 23.1std.0 Build 991 11/28/2023 SC Standard Edition
Info: Copyright (C) 2023 Intel Corporation. All rights reserved.
Info: Your use of Intel Corporation's design tools, logic functions
Info: and other software and tools, and any partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Intel Program License
Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
Info: the Intel FPGA IP License Agreement, or other applicable license
Info: agreement, including, without limitation, that your use is for
Info: the sole purpose of programming logic devices manufactured by
Info: Intel and sold by Intel or its authorized distributors. Please
Info: refer to the applicable agreement for further details, at
Info: https://fpgasoftware.intel.com/eula.
Info: Processing started: Mon Oct 28 11:06:19 2024
Info: Command: quartus_pgm -c 1 -m JTAG -o p;../../../../DE0-Nano_Basic_Computer.sof@1
Info (213045): Using programming cable "USB-Blaster [USB-0]"
Info (213011): Using programming file ../../../../../../DE0-Nano_Basic_Computer.sof with checksum 0x005DE1F1 for device EP4C22
F17@1
Info (209060): Started Programmer operation at Mon Oct 28 11:06:20 2024
Info (209016): Configuring device index 1
Info (209017): Device 1 contains JTAG ID code 0x020F30D0
Info (209007): Configuration succeeded -- 1 device(s) configured
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Mon Oct 28 11:06:22 2024
Info: Quartus Prime Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 4446 megabytes
Info: Processing ended: Mon Oct 28 11:06:22 2024
Info: Elapsed time: 00:00:03
Info: Total CPU time (on all processors): 00:00:00
C:\Users\DE054TOP-9281F1H>mnt/c/altera/12.1sp1/University_Program/NiosII_Computer_Systems/DE0-Nano/DE0-Nano_Basic_Computer

```

Figure 5: Messages displayed on the screen after configuring the FPGA circuit integrated into the DE0-Nano board with the SoC configuration called *DE0-Nano Basic Computer*.

14. Having downloaded the `sof` configuration called *DE0-Nano Basic Computer* into the FPGA chip on the DE0-Nano board, we can now load and run programs on this SoC computer. In the Nios V Command Shell window, execute the following command for downloading the `.elf` program into the main memory of the soft computer.

```
$ niosv-download.exe -g lab1_part1.elf
```

This command also run the `.elf` program.

15. Observe the LEDs located on the board are turning on and off quickly (see Figure 6). This test provides an indication that the DE0-Nano board is functioning properly. Stop the execution of the sample program by typing "CTRL+c" in the Command Shell window.



Figure 6: LEDs on the board are turning on and off after downloading and executing the `lab1_part1.elf` program.

Part II. Designing a simple program

Now, we will explore some features of the programming framework for Nios V by using a simple application program written in the RISC-V assembly language. Consider the program in Figure 7, which finds the

largest number in a list of 32-bit integers that is stored in the memory. This program is available in the file `lab1_part2.s`.

Note that some sample data is included in this program. The data section of program starts at hex address `0x08000038`, as specified by the `.data` assembler directive and shown in `lab1_part2.elf.objdump` file. The first word (4 bytes) is reserved for storing the result, which will be the largest number found. The next word specifies the number of entries in the list. The words that follow give the actual numbers in the list.

Make sure that you understand the program in Figure 7 and the meaning of each instruction in it. Note the extensive use of comments in the program. You should always include meaningful comments in programs that you will write!

Perform the following steps for compiling and executing the program:

1. Create a new directory; we have chosen the directory named `lab1_part2`. Copy the file `lab1_part2.s` into this directory.
2. Now, follows the same steps done in Part I for assembling with `riscv32-unknown-elf-as.exe` file, linking with `riscv32-unknown-elf-ld.exe`, and report with `niosv-stack-report.exe` and `riscv32-unknown-elf-objdump.exe`.
3. Then, configure the DE0-Nano board using the `quartus_pgm.exe` command and `DE0_Nano_Basic_Computer_22jul24.s` file and download the `.elf` program using `niosv-download`.

The next steps will use the GNU Debugger (GDB) for RISC-V processors. Open three Nios V Command Shell terminals.

Terminal-1 opens the Open On-Chip Debugger (OpenOCD). OpenOCD is part of the Nios V Command Shell tool chain and provides on-chip programming and debugging support with a layered architecture of JTAG interface.

Terminal-1: OpenOCD

```
$ sh
$ openocd-cfg-gen ./niosv.cfg
$ openocd -f ./niosv.cfg
```

The second terminal is used as above in Part I for compiling, linking and configuring the FPGA device. In this section of the assignment, we have prepared a `Makefile` file to automatize these steps. The options for the `Makefile` can be viewed using: `make -help`.

Terminal-2: Compile, link and configure

```
$ cd lab1_part2
$ sh
# compiling and link
$ make
# configuring the FPGA
$ make configure
```

OpenOCD complies with the remote gdbserver protocol and, as such, can be used to debug remote targets. GDB works with OpenOCD. Terminal-3 opens the GDB tool that is part of the Nios V Command Shell tool chain. GDB uses several commands to interact with the Nios V architecture.

```
lab1_part2.s

.text /* executable code follows */

.global _start
_start:

/* initialize base addresses of parallel ports */
la x15, RESULT /* x15: point to the start of data section */
lw x16, 4(x15) /* x16: counter, initialized with n */
addi x17, x16, 8 /* x17: point to the first number */
lw x18, (x17) /* x18: largest number found */

LOOP:
addi x16, x16, -1 /* Decrement the counter */
beq x16, zero, DONE /* Finished if r5 is equal to 0 */
addi x17, x17, 4 /* Increment the list pointer */
lw x19, (x17) /* Get the next number */
bge x18, x19, LOOP /* Check if larger number found */
add x18, x19, zero /* Update the largest number found */
j LOOP

DONE:
sw x18, (x15) /* Store the largest number into RESULT */

STOP:
j STOP /* Remain here if done */

.data /* software variables follow */

RESULT:
.skip 4 /* Space for the largest number found */

N:
.word 7 /* Number of entries in the list */

NUMBERS:
.word 4, 5, 3, 6, 1, 8, 2 /* Numbers in the list */

.end
```

Figure 7: Example of RISC-V program for the Nios V/m soft processor.

Terminal-3: GDB debugger

```
$ cd lab1_part2
$ sh
$ riscv32-unknown-elf-gdb
(gdb) target extended-remote localhost:3333
(gdb) file lab1_part2.elf
(gdb) load
(gdb) info registers
```

In Terminal-3, read the memory address 0x08000038 using the following command:

Terminal-3: GDB debugger

```
(gdb) x 0x08000038
```

The data value shown on Terminal-2 should be the maximum of the list of numbers indicated in the `.data` section of the source code (see Figure 7).

Now, run and stop the program at the last branch instruction which is loaded in the memory location 0x8000034. To do this, a *breakpoint* is inserted as indicated in the following box. Finally, the value of the PC register is read.

Terminal-3: GDB debugger

```
(gdb) b *0x8000034
(gdb) continue
(gdb) info registers
```

Question 1.

Examine the disassembled code of the `lab1_part2.elf` file (see `lab1_part2.elf.objdump` file). Note the difference in comparison with the original source code. Make sure that you understand the meaning of each instruction. Observe also that your program was loaded into memory locations with the starting address 0x08000000. These addresses correspond to the on-chip SRAM memory, which was selected when specifying the system parameters.

Note that the pseudoinstruction `la x15, RESULT` in the original source code has been replaced with two machine instructions, `auipc a5,0x0` and `addi a5,a5,56`, which load the 32-bit address `RESULT` into register `a5` in two parts. `auipc a5,0x0` initializes the `a5` register to the current value of the PC register: 0x08000000. `addi a5,a5,56` adds 56 = 0x38 to the `a5` register. The register `x5` is named `a5`.

- Examine the disassembled code to see the difference in comparison with the original source program. Make sure that you understand the meaning of each instruction.

This time add a breakpoint at address 0x8000024, so that the program will automatically stop executing whenever the `bge` branch instruction at this location is about to be executed. Run the program and observe the contents of registers `s2` and `s3` each time this breakpoint is reached.

Terminal-3: GDB debugger

```
(gdb) b *0x8000024
(gdb) continue
(gdb) info registers
```

Return to the beginning of the program by setting the Program Counter to 0. Now, single step through the program. Watch how the instructions change the data in the processor's registers.

Terminal-3: GDB debugger

```
(gdb) b *0x8000000  
(gdb) j *0x8000000  
(gdb) stepi  
(gdb) info registers
```

Remove the breakpoint. Then, set the Program Counter to 0x8000008, which will bypass the first two instructions which load the address RESULT into register a5. Also, set the value in register a5 to 0x8000004. Run the program.

Terminal-3: GDB debugger

```
(gdb) j *0x8000008  
(gdb) continue  
(gdb) info registers
```

Question 2.

- What will be the result of this execution?

References

- [1] Terasic. DE0-Nano User Manual, 2013.
- [2] Intel. Nios V Embedded Processor Design Handbook, 2023.
- [3] Intel. Nios V Processor Software Developer Handbook, 2023.