



## **Lab Assignment 3:**

# **Performance evaluation of pipelined processors**

Computer Architecture (40969)  
Computer Science School (EII)  
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# Main goals of lab 3

- Performance evaluation of the Nios V/g pipelined processor and comparison with the Nios V/m pipelined processor: CPI, operations/sec.
- Analyze the effect on Nios V/g performance of the machine instruction reordering software technique.
- Propose the realization of a theoretical exercise in which a possible change in the Nios V/g microarchitecture is evaluated.

# Scheduling: 4 weeks

- S1: Section 1; 2 hours
- S2: Section 2; 2 hours
- S3: Sections 3 y 4; 2 hours
- S4: Test; 1,5 hours