PROJECT

ON

IMPLEMENTATION AND PERFORMANCE EVALUATION OF 32x32 BIT MULTIPLIER ON FPGA

submitted in partial fulfillment of the requirement

For the degree of

BACHELOR OF TECHNOLOGY IN

ELECTRONICS AND COMMUNICATION ENGINEERING

UNDER THE SUPERVISION OF

Dr. Mansi Jhamb

USICT

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Certificate

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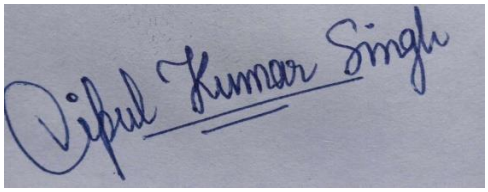

Date: 16 September,2022
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Improvements suggested to the candidate.

Mansi Jhamb/16-09-22

Chapter 1

Introduction

In this world , starting from smallest to biggest machinery i.e nano chipset to motherboards are being controlled by microcontrollers , DSP's and FPGA and their combinations as SoCs provide solution for embedded system and This is all possible through the VLSI .

Now a days , we are deeply connected to VLSI directly or indirectly through daily essential gadgets like smartphone , television , etc. In VLSI , FPGA's are basically used more because they are power efficient and gather millions of integrated circuits on single chip. And

VHDL is one of the Very High Speed integrated circuit (VHSIC) hardware description language used for the development and running FPGA's . It is used majority of tech companies like Google , Apple , Microsoft , Intel etc for the various purposes like intensive computing . to run servers across the world . These tech Giant's also works on to make FPGA's to make power efficient as the servers needs more power and resources to manage the internet and let them keep running .

These FPGA's are the future of IT sector and Fast running digital world to automate the things across the globe to reduce human efforts .FPGA's are used almost everywhere around us .

Fig 1. FPGA

FPGA Uses and Applications

We cannot limit the applications of FPGA's with finite examples , they have very vast application starting from embedded system to super computers . It's become the part of human life to reduce efforts and being with us till the existence of human on earth.

- They are used in **DEFENCE FIELD** for the aircrafts , drone and missiles for the fast and efficient performance and precise calculations. These FPGA's are intelligent too like
  They are used in radars to determine the friend and foe ships and aircrafts.

- They are used in **AEROSPACE INDUSTRY** as they need more calculations and other electronics components. They are used in rockets and aircrafts for calculating the perfect trajectory for the safe and secure travel .

- They are used in **DATA CENTRES** , **COMPUTER MANUFACTURING** and Even in **SUPERCOMPUTERS** as they requires powerful GPU's and motherboard for their best or higher performance and supercomputer are much faster so they need faster and power efficient FPGA's for the predictions , research and intense mathematics calculations .

- They are used in Medical field for the precise surgeries like removal of tumour etc or the place where least human efforts are required with more accuracy . They are used in detecting and diagnoses of diseases , etc .

Chapter 2

Various Types of FPGA's

FPGAs (field programmable gate arrays) are a flexible type of semiconductor chip architecture that have the capability to change their structure and design according to the needs.

There are different types of FPGA's are available in market according to their requirement and their performance , size and efficiency which matters a lot . some of them are as powerful that they are used in cloud computing and servers like AWS (amazon web services) , Google and Microsoft cloud Computing engines as their back bone because they need to work restlessly at their peak performance like intel Stratix® series , AMD EPYC series FPGA's.

And some of FPGA's are small in size and more efficient and works on few volts for their working and these FPGA's are mostly used in mobile phones , android phones , etc and in embedded systems .

But they all support the feature of reprogrammability and this feature make them more useful and help in reduce e waste . This feature of reprogrammibilty make FPGA's have more use cases .These days larger sized but least or low power FPFGA's are more popular as they have more use case in IOT and Computer Vision and more in AI based applications .

From consumer point of view , FPGA's have different applications like in music player low power FPGA's are used in combination with python on software based algorithms and some other applications are in drone and home security .

Some of these FPGA's are **VIRTEX 6 , VIRTEX 6 LP (LOWER POWER) AND VIRTEX 7** , etc . Like these, there are much more number's of FPGA's are available and they all serves the multiple purposes according to their specifications.

Fig 2. Virtex 6 FPGA

Virtex®-6 FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins, It contain many built-in system-level blocks. These features allow logic designers to build the highest levels of performance and functionality into their FPGA based systems. It offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, connectivity, and soft microprocessor capabilities.

The **Virtex-6 family** is based on a 40 nm process technology for compute-intensive electronic systems, and the company claims it consumes 15 percent less power and has 15 percent improved performance over competing 40 nm FPGAs

Fig 3. Virtex 7 FPGA

Virtex®-7 FPGAs are optimized for system performance and integration at 28nm and bring best-in-class performance/watt fabric, DSP performance, and I/O bandwidth to your designs. The family is used in an array of applications such as 10G to 100G networking, portable radar, and ASIC Prototyping.

The **Virtex-7** family is based on a 28 nm process technology, and is reported to deliver a two-fold system performance improvement at 50 percent lower power compared to previous generation Virtex-6 devices. In addition,

Chapter 3

IMPLEMENTATION

The multiplier operation is carried in XILINX based on DSP and Slicing Technique .

A binary multiplier is a combinational logic circuit used for multiplying two binary numbers. The two numbers are more specifically known as multiplicand and multiplier and the result is known as a product of that multiplier

The multiplicand & multiplier might be of different bit size means that input A and input B may have different size of input bit. The product have bits depends on the bit size of the multiplicand & multiplier. The bit size of the product is equal to the sum of the bit size of multiplier & multiplicand means bit size of input A and bit size of input B.

Like Input A is of 6 bits and Input B is of 7 bits then , the output C is of bit size = 6 bits + 7bits = 13 bits

In this , we have made 32 X 32 Bit multiplier , which takes two input's of 32 bits , compute and display the output of 62 bits (32 bits + 32 bits) . This multiplication is done with the help of predefined Xilinx operator (*) which takes two inputs operand of signed or unsigned type and compute according .

3.1 Basic's of Binary Calculation

It is as simple as general multiplication and perform exactly same like 0 X 1 = 0 . etc

Input 1 (A)	Input 2 (B)	Output
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

Truth Table for a bit multiplication

This is how multiplication is done in computer (Bit Wise) and truth table for multiplication is provided above . From the table it is noticed that its truth table is similar to AND gate truth table . Simply we can say multiplication of 2 bits is comparatively similar AND operation for these 2 bits .

3.2 VHDL Source Code

```
library IEEE;


use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

use IEEE.NUMERIC_STD.ALL;


entity Multiplier32x32 is

generic (no_of_bits : Natural:= 32);

Port ( InputA : in STD_LOGIC_VECTOR (no_of_bits-1 DOWNTO 0);

       InputB : in STD_LOGIC_VECTOR (no_of_bits-1 DOWNTO 0);

       OutputC : out STD_LOGIC_VECTOR (2*no_of_bits-1 DOWNTO
0));

end Multiplier32X32;

architecture Behavioral of Multiplier32x32 is

signal MUL : STD_LOGIC_VECTOR (2*no_of_bits-1 DOWNTO 0);

begin

P1: process (InputA,InputB)

begin

 MUL <= STD_LOGIC_VECTOR ( InputA * InputB ) ; --
multiplication of two inputs (Input A and Input B) and
stores them in mul

end process P1;

outputC <= MUL ;

end Behavioral;
```

3.3 Schematics

For each and every VHDL FPGA projects , we basically have in two types of schematics

1. RTL Schematics .

It is based on resistor transistor level , this is created after the HDL synthesis phase of the synthesis process (which include some a processes like building maps , translate etc).

It is independent of the targeted devices I which it is used and is pre optimised design of the generic symbols . They have same name as of entity in vhdl , it contains input and output ports.

2. Technology Schematics .

This schematic is being generated after the optimization and technology targeting phase of the synthesis process. And it is more technical then the RTL schematic and they are based on the targeted devices and contains logical elements like LUT's (loop up table's) , input /output buffers and some other logical components of digital electronics like mux , etc Viewing this schematic allows you to see a technology-level representation of your HDL optimized for a specific Xilinx architecture .

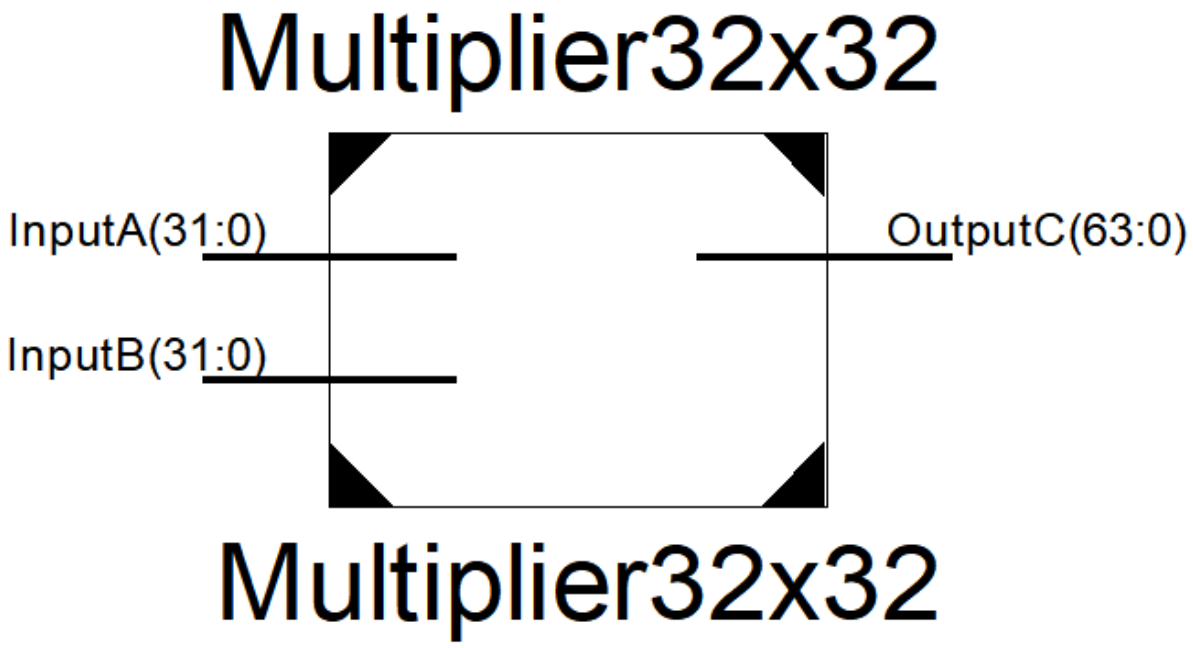

Fig 4. Outer RTL Schematic

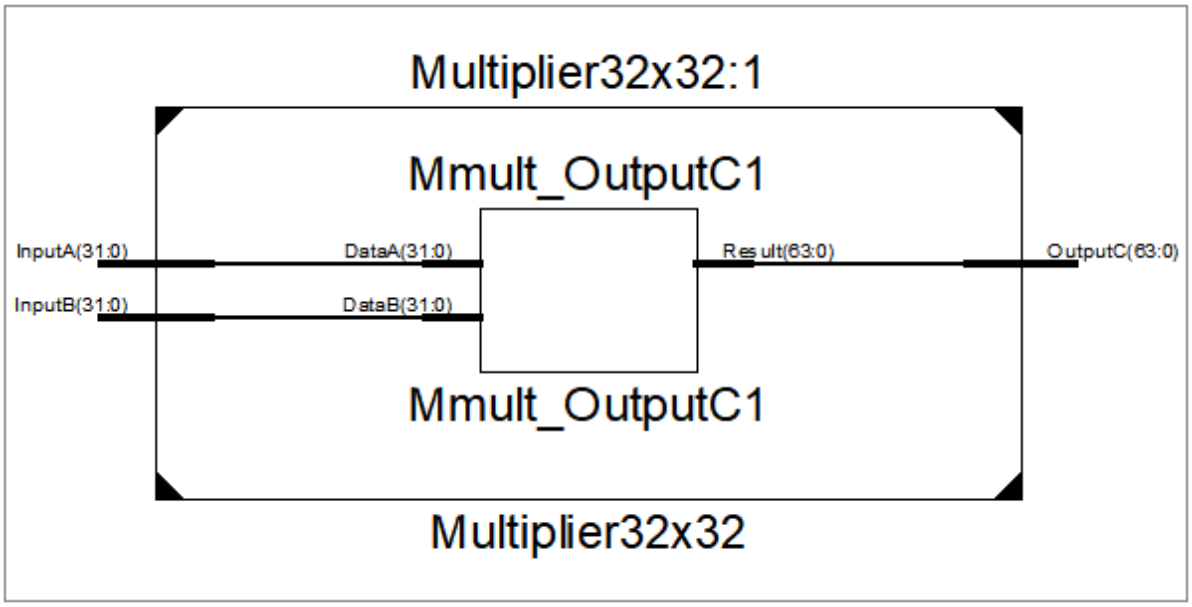

Fig 5. Inner RTL Schematic

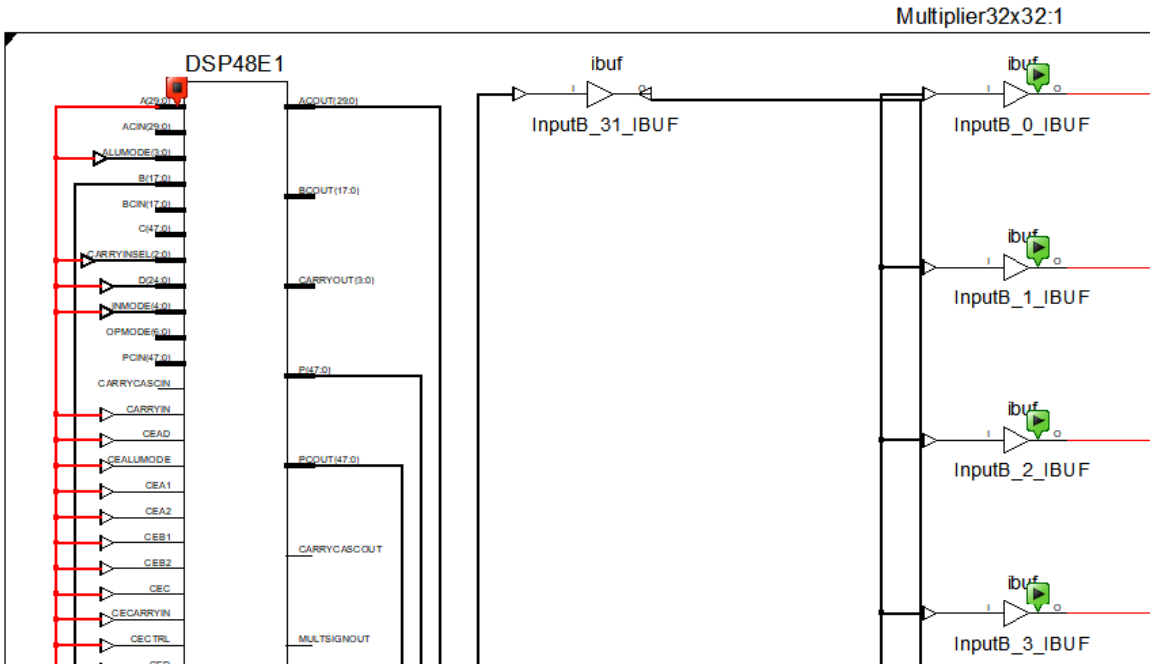

Fig 6. Technology Schematic

(Note : This is not complete screenshot of whole technology schematics)

3.4 Output Waveform

This represents the output in the form of wave , it is generated in VHDL by simulator called ISim . This waveforms helps in the study and analysis of different functions performed . Signal in VHDL store group of value using the concept of array , means it might store more than one value . All the signals process starts from the driver signal which holds its present and all its future values in a particular sequence

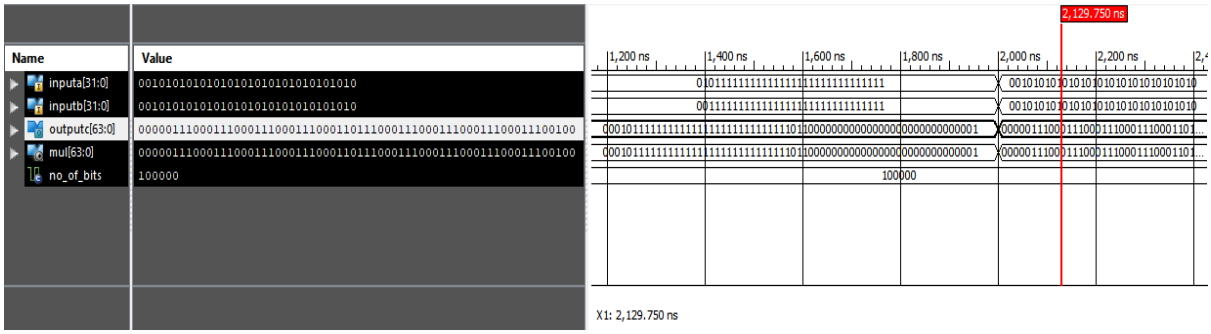

Fig 7. Representing Waveform

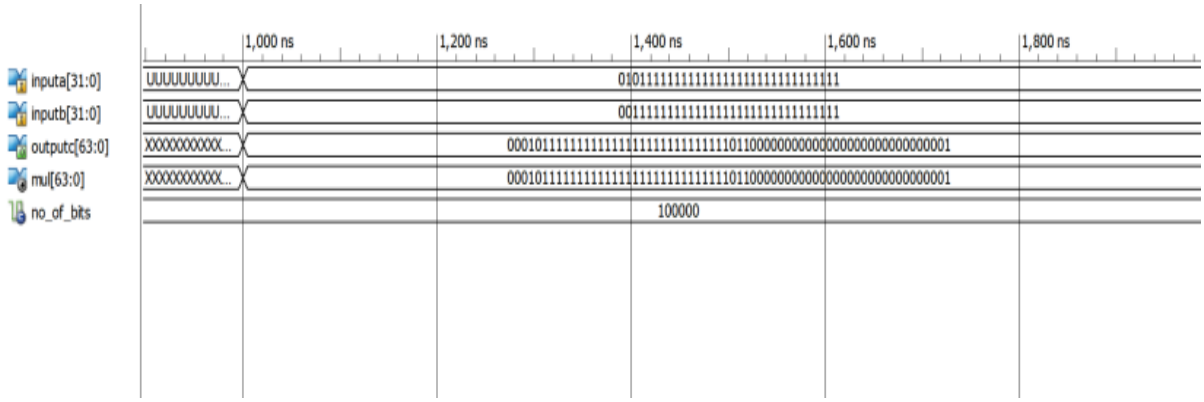

Fig 8. Representing values of A , B and OUTPUT

Chapter 4

Results

This includes all the factors that affects the performance of the virtex's like Quiescent Current , Thermal temperature , Voltage , efficiency , etc.

4.1 For Virtex 6

Device utilization Summary

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	0	93,120	0%
Number of Slice LUTs	0	46,560	0%
Number of occupied Slices	0	11,640	0%
Number of LUT Flip Flop pairs used	0		
Number of bonded IOBs	128	240	53%
Number of RAMB36E1/FIFO36E1s	0	156	0%
Number of RAMB18E1/FIFO18E1s	0	312	0%
Number of BUFG/BUFGCTRLs	0	32	0%
Number of ILOGICE1/ISERDESE1s	0	360	0%
Number of OLOGICE1/OSERDESE1s	0	360	0%
Number of BSCANs	0	4	0%
Number of BUFHCEs	0	72	0%
Number of BUFIODQSs	0	36	0%
Number of BUFRs	0	18	0%
Number of CAPTUREs	0	1	0%
Number of DSP48E1s	4	288	1%
Number of EFUSE_USRs	0	1	0%
Number of FRAME_ECCs	0	1	0%
Number of GTXE1s	0	8	0%
Number of IBUFDS_GTXE1s	0	6	0%
Number of ICAPs	0	2	0%

Number of IDELAYCTRLs	0	9	0%
Number of IODELAYE1s	0	360	0%
Number of MMCM_ADVs	0	6	0%
Number of PCIE_2_0s	0	1	0%
Number of STARTUPs	1	1	100%
Number of SYSMONs	0	1	0%
Number of TEMAC_SINGLEs	0	4	0%
Average Fanout of Non-Clock Nets	1.14		

Power Analyzation

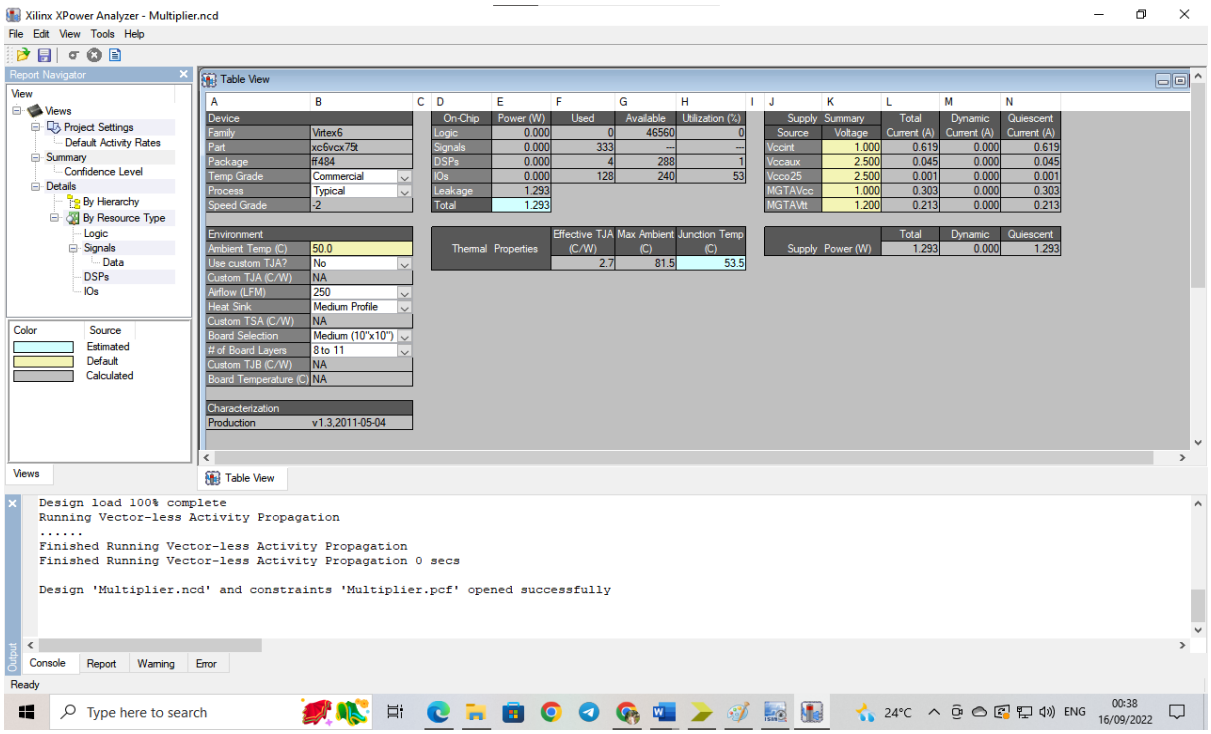

Fig 9. Power Analysis for Virtex 6

4.2 For Virtex 6 Lower Power

Device utilization Summary

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	0	93,120	0%
Number of Slice LUTs	0	46,560	0%
Number of occupied Slices	0	11,640	0%
Number of LUT Flip Flop pairs used	0		
Number of bonded IOBs	128	240	53%
Number of RAMB36E1/FIFO36E1s	0	156	0%
Number of RAMB18E1/FIFO18E1s	0	312	0%
Number of BUFG/BUFGCTRLs	0	32	0%
Number of ILOGICE1/ISERDESE1s	0	360	0%
Number of OLOGICE1/OSERDESE1s	0	360	0%
Number of BSCANs	0	4	0%
Number of BUFHCEs	0	72	0%
Number of BUFIODQSs	0	36	0%
Number of BUFRs	0	18	0%
Number of CAPTUREs	0	1	0%
Number of DSP48E1s	4	288	1%
Number of EFUSE_USRs	0	1	0%
Number of FRAME_ECCs	0	1	0%
Number of GTXE1s	0	8	0%
Number of IBUFDS_GTXE1s	0	6	0%
Number of ICAPs	0	2	0%
Number of IDELAYCTRLs	0	9	0%
Number of IODELAYE1s	0	360	0%
Number of MMCM_ADVs	0	6	0%
Number of PCIE_2_0s	0	1	0%
Number of STARTUPs	1	1	100%
Number of SYSMONs	0	1	0%
Number of TEMAC_SINGLEs	0	4	0%
Average Fanout of Non-Clock Nets	1.14		

Power Analyzation

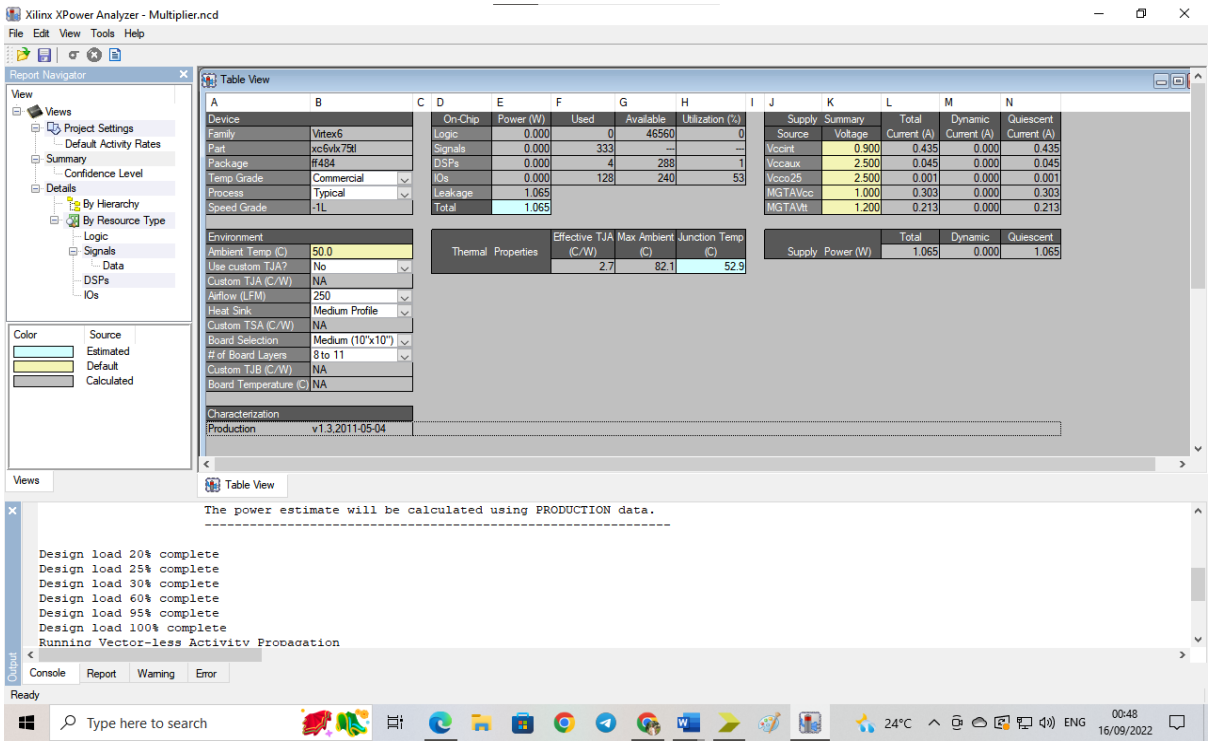

Fig 10. Power Analysis for Virtex 6 LP

4.3 For Virtex 7

Device utilization Summary

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	0	93,120	0%
Number of Slice LUTs	0	46,560	0%
Number of occupied Slices	0	11,640	0%
Number of LUT Flip Flop pairs used	0		
Number of bonded IOBs	128	240	53%
Number of RAMB36E1/FIFO36E1s	0	156	0%
Number of RAMB18E1/FIFO18E1s	0	312	0%
Number of BUFG/BUFGCTRLs	0	32	0%
Number of ILOGICE1/ISERDESE1s	0	360	0%
Number of OLOGICE1/OSERDESE1s	0	360	0%
Number of BSCANs	0	4	0%
Number of BUFHCEs	0	72	0%
Number of BUFIODQSs	0	36	0%
Number of BUFRs	0	18	0%
Number of CAPTUREs	0	1	0%
Number of DSP48E1s	4	288	1%
Number of EFUSE_USRs	0	1	0%
Number of FRAME_ECCs	0	1	0%
Number of GTXE1s	0	8	0%
Number of IBUFDS_GTXE1s	0	6	0%
Number of ICAPs	0	2	0%
Number of IDELAYCTRLs	0	9	0%
Number of IODELAYE1s	0	360	0%
Number of MMCM_ADVs	0	6	0%
Number of PCIE_2_0s	0	1	0%
Number of STARTUPs	1	1	100%
Number of SYSMONs	0	1	0%
Number of TEMAC_SINGLEs	0	4	0%
Average Fanout of Non-Clock Nets	1.14		

Power Analyzation

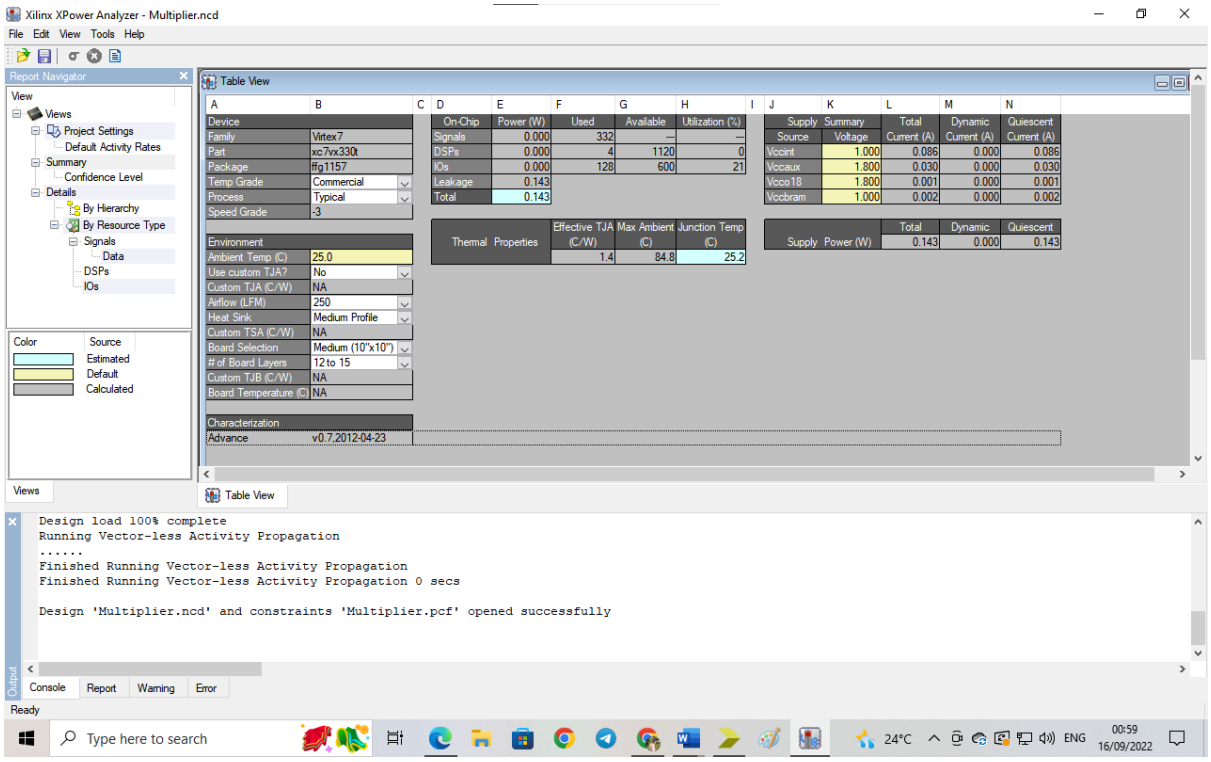

Fig 11. Power Analysis for Virtex 7

Chapter 5

Conclusion

This is done to study the performance of FPGA's based on factors like Quiescent Current , Power , Junction Temperature , etc. This is comparison between different virtex's like viretx 6 , virtex6 LP , virtex 7 .

Factors	**Vertex 6**	**Vertex 6 LP**	**Vertex 7**
Quiescent Current (A)	1.293	1.065	0.143
Power (W)	1.293	1.065	0.143
Junction Temperature (C)	53.5	52.9	25.2

Comparison Table for different FPGA's Model for performance and efficiency.

We are Planning to publish these results...