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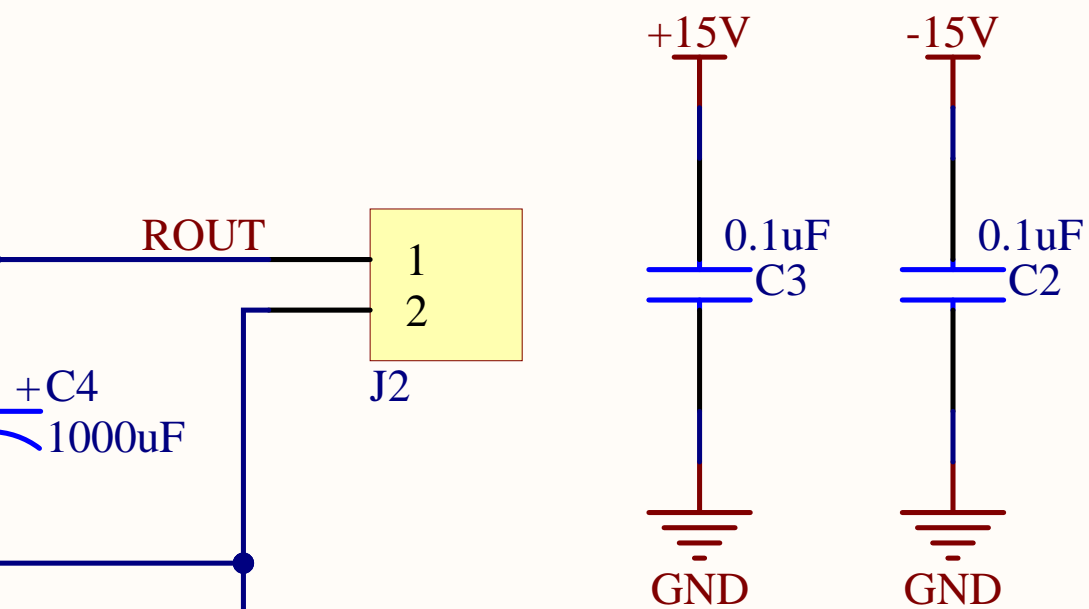
Phase_Detection_Rev1

The diagram illustrates a phase detection circuit, labeled "Phase_Detection_Rev1". It features three identical signal processing channels for PHASE_RY, PHASE_BY, and PHASE_BR. Each channel consists of a transformer (Header 5X2A) connected to a 3.3V supply (PH_R, PH_Y, PH_B). The signals are processed by an LM1224 op-amp configured as a comparator. The op-amp's non-inverting input (IN+) is connected to the signal input through a 1k resistor (R1, R5, R9). The inverting input (IN-) is connected to a 3.3V supply through a 1k resistor (R2, R6, R10). The op-amp's output (OUT) is connected to a 3.3V supply through a 1k resistor (R3, R7, R11). The op-amp's ground (GND) is connected to a 3.3V supply through a 1k resistor (R4, R8, R12). The op-amp's output (OUT) is connected to a 3.3V supply through a 1k resistor (R3, R7, R11). The op-amp's ground (GND) is connected to a 3.3V supply through a 1k resistor (R4, R8, R12). The op-amp's output (OUT) is connected to a 3.3V supply through a 1k resistor (R3, R7, R11). The op-amp's ground (GND) is connected to a 3.3V supply through a 1k resistor (R4, R8, R12).

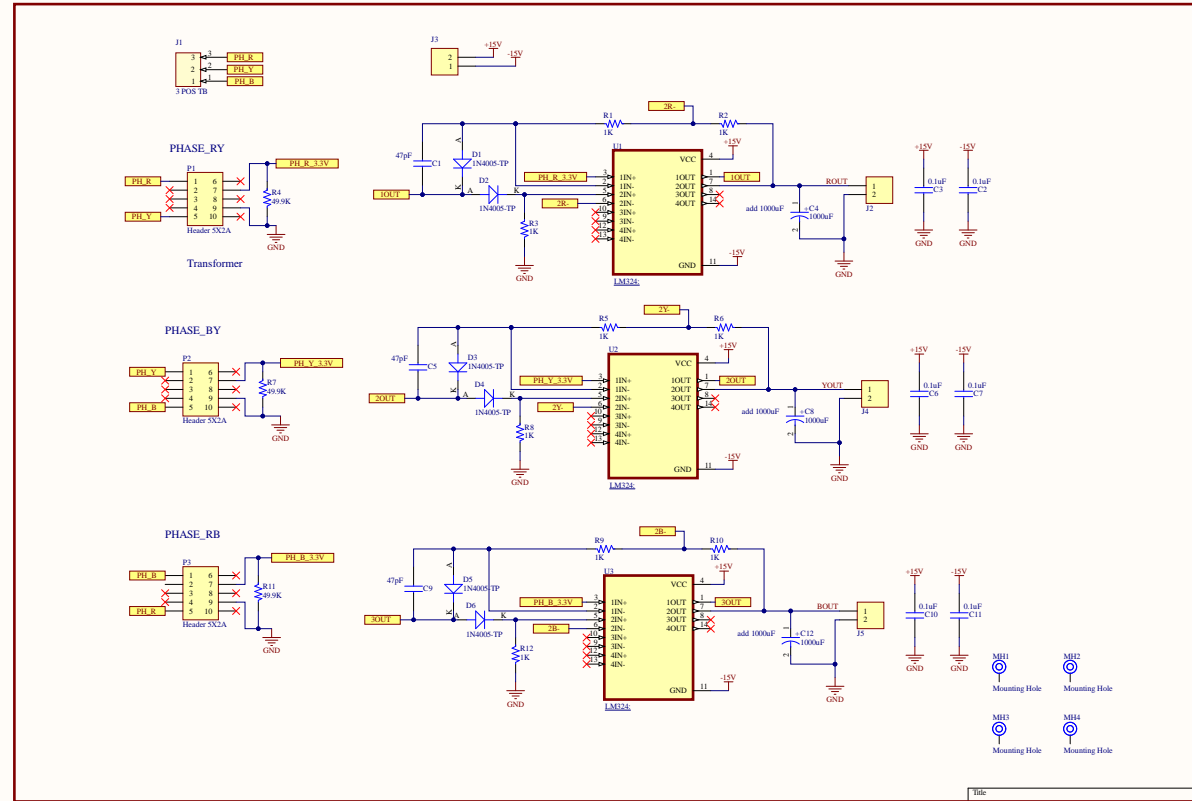
Variant : Testing_Purpose

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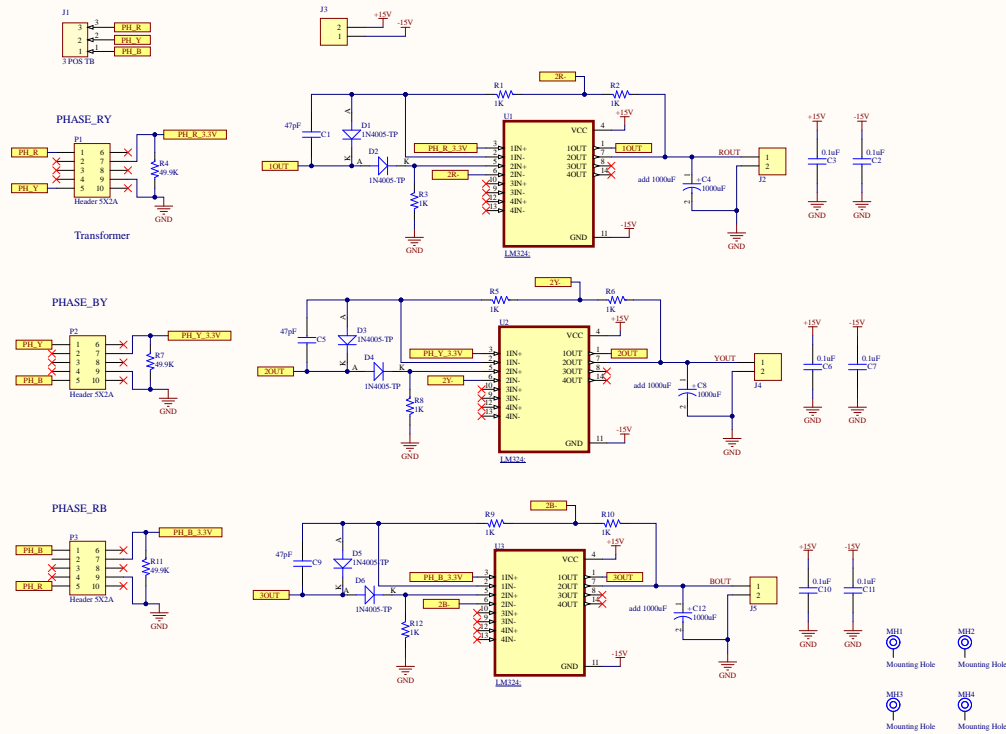
Phase_Detection_Rev1



Variant : Testing Purpose

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Phase_Detection_Rev1



Variant : Testing_Purpose

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