Rubric for DVD Mid Semester Exam(ECE314/ECE514) 2024

Name: Roll number: Date:08-10-2024

Instructions:

1. **This question paper is of 30 marks in total.**
2. **Students registered for the ECE314 course are required to attempt questions amounting to 25 marks. Any additional questions attempted beyond 25 marks will be treated as bonus.**
3. **Students registered for the ECE514 course must attempt the entire paper of 30 marks.**

1. Answer the following questions: **[6 marks]**
   a. During fabrication, both high K and low K dielectric oxides are used. Where is it desired to use which dielectric and why? [CO1] **[2 marks]**

      Sol: As the technology scales, oxide thickness also reduces due to which there is an increase in gate leakage through tunneling. To prevent tunneling gate oxide is made thick but this leads to loss in gate control. So, we use high-k dielectrics like HfO2 to make gate oxides so that we can make thicker dielectrics to reduce gate leakage while retaining a good control over the gate region. [1 marks]
      During BEOL fabrication processes, while making interconnects, we use low-k dielectric oxides so that inter-metal and intra-metal capacitances can be reduced. These capacitance strongly impact the power and performance of the circuit and need to be minimized. [1 marks]

   b. A mobile processor core is to be designed. Battery life is a key concern. So the dynamic power has to be kept low, but users also demand high performance for gaming and video streaming. How would you balance these two conflicting priorities? [CO3] **[1 mark]**

      Sol: Dynamic Voltage and Frequency Scaling (DVFS) allows the processor to dynamically adjust both the voltage and frequency based on the current workload and performance requirements. This allows the processor to run efficiently under varying conditions:

Low Workload/Idle Scenarios (Battery Saving Mode): When the phone is performing light tasks such as checking emails, messaging, or standby mode, the processor can operate at a lower frequency and voltage. This reduces power consumption and extends battery life because the full performance capacity isn't required.

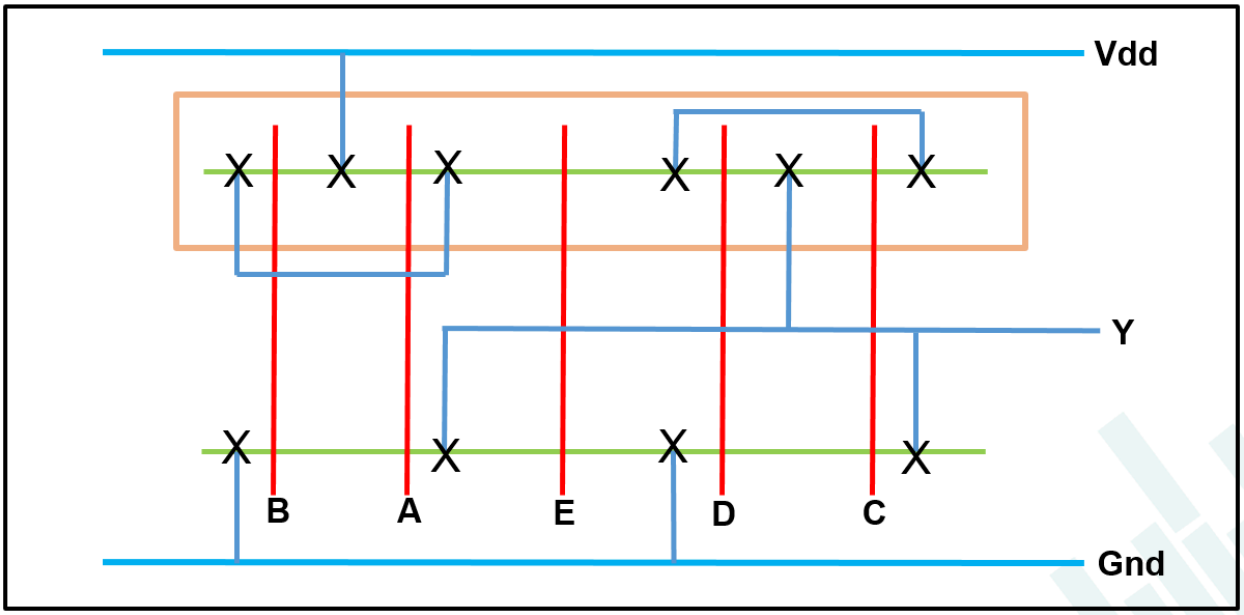
High Workload Scenarios (Performance Mode): When running demanding applications like **gaming** or **video streaming**, DVFS can increase the voltage and frequency to ensure that the processor delivers the high performance required. Although this consumes more power, DVFS ensures that the processor is only operating at high power during critical periods, thereby minimizing unnecessary battery drain.

c. What is done to prevent latch-up? [CO1] **[1 mark]**

Sol: Substrate Contacts (NTAP,PTAP) are provided at regular intervals to reduce substrate resistance and prevent formation of back to back parasitic BJT latch.

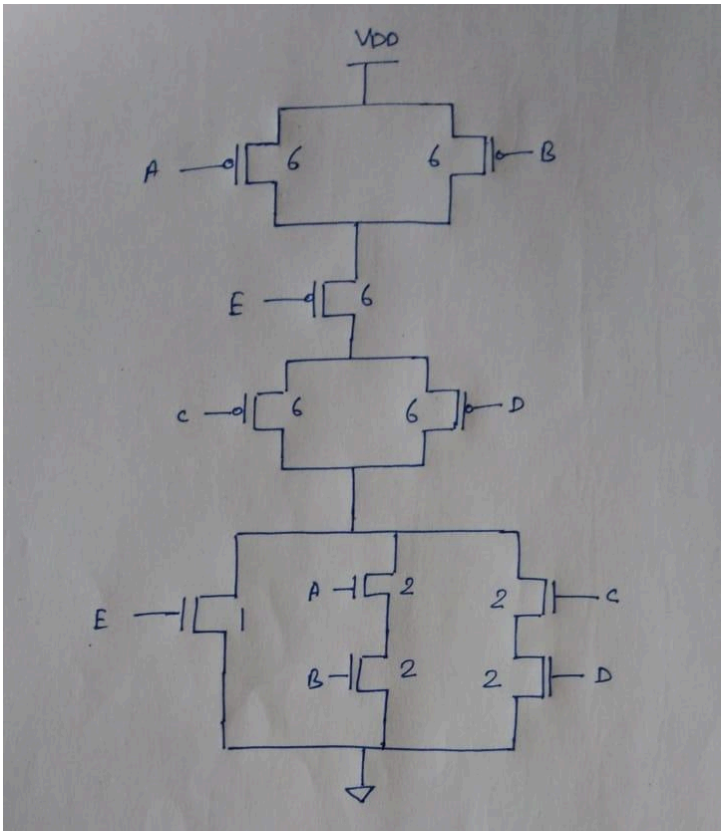
d. In dynamic voltage frequency scaling, for operating in high performance, do we first increase the voltage and then increase the frequency or we first increase the frequency and then increase the voltage ? Support your answer with reasoning. [CO3] **[2 marks]**
Sol: In DVFS, if we increase the supply voltage first then the delay of logic gates will decrease and then if we increase the frequency, it will not lead to any timing failures. [1 marks : correct statement + 1 mark : correct reason]

2. In the below figure, given is a stick diagram of a complex logic gate. Answer the following questions with respect to this stick diagram. **[8 marks]**



a. Write the boolean expression for this stick diagram. **[1 mark]**
Sol: ~(AB+CD+E)

b. Draw CMOS schematic for the above derived boolean expression and size the transistors with respect to unit inverter. **[2 marks]**
Sol: [1 mark : Schematic + 1 mark : Sizing]



c. Strength of this complex logic gate is increased to 3 times the strength of the unit inverter. What will be the logical effort with respect to input B and input E. **[1 mark]**

Sol: Logical Effort is independent of drive strength. Logical effort of B = 8/3 and logical effort at E = 7/3

d. Based on the schematic drawn in part b, what will be the input stimuli to calculate rise and fall propagation and contamination delay ? Clearly state any assumptions. **[4 marks]**

1 mark for each stimulus (if transitions are shown) and 0.5 marks if only the final input pattern is written.

Sol: For rise propagation delay
B = 1, D = 1, E = 0, C = 0, A = 1 -> 0
or
A=1, D = 1, E = 0, C = 0, B = 1 -> 0
or
A=1, C = 1, D = 0, E = 0, B = 1 -> 0

For fall propagation delay
E = C = D = 0, A = 1, B = 0 -> 1
or
E = A = B = 0, C = 1, D = 0 -> 1
or
C = 1, D = E = 0, A = 1, B = 0 -> 1

For rise contamination delay
E = A = B = 0, C,D = 1 -> 0

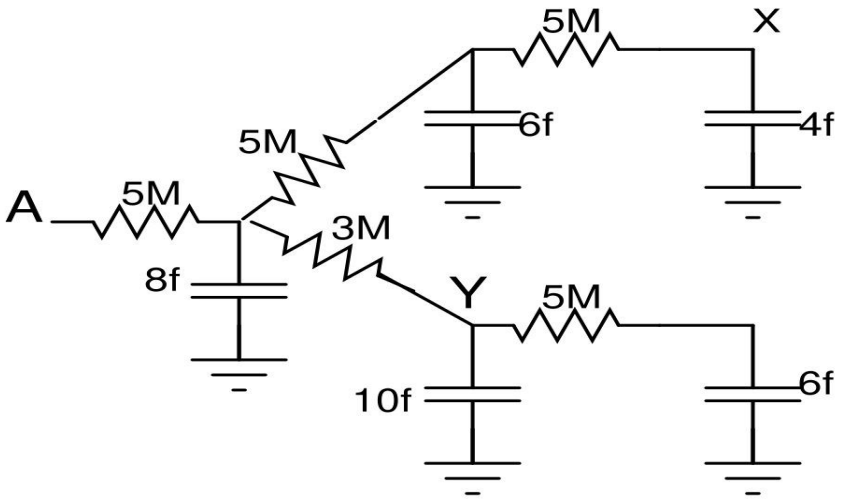
For fall contamination delay
B = D = 1, A,C,E = 0 -> 1

3. For a CMOS process which of the following might be less than target, more than target or remains at target in different process lots: [CO2] **[3 marks]**
Sol:

Corner/Parameter	tox	Width	Length
FF	LESS	MORE	LESS
SS	MORE	LESS	MORE
TT	ON	ON	ON

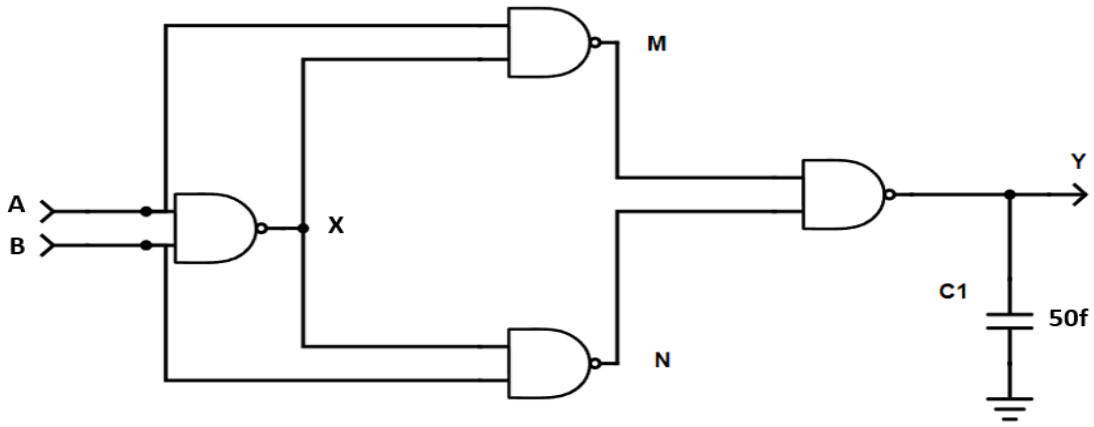
**1 mark for each correct row, no other partial marks.

4. Calculate the Elmore Delay with respect to point A in the given circuit for:
   (i) Point X **(2 marks)**
   (ii) Point Y **(2 marks)** **[CO1,CO2]**



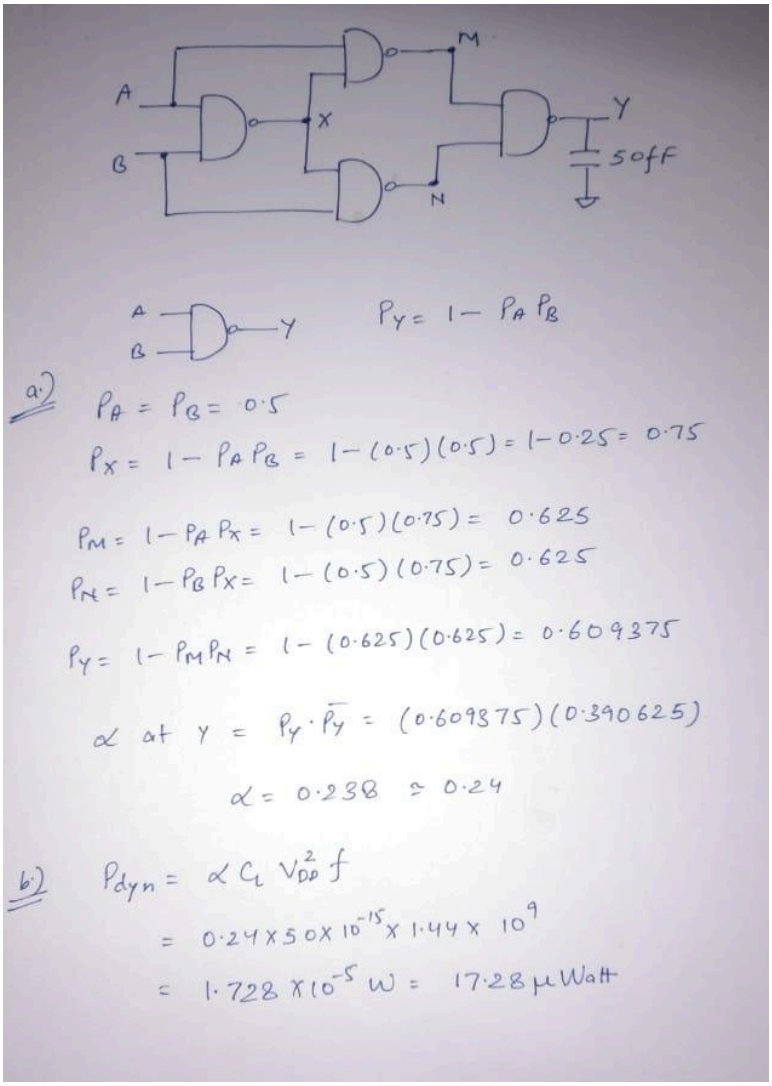
Sol: (i) 8f(5M) + 6f(5M + 5M) + 4f(5M + 5M + 5M) + 10f(5M) + 6f(5M) = 240ns
(ii) 8f(5M) + 10f(5M+ 3M)+ 6f(5M+3M) + 6f(5M) + 4f(5M) = 218ns (0.5 marks deducted if units are wrong for each part)

5. Given below is a NAND gate implementation of XOR gate. Answer the following questions. [CO3] **[4 marks]**



a. Given that occurrence of logic 0 and logic 1 at input A and B is equiprobable, then what is the activity factor at 'Y' node. **[2 marks]**

b. If the circuit is operated at VDD = 1.2V and clock frequency of 1GHz then, what is the dynamic power dissipation at the 'Y' node ? **[2 marks]**



6. A chip is produced using 90nm technology and occupies 100mm² of area with a yield of 50%. Each chip is sold for Rs. 200/- at a profit of Rs. 25/- per die. Now the company decided to design the same product in 65nm technology node, reducing the area by 20%. Answer the following questions. [CO1] **[2 marks]**

   a. What will be the new expected yield ? **[1 mark]**
   Sol: Yield is inversely dependent on area of die. Area reduces by 20% that is now new area is 80mm². New Yield = (50*100)/80 = 62.5%

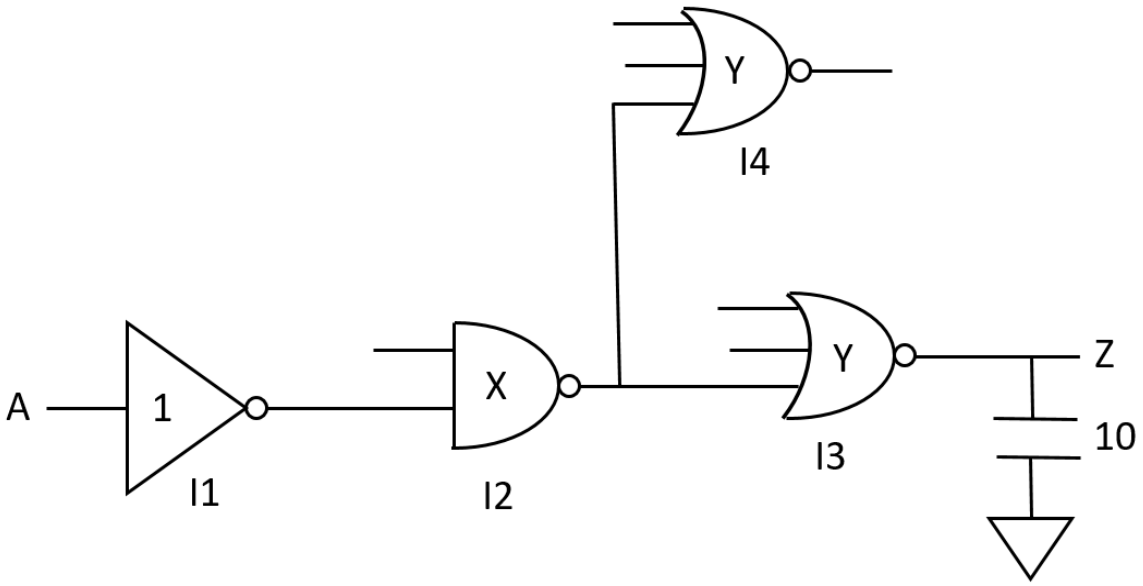
   b. Company decided to sell the product at the same price. What will be the new profit per die? **[1 mark]**
   Sol: Assuming that 100 dies are produced per wafer

Initial yield was 50%
No. of functional dies = 50
Every wafer earns = 50 x Rs. 200 = Rs. 10000
Total profit on 50 dies = 50 x Rs. 25 = Rs. 1250 (profit per die 25)

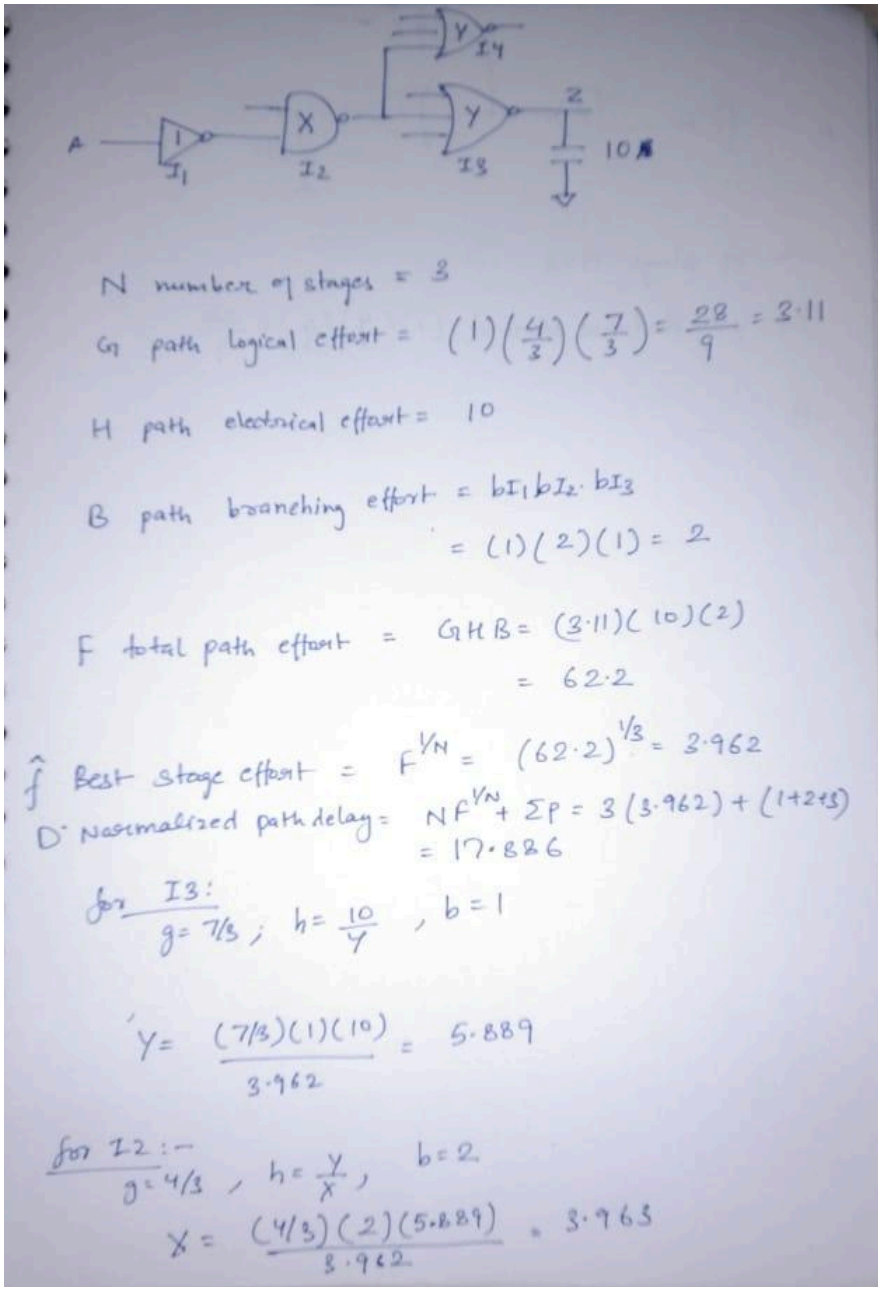
Total Dies made now = (100/80)*100 = 125
New Yield = 62.5%
No. of Good Dies = 125 x 0.625 = 78.125 equivalent to 78
So, now 28 extra dies could be sold at Rs. 200
Extra Profit = 28 x Rs. 200 = Rs. 5600
Total Profit = Rs. 5600 + Rs. 1250 = Rs. 6850
Profit per die = Rs.6850/78 = Rs. 87 or Rs. 88 (nearly)

**Marks only when the answer is correct for each part.

7. In the gate level schematic given below, find the normalized path delay from input A to Z via I1, I2, I3. Also find the values of drive strengths X and Y of gates I2 and I3 respectively. [CO2] **[3 Marks]**



Sol:



N number of stages = 3

G path logical effort = $(1)\left(\frac{4}{3}\right)\left(\frac{7}{3}\right) = \frac{28}{9} = 3.11$

H path electrical effort = 10

B path branching effort = $b_{I_1} b_{I_2} \cdot b_{I_3}$

$= (1)(2)(1) = 2$

F total path effort = $GHB = (3.11)(10)(2)$

$= 62.2$

$\hat{f}$ Best stage effort = $F^{1/N} = (62.2)^{1/3} = 3.962$

D Normalized path delay = $NF^{1/N} + \Sigma p = 3(3.962) + (1+2+3)$

$= 17.886$

for I3:

$g = 7/3$; $h = \frac{10}{Y}$, $b = 1$

$Y = \frac{(7/3)(1)(10)}{3.962} = 5.889$

for I2:-

$g = 4/3$, $h = \frac{Y}{X}$, $b = 2$

$X = \frac{(4/3)(2)(5.889)}{3.962} = 3.963$