End Semester Paper Rubric

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Q1. Answer the following questions. [8 Marks]

a. Flash memories are not used in making cache memories? List two reasons. [2 Marks] (CO4)

Ans: **Cache memory is a high-speed storage layer between the CPU and main memory,** designed to store frequently accessed data and instructions. This reduces latency, accelerates processing, and enhances system performance.

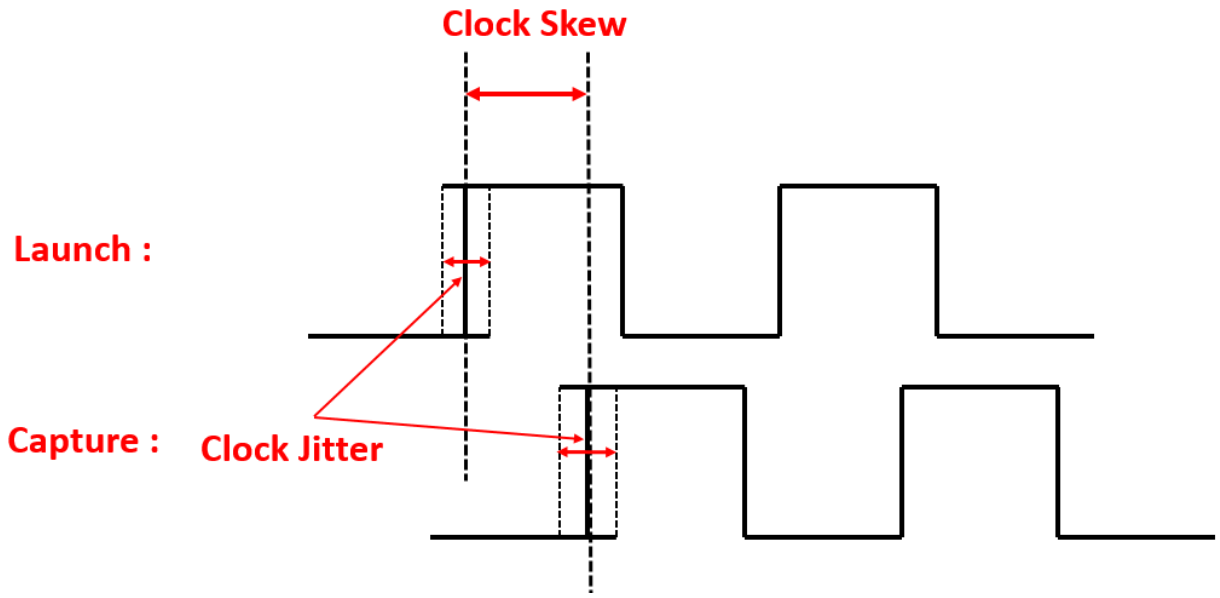
- **Flash cells, however, are slower than SRAM cells** and cannot match the CPU's clock speed.
- Additionally, **flash memory has significantly lower endurance compared to SRAM**. Since CPUs perform millions of read and write operations per second, flash memory cannot sustain it.

Therefore, flash memory is unsuitable for use in caches.

b. List any two differences between clock skew and clock jitter? [2 Marks] (CO4)

Ans:

Clock Skew	Clock Jitter
1. The time difference between the arrival of the same clock edge at the launch and capture flops. 2. It is due to differences in gate (number of gates) and wire delays (wire length) 3. It causes the clock signal to reach **different sequential elements** at different times.	1. Clock jitter refers to temporal variations in the consecutive edges of a clock signal causing deviations in timing from cycle to cycle. 2. Jitter can result from power supply noise, electromagnetic interference or variations in the clock generation circuit. Potentially degrading performance and causing timing violations in high speed design. 3. It affects the **same flip-flop** operating on the same clock, leading to inconsistent behavior across cycles.

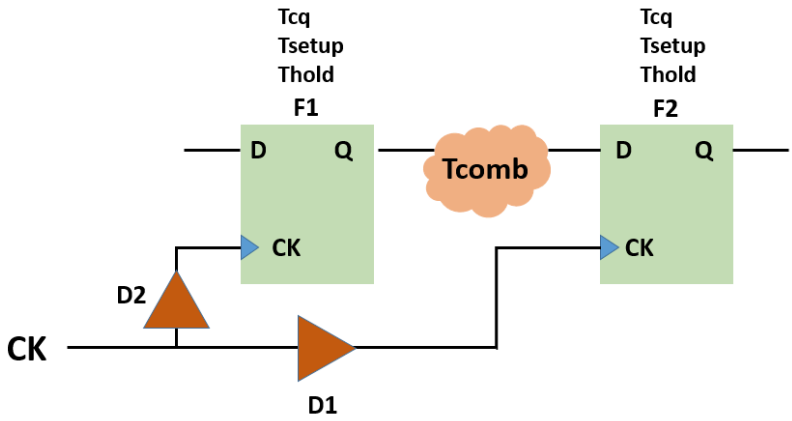


c. Long contacts are used in SRAM cell layouts. State the benefit of using long contact and why is it allowed to make long contacts in SRAM cells and not in other digital circuits or standard cells? [2 Marks] (CO4)

Ans: **Long contacts are permitted in memory cell layouts to save area.** This is possible because **memory cells are arranged in an array and all the abutments are fixed. This allows development of resolution enhancement techniques (RET) to ensure good Yield despite a rectangular shape**. Predefined masks specific to memories enable long contacts without causing yield loss.

Standard cells can be abutted with any other standard cells, so it is not possible to ascertain and fix the neighbourhood of long contacts. Therefore, it is not possible to design RETs for long contacts in standard cells. Therefore long contacts are not allowed in standard cells.

d. Tcomb is the delay of the combinational logic between flip flops, D1 and D2 are delays in clock path and Tcq, Tsetup and Thold are timing parameters of the flip flops. It is given that Tcomb, Tcq, Tsetup and Thold are fixed. For which of the following cases will the design be slower? Give reasons for your choice. [2 Marks] (CO4)



Case 1: D1 > D2
Case 2: D1 < D2
Case 3: D1 = D2
Case 4: Does not depend on D1 and D2

Ans:

Required Time = Tclk - (D1 - D2) - Tsetup
Arrival Time = Tcq + Tcomb

For no setup violation, Required Time > Arrival Time
Tclk > Tcq + Tcomb - (D1 - D2) + Tsetup

For Case1: D1 > D2,
D1 - D2 > 0,
Tclk1 > Tcq + Tcomb + Tsetup - (D1 - D2)
Tclk1 > Tcq + Tcomb + Tsetup - abs(D1 - D2)

For Case2: D1 < D2,
D1 - D2 < 0,
Tclk2 > Tcq + Tcomb + Tsetup - (D1 - D2)
Tclk2 > Tcq + Tcomb + Tsetup + abs(D1 - D2)

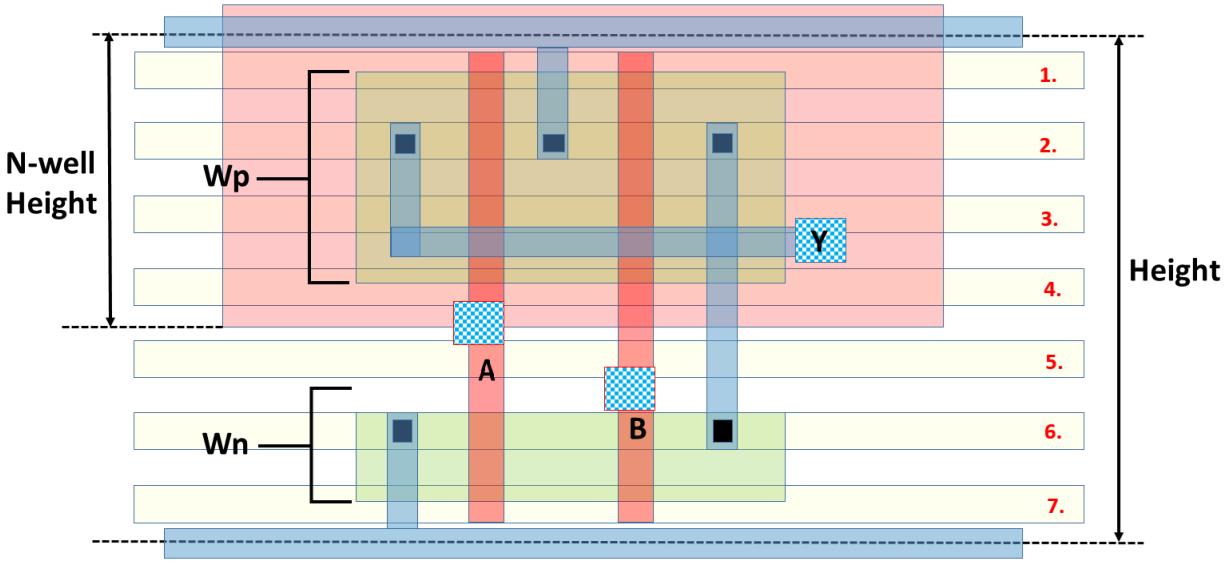
For Case3: D1 = D2,

D1 - D2 = 0
Tclk3 > Tcq + Tcomb + Tsetup

Tclk2 > Tclk3 > Tclk1

For D1 < D2, more time period is required to meet the setup requirement. Hence for **case 2, the design will be slower.**

Q2. Answer the following questions with respect to the given standard cell. (CO3)

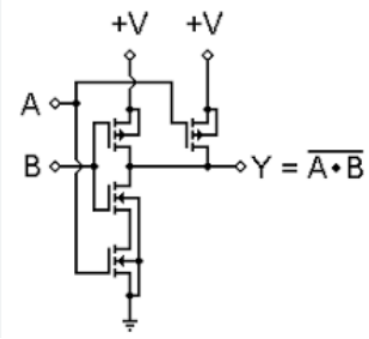


Following DRCs are given:

Pitch of Track = 0.2 um (Metal width = 0.1um and M-to-M spacing = 0.1um)
Poly Extension over OD (Active layer) = 0.08u
OD-Nwell Extension = 0.15um
OD-Nwell Spacing = 0.15um
Poly to Poly 1/2 DRC = 0.1um

a. Draw the CMOS schematic of the circuit implemented in the above standard cell. Also write the boolean expression for Y. [1 Mark]

Ans:



b. Using the DRCs given above, calculate the height of the standard cell and height of the Nwell. [2 Marks]

Ans: Std. Cell Height = Pitch of Track x No. of Track = 0.2um x 7 = 1.4um
Nwell Height = Pitch of Track x No. of Tracks through Nwell = 0.2 x 4 = 0.8um

c. Using the DRCs given above and heights calculated in part b, calculate the width of PMOS (Wp) and NMOS (Wn). [2 Marks]

Ans: 1/2DRC + Poly_Ext + Wp + OD_NW_Ext + OD_NW + Wn + Poly_Ext + 1/2DRC = 1.4um
=> Wp + Wn = 0.74um —---------- Eq(1)

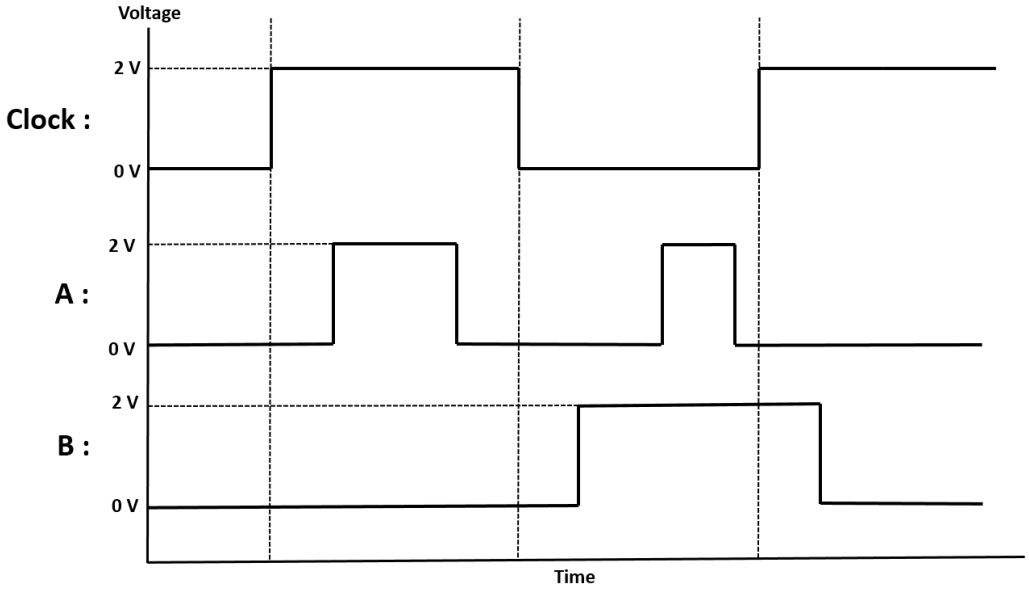
1/2DRC + Poly_Ext + Wp + OD_NW_Ext = 0.8um
=> Wp = 0.47um —----------Eq(2)

Substituting Eq(2) in Eq(1), we get Wn = 0.27um

d. As discussed during the project presentation, the pins need to span two tracks. Which tracks will you utilize when creating pins A, B, and Y? [3 Marks]

Ans: A: Tracks 4 and 5 as well as Tracks 5 and 6
B: Tracks 5 and 6
Y: Tracks 3 and 4

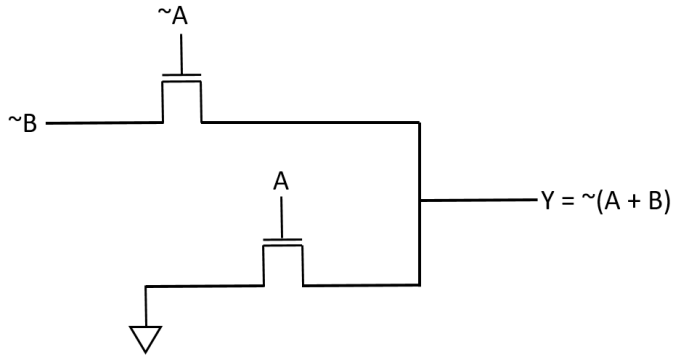
Q3. Answer the following questions (CO3)

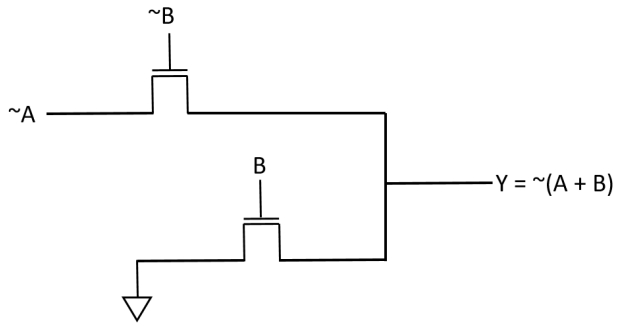


a. Implement 2 input NOR gate using pass transistor logic and dynamic logic. Use only NMOS for pass transistor logic. [2 Marks]

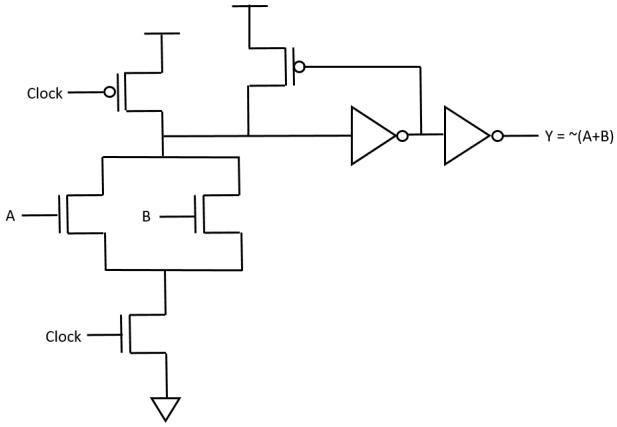
Ans:

PTL Implementation of 2 input NOR:



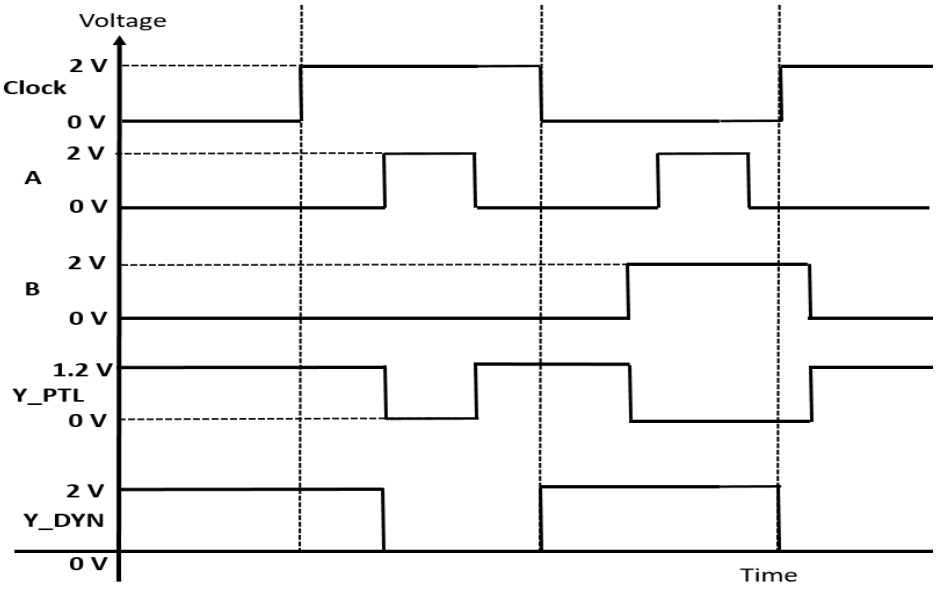


Dynamic logic based implementation of 2 input NOR:

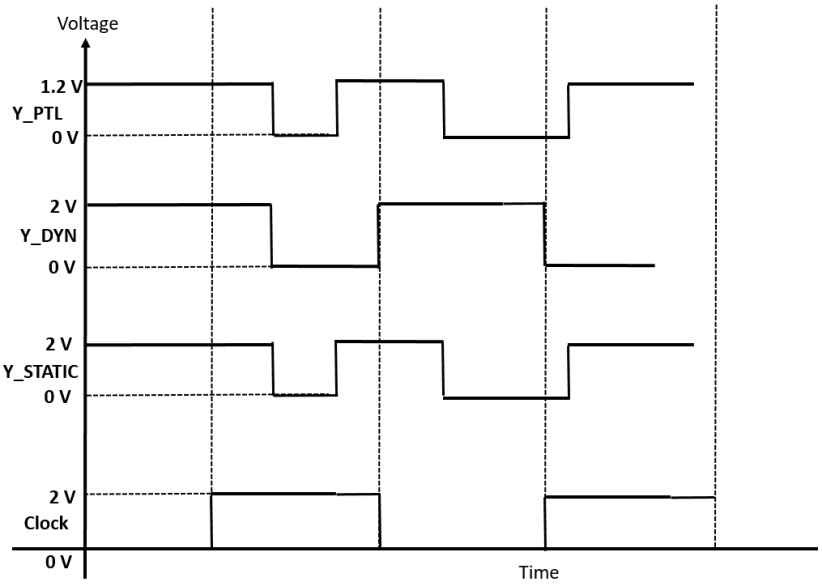


Marks will be given even if the keeper circuit is not made.

b. Stimuli shown in the given figure is applied to logic gates designed in part a. Draw the output waveforms of implementations of 2 input NOR gates. Clearly show the voltage levels of the output waveform.(Vtn = 0.8V and Vtp = -0.7V) [2 Marks]



c. Compare the output waveform of the pass transistor gate and dynamic gate with the output waveform obtained from the static CMOS gate. Give reasons for the mismatches in waveforms of pass transistor logic and dynamic logic implementation. [2 Marks]



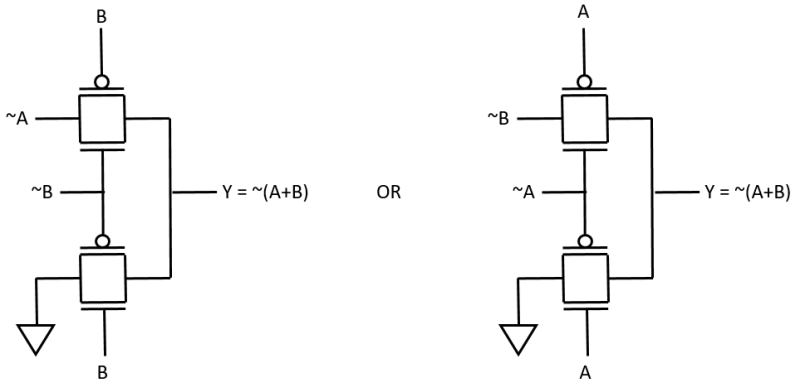
Ans: On comparing output of pass transistor based implementation of NOR gate with output of static CMOS based implementation, it is observed that the functionality of the gate remains unaffected but the output waveform does not have a **rail to rail swing.** The maximum output voltage level for a pass transistor based gate is 1.2 V while the maximum voltage level for static CMOS based gate is 2V. This is due to **weak pull up characteristics of an NMOS device**. It can **pull-up up to VDD - Vtn but NMOS devices are strong pull down devices and hence can pull down to complete 0 voltage level**.

For a dynamic gate, there are two phases: one is the precharge phase when clock = 0 and other is evaluate phase when clock = 1. When clock = 0 then the output is precharged to logic 1. **During the precharge phase, there is no effect of any transitions in the input, on the output of the gate**. Which can be observed in the second precharge phase. We should compare the output waveform only in the evaluate phase. In the first evaluate phase, the output waveform mismatches with the output of the static CMOS gate. **It mismatches at the point where A makes a transition from 1 to 0.**

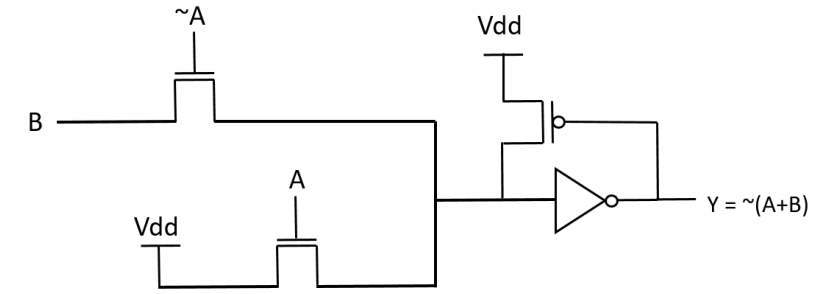
d. If the behavior of the PTL or dynamic NOR gate is different from static NOR gate, how would you remove these mismatches? Make necessary changes in the circuit if possible. [2 Marks]

Ans:
In pass transistor logic, the voltage swing in the output waveform was not rail to rail. The logic high was 1.2V while logic 0 was 0V. While in the static CMOS gate, logic high was 2V and logic 0 was 0V. To resolve this issue we can use a Transmission gate based design. Transmission gate is made of both PMOS and NMOS. PMOS is a strong pull up device while NMOS is a strong pull down. Hence a transmission gate can help to restore the rail to rail swing in the output waveform.

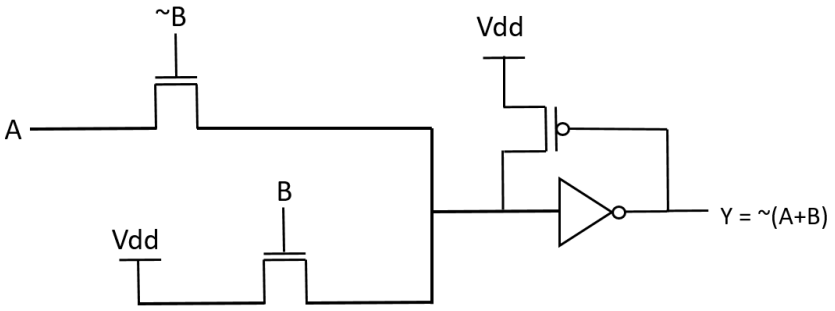
Transmission gate based implementation:



Keeper Circuit in PTL:



or



There can be many other implementations. Marks will be given by carefully examining those implementations.

It is a limitation of dynamic circuits that 1 to 0 transitions are ignored in the evaluation phase.

e. A 2 input OR gate is implemented by cascading a CMOS inverter at the output of the 2 input NOR gate implemented in pseudo NMOS logic. Output of OR gate is 0 only one of input A or B is high. It is observed that this happens only in SF corner. What could be the possible reason behind this symptom? How would you prevent this? [1 Mark]

Ans: Pseudo NMOS designs are ratioed logic. In cross corners like SF/FS this ratio can change considerably and impact circuit functionality.
In the given case, at the SF corner, Vt of NMOS is high and therefore its current is low. However Vt of PMOS is low and it can drive a larger current. If only one of the NMOS devices turns on, it is unable to sink the current of the always on PMOS device. Therefore output of NOR remains high enough and output of OR gate remains low.
To prevent this we must verify across all the cross corners.

Q4. In a pipelined circuit, three independent stages have delays of 3ns, 5 ns, and 4 ns respectively. (CO4)

a) Without time borrowing, what would be the clock period of the pipeline? Explain. (1 Mark)
b) How can time borrowing be utilized to improve the design? Propose a revised clock period considering time borrowing and explain its impact on the pipeline's performance. (2 Marks)

Ignore sequencing overheads in the above analysis.

Ans: (a)Without time borrowing, the clock period is determined by the stage with the maximum delay:

Tclock=max(Stage 1, Stage 2, Stage 3)=5 ns

This is because all stages need to **align with the longest stage to avoid data loss.**

(b) Time borrowing **allows shorter stages to lend unused slack to longer stages**, effectively redistributing delay across stages. This reduces the constraints on the longest stage and enables balancing.

For this pipeline:

Tclock=Average of total delays across stages=(3 ns+5 ns+4 ns)/3 =4 ns

When time borrowing is implemented, **the slack from Stage 1 can be used to increase the effective time available for Stage 2**:

Stage 1 Lending Slack: Stage 1 completes its operation in 3 ns and has 1 ns of slack. This slack allows Stage 2 to begin processing slightly earlier. Therefore the clock period reduces to 4 ns.

Q5: You have two 6T SRAM cell designs, Design1 and Design2 with the given PU,PG,PD size in 65nm technology . (CO4)

Design 1: PD = 300/70 ,PU = 125/70 , PG= 270/70
Design 2: PD = 260/70 ,PU = 125/70 , PG = 180/70

a. Which design has better SNM?
   Ans: Design 1 (Because it has larger PD, Rpd less and Vbump less so more stability during read)
b. Which design has better write margin?
   Ans: Design 1 (Because it has stronger PG so we can easily overpower PU)
c. Which design has more bit line leakage?
   Ans: Design 1 (Larger PG means more bitline leakage)
d. Which cell has lower leakage?
   Ans: Design 2 (As Larger PG and PD will leak more in subthreshold)