



ic 7432 truth table

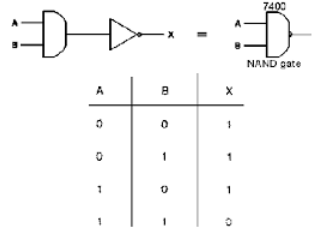
praveen kumar

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Input	Input	Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

INPUT		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table



S.NO	GATE	SYMBOL	INPUTS	OUTPUT
1	NAND IC 7403		A, B	C
2	NOR IC 7402		A, B	C
3	AND IC 7408		A, B	C
4	OR IC 7401		A, B	C
5	NOT IC 7404		A	C
6	EX-OR IC 7400		A, B	C

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Input	Input	Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

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IC 7432: It is a quad two input OR gate used independently. On any gate if the Output is 'High' ...

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put	Input	Output
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

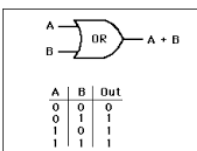
2-INPUT NAND

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

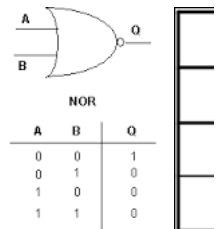
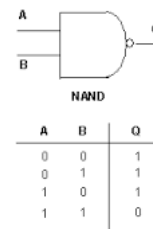
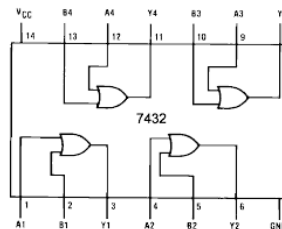
Truth Table

NAND Gate Truth Table

Inputs	Output
A B	C
0 0	1
0 1	1
1 0	1
1 1	0



The OR operation will be signified by $A + B$. Other common mathematical notations for it are $A \vee B$ and $A \cup B$, called the union of A and B.



S.NO	GATE	SYMBOL	INPUTS	OUTPUT
1	NAND IC 7403		A, B	C
2	NOR IC 7402		A, B	C
3	AND IC 7408		A, B	C
4	OR IC 7401		A, B	C
5	NOT IC 7404		A	C
6	EX-OR IC 7400		A, B	C

S.NO	GATE	SYMBOL	INPUTS	OUTPUT
1	NAND IC 7403		A, B	C
2	NOR IC 7402		A, B	C
3	AND IC 7408		A, B	C
4	OR IC 7401		A, B	C
5	NOT IC 7404		A	C
6	EX-OR IC 7400		A, B	C

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

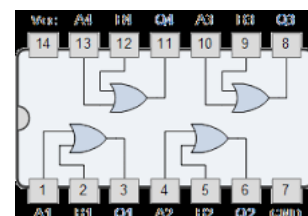
INPUT		OUTPUT
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Inputs			Output
W	X	Y	Z = W + X + Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

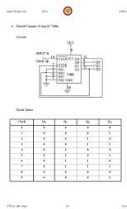
S.NO	GATE	SYMBOL	INPUTS	OUTPUT
1	NAND IC 7403		A, B	C
2	NOR IC 7402		A, B	C
3	AND IC 7408		A, B	C
4	OR IC 7401		A, B	C
5	NOT IC 7404		A	C
6	EX-OR IC 7400		A, B	C

Inputs		Outputs
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

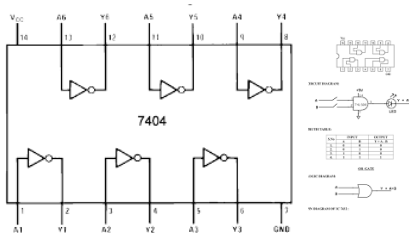
ANSI Symbol	IC Symbol	Description	Boolean
		The AND gate output is at logic 1 when, and only when, all its inputs are at logic 1. If all the inputs are at logic 0, the output is at logic 0.	$X = A \cdot B$
		The NAND gate output is at logic 1 when one or more of its inputs are at logic 1. If all the inputs are at logic 0, the output is at logic 1.	$X = A \cdot B$
		The OR gate output is at logic 1 when one or more of its inputs are at logic 1. If all the inputs are at logic 0, the output is at logic 0.	$X = A + B$
		The NOR gate output is at logic 1 when one or more of its inputs are at logic 0. If all the inputs are at logic 1, the output is at logic 0.	$X = A + B$
		The XOR gate output is at logic 1 when one or more of its inputs are at logic 1, but the output is at logic 0 when all inputs are at logic 1.	$X = A \oplus B$
		The XNOR gate output is at logic 1 when one or more of its inputs are at logic 1, but the output is at logic 0 when all inputs are at logic 1.	$X = A \oplus B$



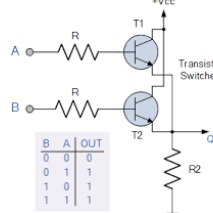
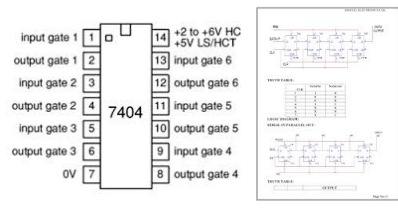
S.NO	GATE	SYMBOL	INPUTS	OUTPUT
1	NAND IC 7403		A, B	C
2	NOR IC 7402		A, B	C
3	AND IC 7408		A, B	C
4	OR IC 7401		A, B	C
5	NOT IC 7404		A	C
6	EX-OR IC 7400		A, B	C



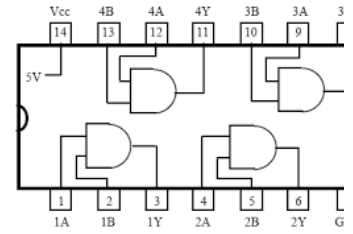
Analog Input	A	B	C	Digital Output	
				X	Y
0 to $\frac{1}{4}V_{cc}$	0	0	0	0	0
$\frac{1}{4}V_{cc}$ to $\frac{2}{4}V_{cc}$	0	0	1	0	1
$\frac{2}{4}V_{cc}$ to $\frac{3}{4}V_{cc}$	0	1	1	1	0
$\frac{3}{4}V_{cc}$ to V_{cc}	1	1	1	1	1



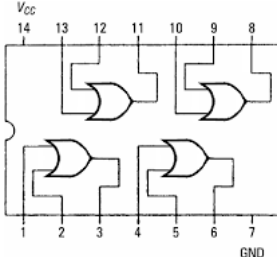
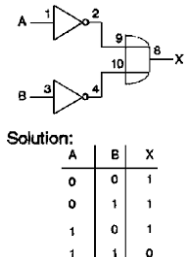
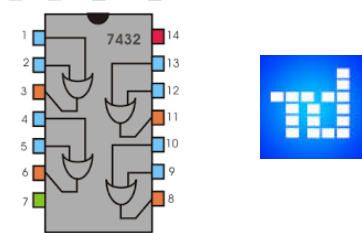
Input Data A				Input Data B				Addition			
A4	A3	A2	A1	B4	B3	B2	B1	S4	S3	S2	S1
1	0	0	0	0	0	1	0	1	0	1	0
1	0	0	0	1	0	0	0	1	0	0	0
0	0	1	0	1	0	0	0	1	0	1	0
0	0	0	1	0	1	1	1	1	0	0	0
1	0	1	0	1	0	1	1	1	0	0	1
1	1	1	0	1	1	1	1	1	0	1	0
1	0	1	0	1	1	0	1	1	0	1	1



Inputs			Outputs							
a	b	c	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	1	0	0
1	0	1	0	0	0	0	0	0	1	0
1	1	0	0	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	1
Output function			\overline{abc}	$\overline{a}bc$	$a\overline{bc}$	abc	\overline{abc}	$\overline{a}bc$	$a\overline{bc}$	abc



I/P O/P +V_{cc} Ground



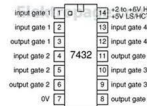
Truth Table

The truth table has an entry for each possible combination of inputs.
For n inputs there will be 2^n entries ... 2 inputs = 4 entries.

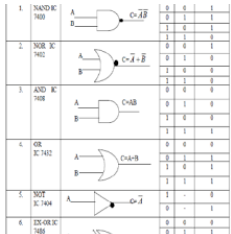
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

We can have more than two inputs in which case the only time we would have a 1 out is when all the inputs are true.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

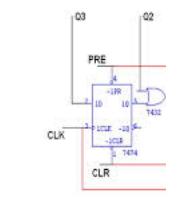
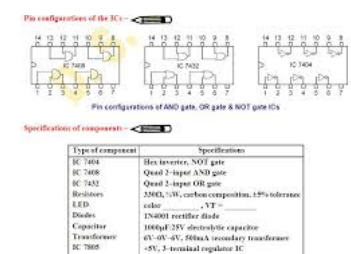
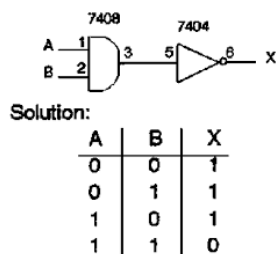
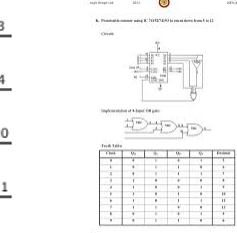
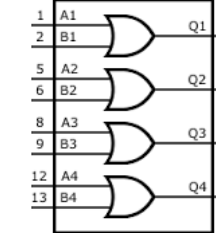


BCD Input				Excess-3 Output			
B3	B2	B1	B0	C3	C2	C1	C0
0	0	0	0	1	0	0	0
0	0	0	1	1	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	1	0	1	1
0	1	0	0	1	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	1	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1



CLK	Q3	Q2	Q1	Q0	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

Excess-3 Input				BCD Output			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	0	1	0	1	0	1
0	0	1	0	1	0	0	0
0	0	1	0	1	0	0	1
0	0	1	1	1	0	1	0
0	0	1	1	1	0	1	1
0	1	0	0	1	1	0	0
0	1	0	0	1	1	0	1
0	1	0	1	1	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	1	1	1	0
0	1	1	0	1	1	1	1
0	1	1	1	1	1	1	1



FUNCTION TABLE

INPUTS		OUTPUT
A	B	
H	X	H
X	H	H
L	L	L

INPUT		OUTPUT
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

Inputs		Output
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

