# List of 4000 and 7400 series integrated circuits

Source: [Wikipedia](#)

## List of 4000 series

| 4000 | Dual 3-input NOR gate + 1 Inverter |
|------|-------------------------------------|
| 4001 | Quad 2-input NOR gate |
| 4002 | Dual 4-input NOR gate |
| 4006 | 18 stage Shift register |
| 4007 | Dual Complementary Pair Plus Inverter |
| 4008 | 4 bit adder |
| 4009 | Hex inverting buffer |
| 4010 | Hex non-inverting buffer |
| 4011 | Buffered Quad 2-Input NAND gate |
| 4012 | Dual 4-input NAND gate |
| 4013 | Dual D-type flip-flop |
| 4014 | 8-stage shift register |
| 4015 | Dual 4-stage shift register |
| 4016 | Quad bilateral switch |
| 4017 | Divide-by-10 counter (5-stage Johnson counter) |
| 4018 | Presettable divide-by-n counter |
| 4019 | Quad AND-OR Select Gate |
| 4020 | 14-stage binary counter |
| 4021 | 8-bit static shift register |
| 4022 | Divide-by-8 counter (4-stage Johnson counter) |
| 4023 | Triple 3-input NAND gate |
| 4024 | 7-Stage Binary Ripple Counter |
| 4025 | Triple 3-input NOR gate |
| 4026 | BCD counter with decoded 7-segment output |
| 4027 | Dual JK flip-flop |
| 4028 | BCD to decimal (1-of-10) decoder |
| 4029 | Presettable up/down counter, binary or BCD-decade |
| 4030 | Quad XOR gate (replaced by 4070) |
| 4031 | 64-Bit Static Shift Register |
| 4032 | Triple serial adder |

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|---|---|
| 4033 | BCD counter + 7-segment decoder w/ripple blank |
| 4034 | 8-stage bidirectional parallel or serial input/parallel output |
| 4035 | 4-stage parallel-in/parallel-out (PIPO) with J-K input and true/complement output |
| 4038 | Triple serial adder |
| 4040 | 12-stage binary ripple counter |
| 4041 | Quad true/complement buffer |
| 4042 | Quad D-type latch |
| 4043 | Quad NOR R/S latch |
| 4044 | Quad NAND R/S latch (tristate output) |
| 4045 | 21-Stage Counter |
| 4046 | PLL with VCO |
| 4047 | Monostable/Astable Multivibrator |
| 4048 | Multifunctional expandable 8-input (tristate output) |
| 4049 | Hex inverter/buffer (NOT gate) |
| 4050 | Hex buffer/converter (non-inverting) |
| 4051 | Analogue multiplexer/demultiplexer (1-of-8 switch) |
| 4052 | Analogue multiplexer/demultiplexer (Dual 1-of-4 switch) |
| 4053 | Analogue multiplexer/demultiplexer (Triple 1-of-2 switch) |
| 4054 | 7-segment decoder/LCD driver |
| 4055 | BCD-to-7-segment decoder/driver with "display-frequency" output |
| 4056 | BCD-to-7-segment decoder/driver with strobed latch function |
| 4059 | Programmable divide-by-N counter |
| 4060 | 14-stage binary ripple counter and oscillator |
| 4062 | Logic dual 3 majority gate |
| 4063 | 4-bit Digital comparator |
| 4066 | Quad Analog switch (Low "ON" Resistance) |
| 4067 | 16-channel analogue multiplexer/demultiplexer (1-of-16 switch) |
| 4068 | 8-input NAND gate |
| 4069 | Hex inverter |
| 4070 | Quad XOR gate |
| 4071 | Quad 2-input OR gate |
| 4072 | Dual 4-input OR gate |
| 4073 | Triple 3-input AND gate |
| 4075 | Triple 3-input OR gate |
| 4076 | Quad D-type register with tristate outputs |

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|---|---|
| 4077 | Quad 2-input XNOR gate |
| 4078 | 8-input NOR gate |
| 4081 | Quad 2-input AND gate |
| 4082 | Dual 4-input AND gate |
| 4085 | Dual 2-wide, 2-input AND/OR invert (AOI) |
| 4086 | Expandable 4-wide, 2-input AND/OR invert (AOI) |
| 4089 | Binary rate multiplier |
| 4093 | Quad 2-input Schmitt trigger NAND gate |
| 4094 | 8-stage shift-and-store bus |
| 4095 | Gated "J-K" (non-inverting) |
| 4096 | Gated "J-K" (inverting and non-inverting) |
| 4097 | Differential 8-channel analog multiplexer/demultiplexer |
| 4098 | Dual one-shot monostable |
| 4099 | 8-bit addressable latch |
| 4104 | Quad Low-to-High Voltage Translator with tristate outputs |
| 4502 | Hex inverting buffer (tristate) |
| 4503 | Hex non-inverting buffer with tristate outputs |
| 4504 | Hex voltage level shifter for TTL-to-CMOS or CMOS-to-CMOS operation |
| 4508 | Dual 4-bit latch with tristate outputs |
| 4510 | Presettable 4-bit BCD up/down counter |
| 4511 | BCD to 7-segment latch/decoder/driver |
| 4512 | 8-input multiplexer (data selector) with tristate output |
| 4513 | BCD to 7-segment latch/decoder/driver (4511 plus ripple blanking) |
| 4514 | 1-of-16 decoder/demultiplexer active HIGH output |
| 4515 | 1-of-16 decoder/demultiplexer active LOW output |
| 4516 | Presettable 4-bit binary up/down counter |
| 4517 | Dual 64-Bit Static Shift Register |
| 4518 | Dual BCD up counter |
| 4519 | Quad 2-input multiplexer (data selector) |
| 4520 | Dual 4-bit binary up counter |
| 4521 | 24-stage frequency divider |
| 4522 | Programmable BCD divide-by-N counter |
| 4526 | Programmable 4-bit binary down counter |
| 4527 | BCD rate multiplier |
| 4528 | Dual Retriggerable Monostable Multivibrator with Reset |

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|---|---|
| 4529 | Dual 4-channel analog |
| 4532 | 8-bit priority encoder |
| 4536 | Programmable Timer |
| 4538 | Dual Retriggerable Precision Monostable Multivibrator |
| 4539 | Dual 4-input multiplexer |
| 4541 | Programmable Timer |
| 4543 | BCD to 7-Segment Latch/Decoder/Driver with Phase Input |
| 4553 | 3-digit BCD counter |
| 4555 | Dual 1-of-4 decoder/demultiplexer active HIGH output |
| 4556 | Dual 1-of-4 decoder/demultiplexer active LOW output |
| 4557 | 1-to-64 Bit Variable Length Shift Register |
| 4560 | NBCD adder |
| 4566 | Industrial time-base generator |
| 4572 | Hex gate : quad NOT, single NAND, single NOR |
| 4584 | Hex schmitt trigger |
| 4585 | 4-bit Digital comparator |
| 4724 | 8-bit addressable latch |
| 4750 | Frequency synthesizer |
| 4751 | Universal divider |
| 4794 | 8-Stage Shift-and-Store Register LED Driver |
| 4894 | 12-Stage Shift-and-Store Register LED Driver |
| 4938 | Dual Retriggerable Precision Monostable Multivibrator with Reset |
| 4952 | 8-channel analog multiplexer/demultiplexer |
| 40098 | 3-state hex inverting buffer |
| 40100 | 32-bit left/right Shift Register |
| 40101 | 9-bit Parity Generator/Checker |
| 40102 | Presettable 2-decade BCD down counter |
| 40103 | Presettable 8-bit binary down counter |
| 40104 | 4 bit bidirectional Parallel-in/Parallel-out PIPO Shift Register (tristate) |
| 40105 | 4-bit x 16 word Register |
| 40106 | Hex Inverting Schmitt-Trigger-(NOT gates) |
| 40107 | dual 2-input NAND buffer/driver |
| 40108 | 4x4-bit (tristate) synchronous triple-port register file |
| 40109 | Quad level shifter |
| 40110 | Up/Down Counter-Latch-Decoder-Driver |

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|---|---|
| 40116 | 8-bit bidirectional CMOS-to-TTL level converter |
| 40117 | Programmable dual 4-bit terminator |
| 40147 | 10-line to 4-line [BCD] priority encoder |
| 40160 | Decade counter/asynchronous clear |
| 40161 | Binary counter/asynchronous clear |
| 40162 | 4-bit synchronous decade counter with load, reset, and ripple carry output |
| 40163 | 4-bit synchronous binary counter with load, reset, and ripple carry output |
| 40174 | Hex D-type flip-flop with reset; positive-edge trigger |
| 40175 | Quad D-type flip-flop with reset; positive-edge trigger |
| 40181 | 4-bit 16-function arithmetic logic unit (ALU) |
| 40192 | Presettable 4-bit BCD up/down counter |
| 40193 | Presettable 4-bit binary up/down counter |
| 40194 | 4-bit universal bidirectional with asynchronous master reset |
| 40195 | 4-bit universal shift register |
| 40208 | $4 \times 4$-bit (tristate) synchronous triple-port register file |
| 40240 | Buffer/Line driver; Inverting (tristate) |
| 40244 | Buffer/Line Driver; Non-Inverting (tristate) |
| 40245 | Octuple bus transceiver; (tristate) outputs, |
| 40257 | Quad 2-Line-to-1-Line Data Selector/Multiplexer (tristate) |
| 40373 | Octal D-Type Transparent latch (tristate) |
| 40374 | Octal D-type flip-flop; positive-edge trigger (tristate) |

# List of 7400 series

7400 series derivative families

### ❖ Bipolar

- **74** - The "standard TTL" logic family had no letters between the "74" and the specific part number.
- **74L** - Low power (compared to the original TTL logic family), very slow
- **H** - High speed (still produced but generally superseded by the S-series, used in 1970s era computers)
- **S** - Schottky (obsolete)
- **LS** - Low Power Schottky
- **AS** - Advanced Schottky
- **ALS** - Advanced Low Power Schottky
- **F** - Fast (faster than normal Schottky, similar to AS)

### ❖ CMOS

- **C** - CMOS 4–15 V operation similar to buffered 4000 (4000B) series
- **HC** - High speed CMOS, similar performance to LS, 12 nS
- **HCT** - High speed, compatible logic levels to bipolar parts
- **AC** - Advanced CMOS, performance generally between S and F
- **AHC** - Advanced High-Speed CMOS, three times as fast as HC
- **ALVC** - Low voltage - 1.65 to 3.3 V, Time Propagation Delay (TPD) 2 nS[7]
- **AUC** - Low voltage - 0.8 to 2.7 V, TPD < 1.9 nS@1.8 V[7]
- **FC** - Fast CMOS, performance similar to F
- **LCX** - CMOS with 3 V supply and 5 V tolerant inputs
- **LVC** - Low voltage – 1.65 to 3.3 V and 5 V tolerant inputs, tpd < 5.5 nS@3.3 V, tpd < 9 nS@2.5 V[7]
- **LVQ** - Low voltage - 3.3 V
- **LVX** - Low voltage - 3.3 V with 5 V tolerant inputs
- **VHC** - Very High Speed CMOS - 'S' performance in CMOS technology and power

### ❖ BiCMOS

- **BCT** - BiCMOS, TTL-compatible input thresholds, used for buffers
- **ABT** - Advanced BiCMOS, TTL-compatible input thresholds, faster than ACT and BCT

| Part number | Description | |
|---|---|---|
| **7400** | quad 2-input NAND gate | |
| **741G00** | single 2-input NAND gate | |
| **7401** | quad 2-input NAND gate with open collector outputs | |
| **741G01** | single 2-input NAND gate with open drain output | |
| **7402** | quad 2-input NOR gate | |
| **741G02** | single 2-input NOR gate | |
| **7403** | quad 2-input NAND gate with open collector outputs | |
| **741G03** | single 2-input NAND gate with open drain output | |
| **7404** | hex inverter | |
| **741G04** | single inverter | |
| **7405** | hex inverter with open collector outputs | |
| **741G05** | single inverter with open drain output | |
| **7406** | hex inverter buffer/driver with 30 V open collector outputs | |
| **741G06** | single inverting buffer/driver with open drain output | |
| **7407** | hex buffer/driver with 30 V open collector outputs | |
| **741G07** | single non-inverting buffer/driver with open drain output | |
| **7408** | quad 2-input AND gate | |
| **741G08** | single 2-input AND gate | |
| **7409** | quad 2-input AND gate with open collector outputs | |
| **741G09** | single 2-input AND gate with open drain output | |
| **7410** | triple 3-input NAND gate | |
| **7411** | triple 3-input AND gate | |
| **7412** | triple 3-input NAND gate with open collector outputs | |
| **7413** | dual Schmitt trigger 4-input NAND gate | |
| **7414** | hex Schmitt trigger inverter | |
| **741G14** | single Schmitt trigger inverter | |
| **7415** | triple 3-input AND gate with open collector outputs | |
| **7416** | hex inverter buffer/driver with 15 V open collector outputs | |
| **7417** | hex buffer/driver with 15 V open collector outputs | |
| **741G17** | single Schmitt-trigger buffer | |
| **7418** | dual 4-input NAND gate with Schmitt trigger inputs | |
| **7419** | hex Schmitt trigger inverter | |

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|---|---|---|
| **7420** | dual 4-input NAND gate | |
| **7421** | dual 4-input AND gate | |
| **7422** | dual 4-input NAND gate with open collector outputs | |
| **7423** | expandable dual 4-input NOR gate with strobe | |
| **7424** | quad 2-input NAND gate gates with schmitt-trigger line-receiver inputs. | |
| **7425** | dual 4-input NOR gate with strobe | |
| **7426** | quad 2-input NAND gate with 15 V open collector outputs | |
| **7427** | triple 3-input NOR gate | |
| **741G27** | single 3-input NOR gate | |
| **7428** | quad 2-input NOR buffer | |
| **7430** | 8-input NAND gate | |
| **7431** | hex delay elements | |
| **7432** | quad 2-input OR gate | |
| **741G32** | single 2-input OR gate | |
| **7433** | quad 2-input NOR buffer with open collector outputs | |
| **7436** | quad 2-input NOR gate (different pinout than 7402) | |
| **7437** | quad 2-input NAND buffer | |
| **7438** | quad 2-input NAND buffer with open collector outputs | |
| **7439** | quad 2-input NAND buffer | |
| **7440** | dual 4-input NAND buffer | |
| **7441** | BCD to decimal decoder/Nixie tube driver | |
| **7442** | BCD to decimal decoder | |
| **7443** | excess-3 to decimal decoder | |
| **7444** | excess-3-Gray code to decimal decoder | |
| **7445** | BCD to decimal decoder/driver | |
| **7446** | BCD to seven-segment display decoder/driver with 30 V open collector outputs | |
| **7447** | BCD to 7-segment decoder/driver with 15 V open collector outputs | |
| **7448** | BCD to 7-segment decoder/driver with Internal Pullups | |
| **7449** | BCD to 7-segment decoder/driver with open collector outputs | |
| **7450** | dual 2-wide 2-input AND-OR-invert gate (one gate expandable) | |
| **7451** | dual 2-wide 2-input AND-OR-invert gate | |
| **7452** | expandable 4-wide 2-input AND-OR gate | |
| **7453** | expandable 4-wide 2-input AND-OR-invert gate | |
| **7454** | 4-wide 2-input AND-OR-invert gate | |
| **7455** | 2-wide 4-input AND-OR-invert Gate (74H version is expandable) | |

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|---|---|---|
| **7456** | 50:1 [frequency divider](#) | |
| **7457** | 60:1 frequency divider | |
| **7458** | 2-input & 3-input AND-OR Gate | |
| **7459** | 2-input & 3-input AND-OR-invert Gate | |
| **7460** | dual 4-input expander | |
| **7461** | triple 3-input expander | |
| **7462** | 3-2-2-3-input AND-OR expander | |
| **7463** | hex current sensing interface gates | |
| **7464** | 4-2-3-2-input AND-OR-invert gate | |
| **7465** | 4-2-3-2 input AND-OR-invert gate with open collector output | |
| **7468** | dual 4 bit decade counters | |
| **7469** | dual 4 bit binary counters | |
| **7470** | AND-gated positive edge triggered J-K [flip-flop](#) with preset and clear | |
| **74H71** | AND-or-gated J-K master-slave flip-flop with preset | |
| **74L71** | AND-gated R-S master-slave flip-flop with preset and clear | |
| **7472** | AND gated J-K master-slave flip-flop with preset and clear | |
| **7473** | dual J-K flip-flop with clear | |
| **7474** | dual D positive edge triggered flip-flop with preset and clear | |
| **7475** | 4-bit bistable [latch](#) | |
| **7476** | dual J-K flip-flop with preset and clear | |
| **7477** | 4-bit bistable latch | |
| **74H78** | dual positive pulse triggered J-K flip-flop with preset, common clock, and common clear (different pinout than 74L78 / 74Ls78) | |
| **74L78** | dual positive pulse triggered J-K flip-flop with preset, common clock, and common clear | |
| **74Ls78** | dual negative edge triggered J-K flip-flop with preset, common clock, and common clear | |
| **7479** | dual D flip-flop | |
| **741G79** | single D-type flip-flop positive edge trigger non-inverting output | |
| **7480** | gated [full adder](#) | |
| **741G80** | single D-type flip-flop positive edge trigger inverting output | |
| **7481** | 16-bit [random access memory](#) | |
| **7482** | 2-bit binary full adder | |
| **7483** | 4-bit binary full adder | |
| **7484** | 16-bit [random access memory](#) | |

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|---|---|---|
| **7485** | 4-bit [magnitude comparator](#) | |
| **7486** | quad 2-input [XOR gate](#) | |
| **741G86** | single 2 input exclusive-OR gate | |
| **7487** | 4-bit true/complement/zero/one element | |
| **7488** | 256-bit [read-only memory](#) | |
| **7489** | 64-bit random access memory | |
| **7490** | [decade counter](#) (separate divide-by-2 and divide-by-5 sections) | |
| **7491** | 8-bit [shift register](#), serial In, serial out, gated input | |
| **7492** | divide-by-12 counter (separate divide-by-2 and divide-by-6 sections) | |
| **7493** | 4-bit binary counter (separate divide-by-2 and divide-by-8 sections) | |
| **7494** | 4-bit shift register, dual asynchronous presets | |
| **7495** | 4-bit shift register, parallel In, parallel out, serial input | |
| **7496** | 5-bit parallel-In/parallel-out shift register, asynchronous preset | |
| **7497** | synchronous 6-bit binary rate multiplier | |
| **741G97** | configurable multiple-function gate | |
| **7498** | 4-bit data selector/storage register | |
| **7499** | 4-bit bidirectional universal shift register | |
| **74100** | dual 4-bit bistable latch | |
| **74101** | AND-or-gated J-K negative-edge-triggered flip-flop with preset | |
| **74102** | AND-gated J-K negative-edge-triggered flip-flop with preset and clear | |
| **74103** | dual J-K negative-edge-triggered flip-flop with clear | |
| **74104** | J-K master-slave flip-flop | |
| **74105** | J-K master-slave flip-flop | |
| **74106** | dual J-K negative-edge-triggered flip-flop with preset and clear | |
| **74107** | dual J-K flip-flop with clear | |
| **74107a** | dual J-K negative-edge-triggered flip-flop with clear | |
| **74108** | dual J-K negative-edge-triggered flip-flop with preset, common clear, and common clock | |
| **74109** | dual J-Not-K positive-edge-triggered flip-flop with clear and preset | |
| **74110** | AND-gated J-K master-slave flip-flop with data lockout | |
| **74111** | dual J-K master-slave flip-flop with data lockout | |
| **74112** | dual J-K negative-edge-triggered flip-flop with clear and preset | |
| **74113** | dual J-K negative-edge-triggered flip-flop with preset | |
| **74114** | dual J-K negative-edge-triggered flip-flop with preset, common clock and clear | |
| **74116** | dual 4-bit latch with clear | |

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|---|---|---|
| **74118** | hex set/reset latch | |
| **74119** | hex set/reset latch | |
| **74120** | dual pulse synchronizer/drivers | |
| **74121** | monostable multivibrator | |
| **74122** | retriggerable monostable multivibrator with clear | |
| **74123** | dual retriggerable monostable multivibrator with clear | |
| **741G123** | single retriggerable monostable multivibrator with clear | |
| **74124** | dual voltage-controlled oscillator | |
| **74125** | quad bus buffer with three-state outputs, negative enable | |
| **741G125** | buffer/Line driver, three-state output with active low output enable | |
| **74126** | quad bus buffer with three-state outputs, positive enable | |
| **74128** | quad 2-input NOR Line driver | |
| **741G126** | buffer/line driver, three-state output with active high output enable | |
| **74130** | quad 2-input AND gate buffer with 30 V open collector outputs | |
| **74131** | quad 2-input AND gate buffer with 15 V open collector outputs | |
| **74132** | quad 2-input NAND schmitt trigger | |
| **74133** | 13-input NAND gate | |
| **74134** | 12-input NAND gate with three-state output | |
| **74135** | quad exclusive-or/NOR gate | |
| **74136** | quad 2-input XOR gate with open collector outputs | |
| **74137** | 3 to 8-line decoder/demultiplexer with address latch | |
| **74138** | 3 to 8-line decoder/demultiplexer | |
| **74139** | dual 2 to 4-line decoder/demultiplexer | |
| **74140** | dual 4-input NAND line driver | |
| **74141** | BCD to decimal decoder/driver for cold-cathode indicator/Nixie tube | |
| **74142** | decade counter/latch/decoder/driver for Nixie tubes | |
| **74143** | decade counter/latch/decoder/7-segment driver, 15 ma constant current | |
| **74144** | decade counter/latch/decoder/7-segment driver, 15 V open collector outputs | |
| **74145** | BCD to decimal decoder/driver | |
| **74147** | 10-line to 4-line priority encoder | |
| **74148** | 8-line to 3-line priority encoder | |
| **74150** | 16-line to 1-line data selector/multiplexer | |
| **74151** | 8-line to 1-line data selector/multiplexer | |
| **74152** | 8-line to 1-line data selector/multiplexer | |
| **74153** | dual 4-line to 1-line data selector/multiplexer | |

| | | |
|---|---|---|
| **74154** | 4-line to 16-line decoder/demultiplexer | |
| **74155** | dual 2-line to 4-line decoder/demultiplexer | |
| **74156** | dual 2-line to 4-line decoder/demultiplexer with open collector outputs | |
| **74157** | quad 2-line to 1-line data selector/multiplexer, noninverting | |
| **74158** | quad 2-line to 1-line data selector/multiplexer, inverting | |
| **74159** | 4-line to 16-line decoder/demultiplexer with open collector outputs | |
| **74160** | synchronous 4-bit decade counter with asynchronous clear | |
| **74161** | synchronous 4-bit binary counter with asynchronous clear | |
| **74162** | synchronous 4-bit decade counter with synchronous clear | |
| **74163** | synchronous 4-bit binary counter with synchronous clear | |
| **74164** | 8-bit parallel-out serial shift register with asynchronous clear | |
| **74165** | 8-bit serial shift register, parallel Load, complementary outputs | |
| **74166** | parallel-Load 8-bit shift register | |
| **74167** | synchronous decade rate multiplier | |
| **74168** | synchronous 4-bit up/down decade counter | |
| **74169** | synchronous 4-bit up/down binary counter | |
| **74170** | 4 by 4 register file with open collector outputs | |
| **74172** | 16-bit multiple port register file with three-state outputs | |
| **74173** | quad d flip-flop with three-state outputs | |
| **74174** | hex d flip-flop with common clear | |
| **74175** | quad d edge-triggered flip-flop with complementary outputs and asynchronous clear | |
| **74176** | presettable decade (bi-quinary) counter/latch | |
| **74177** | presettable binary counter/latch | |
| **74178** | 4-bit parallel-access shift register | |
| **74179** | 4-bit parallel-access shift register with asynchronous clear and complementary $Q_d$ outputs | |
| **74180** | 9-bit odd/even parity bit generator and checker | |
| **74181** | 4-bit arithmetic logic unit and function generator | |
| **74182** | lookahead carry generator | |
| **74183** | dual carry-save full adder | |
| **74184** | BCD to binary converter | |
| **74185** | 6-bit binary to BCD converter | |
| **74186** | 512-bit (64x8) read-only memory with open collector outputs | |
| **74187** | 1024-bit (256x4) read only memory with open collector outputs | |
| **74188** | 256-bit (32x8) programmable read-only memory with open collector outputs | |

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|---|---|---|
| **74189** | 64-bit (16x4) ram with inverting three-state outputs | |
| **74190** | synchronous up/down decade counter | |
| **74191** | synchronous up/down binary counter | |
| **74192** | synchronous up/down decade counter with clear | |
| **74193** | synchronous up/down binary counter with clear | |
| **74194** | 4-bit bidirectional universal shift register | |
| **74195** | 4-bit parallel-access shift register | |
| **74196** | presettable decade counter/latch | |
| **74197** | presettable binary counter/latch | |
| **74198** | 8-bit bidirectional universal shift register | |
| **74199** | 8-bit bidirectional universal shift register with J-Not-K serial inputs | |
| **74200** | 256-bit ram with three-state outputs | |
| **74201** | 256-bit (256x1) ram with three-state outputs | |
| **74206** | 256-bit ram with open collector outputs | |
| **74209** | 1024-bit (1024x1) ram with three-state output | |
| **74210** | octal buffer | |
| **74219** | 64-bit (16x4) ram with noninverting three-state outputs | |
| **74221** | dual monostable multivibrator with schmitt trigger input | |
| **74222** | 16 by 4 synchronous FIFO memory with three-state outputs | |
| **74224** | 16 by 4 synchronous FIFO memory with three-state outputs | |
| **74225** | asynchronous 16x5 FIFO memory | |
| **74226** | 4-bit parallel latched bus transceiver with three-state outputs | |
| **74230** | octal buffer/driver with three-state outputs | |
| **74232** | quad NOR Schmitt trigger | |
| **74237** | 1-of-8 decoder/demultiplexer with address latch, active high outputs | |
| **74238** | 1-of-8 decoder/demultiplexer, active high outputs | |
| **74239** | dual 2-of-4 decoder/demultiplexer, active high outputs | |
| **74240** | octal buffer with Inverted three-state outputs | |
| **74241** | octal buffer with noninverted three-state outputs | |
| **74242** | quad bus transceiver with Inverted three-state outputs | |
| **74243** | quad bus transceiver with noninverted three-state outputs | |
| **74244** | octal buffer with noninverted three-state outputs | |
| **74245** | octal bus transceiver with noninverted three-state outputs | |
| **74246** | BCD to 7-segment decoder/driver with 30 V open collector outputs | |
| **74247** | BCD to 7-segment decoder/driver with 15 V open collector outputs | |

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| **74248** | BCD to 7-segment decoder/driver with Internal Pull-up outputs | |
| **74249** | BCD to 7-segment decoder/driver with open collector outputs | |
| **74251** | 8-line to 1-line data selector/multiplexer with complementary three-state outputs | |
| **74253** | dual 4-line to 1-line data selector/multiplexer with three-state outputs | |
| **74255** | dual 4-bit addressable latch | |
| **74256** | dual 4-bit addressable latch | |
| **74257** | quad 2-line to 1-line data selector/multiplexer with noninverted three-state outputs | |
| **74258** | quad 2-line to 1-line data selector/multiplexer with Inverted three-state outputs | |
| **74259** | 8-bit addressable latch | |
| **74260** | dual 5-input NOR gate | |
| **74261** | 2-bit by 4-bit parallel binary multiplier | |
| **74265** | quad complementary output elements | |
| **74266** | quad 2-input XNOR gate with open collector outputs | |
| **74270** | 2048-bit (512x4) read only memory with open collector outputs | |
| **74271** | 2048-bit (256x8) read only memory with open collector outputs | |
| **74273** | 8-bit register with reset | |
| **74274** | 4-bit by 4-bit binary multiplier | |
| **74275** | 7-bit slice Wallace tree | |
| **74276** | quad J-Not-K edge-triggered Flip-Flops with separate clocks, common preset and clear | |
| **74278** | 4-bit cascadeable priority registers with latched data inputs | |
| **74279** | quad set-reset latch | |
| **74280** | 9-bit odd/even Parity bit Generator/checker | |
| **74281** | 4-bit parallel binary accumulator | |
| **74283** | 4-bit binary Full adder | |
| **74284** | 4-bit by 4-bit parallel binary multiplier (low order 4 bits of product) | |
| **74285** | 4-bit by 4-bit parallel binary multiplier (high order 4 bits of product) | |
| **74287** | 1024-bit (256x4) programmable read-only memory with three-state outputs | |
| **74288** | 256-bit (32x8) programmable read-only memory with three-state outputs | |
| **74289** | 64-bit (16x4) RAM with open collector outputs | |
| **74290** | decade counter (separate divide-by-2 and divide-by-5 sections) | |
| **74291** | 4-bit universal shift register, binary up/down counter, synchronous | |
| **74292** | programmable frequency divider/digital timer | |
| **74293** | 4-bit binary counter (separate divide-by-2 and divide-by-8 sections) | |
| **74294** | programmable frequency divider/digital timer | |

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|---|---|---|
| **74295** | 4-bit bidirectional register with three-state outputs | |
| **74297** | digital phase-locked-loop filter | |
| **74298** | quad 2-input multiplexer with storage | |
| **74299** | 8-bit bidirectional universal shift/storage register with three-state outputs | |
| **74301** | 256-bit (256x1) random access memory with open collector output | |
| **74309** | 1024-bit (1024x1) random access memory with open collector output | |
| **74310** | octal buffer with Schmitt trigger inputs | |
| **74314** | 1024-bit random access memory | |
| **74320** | crystal controlled oscillator | |
| **74322** | 8-bit shift register with sign extend, three-state outputs | |
| **74323** | 8-bit bidirectional universal shift/storage register with three-state outputs | |
| **74324** | voltage controlled oscillator (or crystal controlled) | |
| **74340** | octal buffer with Schmitt trigger inputs and three-state inverted outputs | |
| **74341** | octal buffer with Schmitt trigger inputs and three-state noninverted outputs | |
| **74344** | octal buffer with Schmitt trigger inputs and three-state noninverted outputs | |
| **74348** | 8 to 3-line priority encoder with three-state outputs | |
| **74350** | 4-bit shifter with three-state outputs | |
| **74351** | dual 8-line to 1-line data selectors/multiplexers with three-state outputs and 4 common data inputs | |
| **74352** | dual 4-line to 1-line data selectors/multiplexers with inverting outputs | |
| **74353** | dual 4-line to 1-line data selectors/multiplexers with inverting three-state outputs | |
| **74354** | 8 to 1-line data selector/multiplexer with transparent latch, three-state outputs | |
| **74356** | 8 to 1-line data selector/multiplexer with edge-triggered register, three-state outputs | |
| **74361** | bubble memory function timing generator | |
| **74362** | four-phase clock generator/driver | |
| **74363** | octal 3-state D-latches | |
| **74365** | hex buffer with noninverted three-state outputs | |
| **74366** | hex buffer with Inverted three-state outputs | |
| **74367** | hex buffer with noninverted three-state outputs | |
| **74368** | hex buffer with Inverted three-state outputs | |
| **74370** | 2048-bit (512x4) read-only memory with three-state outputs | |
| **74371** | 2048-bit (256x8) read-only memory with three-state outputs | |
| **74373** | octal transparent latch with three-state outputs | |
| **741G373** | single transparent latch with three-state output | |
| **74374** | octal register with three-state outputs | |

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| **741G374** | single d-type flip-flop with three-state output | |
| **74375** | quad bistable latch | |
| **74376** | quad J-Not-K flip-flop with common clock and common clear | |
| **74377** | 8-bit register with clock enable | |
| **74378** | 6-bit register with clock enable | |
| **74379** | 4-bit register with clock enable and complementary outputs | |
| **74380** | 8-bit multifunction register | |
| **74381** | 4-bit arithmetic logic unit/function generator with generate and propagate outputs | |
| **74382** | 4-bit arithmetic logic unit/function generator with ripple carry and overflow outputs | |
| **74385** | quad 4-bit adder/subtractor | |
| **74386** | quad 2-input XOR gate | |
| **74387** | 1024-bit (256x4) programmable read-only memory with open collector outputs | |
| **74388** | 4-bit register with standard and three-state outputs | |
| **74390** | dual 4-bit decade counter | |
| **74393** | dual 4-bit binary counter | |
| **74395** | 4-bit universal shift register with three-state outputs | |
| **74398** | quad 2-input mulitplexers with storage and complementary outputs | |
| **74399** | quad 2-input multiplexer with storage | |
| **74405** | 1 to 8 decoder, equivalent to Intel 8205, only found as UCY74S405 so might be non-TI number | |
| **74408** | 8-bit parity tree | |
| **74412** | multi-mode buffered 8-bit latches with three-state outputs and clear | |
| **74423** | dual retriggerable monostable multivibrator | |
| **74424** | two-phase clock generator/driver | |
| **74425** | quad gates with three-state outputs and active low enables | |
| **74426** | quad gates with three-state outputs and active high enables | |
| **74428** | system controller for 8080a | |
| **74438** | system controller for 8080a | |
| **74440** | quad tridirectional bus transceiver with noninverted open collector outputs | |
| **74441** | quad tridirectional bus transceiver with Inverted open collector outputs | |
| **74442** | quad tridirectional bus transceiver with noninverted three-state outputs | |
| **74443** | quad tridirectional bus transceiver with Inverted three-state outputs | |
| **74444** | quad tridirectional bus transceiver with Inverted and noninverted three-state outputs | |
| **74448** | quad tridirectional bus transceiver with Inverted and noninverted open collector outputs | |

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| **74450** | 16-to-1 multiplexer with complementary outputs | |
| **74451** | dual 8-to-1 multiplexer | |
| **74452** | dual decade counter, synchronous | |
| **74453** | dual binary counter, synchronous | |
| **74453** | quad 4-to-1 multiplexer | |
| **74454** | dual decade up/down counter, synchronous, preset input | |
| **74455** | dual binary up/down counter, synchronous, preset input | |
| **74456** | NBCD (Natural binary coded decimal) adder | |
| **74460** | bus transfer switch | |
| **74461** | 8-bit presettable binary counter with three-state outputs | |
| **74462** | fiber-optic link transmitter | |
| **74463** | fiber-optic link receiver | |
| **74465** | octal buffer with three-state outputs | |
| **74468** | dual mos-to-ttL level converter | |
| **74470** | 2048-bit (256x8) programmable read-only memory with open collector outputs | |
| **74471** | 2048-bit (256x8) programmable read-only memory with three-state outputs | |
| **74472** | programmable read-only memory with open collector outputs | |
| **74473** | programmable read-only memory with three-state outputs | |
| **74474** | programmable read-only memory with open collector outputs | |
| **74475** | programmable read-only memory with three-state outputs | |
| **74481** | 4-bit slice processor elements | |
| **74482** | 4-bit slice expandable control elements | |
| **74484** | BCD-to-binary converter | |
| **74485** | binary-to-BCD converter | |
| **74490** | dual decade counter | |
| **74491** | 10-bit binary up/down counter with limited preset and three-state outputs | |
| **74498** | 8-bit bidirectional shift register with parallel inputs and three-state outputs | |
| **74508** | 8-bit multiplier/divider | |
| **74520** | 8-bit comparator | |
| **74521** | 8-bit comparator | |
| **74526** | fuse programmable identity comparator, 16 bit | |
| **74527** | fuse programmable identity comparator, 8 bit + 4 bit conventional Identity comparator | |
| **74528** | fuse programmable Identity comparator, 12 bit | |
| **74531** | octal transparent latch with 32 ma three-state outputs | |

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| 74532 | octal register with 32 ma three-state outputs | |
| 74533 | octal transparent latch with inverting three-state Logic outputs | |
| 74534 | octal register with inverting three-state outputs | |
| 74535 | octal transparent latch with inverting three-state outputs | |
| 74536 | octal register with inverting 32 ma three-state outputs | |
| 74537 | BCD to decimal decoder with three-state outputs | |
| 74538 | 1 of 8 decoder with three-state outputs | |
| 74539 | dual 1 of 4 decoder with three-state outputs | |
| 74540 | inverting octal buffer with three-state outputs | |
| 74541 | non-inverting octal buffer with three-state outputs | HC/HCT |
| 74544 | non-inverting octal registered transceiver with three-state outputs | |
| 74558 | 8-bit by 8-bit multiplier with three-state outputs | |
| 74560 | 4-bit decade counter with three-state outputs | |
| 74561 | 4-bit binary counter with three-state outputs | |
| 74563 | 8-bit d-type transparent latch with inverting three-state outputs | |
| 74564 | 8-bit d-type edge-triggered register with inverting three-state outputs | |
| 74568 | decade up/down counter with three-state outputs | |
| 74569 | binary up/down counter with three-state outputs | |
| 74573 | octal D-type transparent latch with three-state outputs | |
| 74574 | octal D-type edge-triggered flip-flop with three-state outputs | |
| 74575 | octal D-type flip-flop with synchronous clear, three-state outputs | |
| 74576 | octal D-type flip-flop with inverting three-state outputs | |
| 74577 | octal D-type flip-flop with synchronous clear, inverting three-state outputs | |
| 74580 | octal transceiver/latch with inverting three-state outputs | |
| 74589 | 8-bit shift register with input latch, three-state outputs | |
| 74590 | 8-bit binary counter with output registers and three-state outputs | |
| 74592 | 8-bit binary counter with input registers | |
| 74593 | 8-bit binary counter with input registers and three-state outputs | |
| 74594 | serial-in shift register with output registers | |
| 74595 | serial-in shift register with output latches | |
| 74596 | serial-in shift register with output registers and open collector outputs | |
| 74597 | serial-out shift register with input latches | |
| 74598 | shift register with input latches | |
| 74600 | dynamic memory refresh controller, transparent and burst modes, for 4K or 16K | |

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| | drams | |
| **74601** | dynamic memory refresh controller, transparent and burst modes, for 64K drams | |
| **74602** | dynamic memory refresh controller, cycle steal and burst modes, for 4K or 16K drams | |
| **74603** | dynamic memory refresh controller, cycle steal and burst modes, for 64K drams | |
| **74604** | octal 2-input multiplexer with latch, high-speed, with three-state outputs | |
| **74605** | latch, high-speed, with open collector outputs | |
| **74606** | octal 2-input multiplexer with latch, glitch-free, with three-state outputs | |
| **74607** | octal 2-input multiplexer with latch, glitch-free, with open collector outputs | |
| **74608** | memory cycle controller | |
| **74610** | memory mapper, latched, three-state outputs | |
| **74611** | memory mapper, latched, open collector outputs | |
| **74612** | memory mapper, three-state outputs | |
| **74613** | memory mapper, open collector outputs | |
| **74620** | octal bus transceiver, inverting, three-state outputs | |
| **74621** | octal bus transceiver, noninverting, open collector outputs | |
| **74622** | octal bus transceiver, inverting, open collector outputs | |
| **74623** | octal bus transceiver, noninverting, three-state outputs | |
| **74624** | voltage-controlled oscillator with enable control, range control, two-phase outputs | |
| **74625** | dual voltage-controlled oscillator with two-phase outputs | |
| **74626** | dual voltage-controlled oscillator with enable control, two-phase outputs | |
| **74627** | dual voltage-controlled oscillator | |
| **74628** | voltage-controlled oscillator with enable control, range control, external temperature compensation, and two-phase outputs | |
| **74629** | dual voltage-controlled oscillator with enable control, range control | |
| **74630** | 16-bit error detection and correction (EDAC) with three-state outputs | |
| **74631** | 16-bit error detection and correction with open collector outputs | |
| **74632** | 32-bit error detection and correction | |
| **74638** | octal bus transceiver with inverting three-state outputs | |
| **74639** | octal bus transceiver with noninverting three-state outputs | |
| **74640** | octal bus transceiver with inverting three-state outputs | |
| **74641** | octal bus transceiver with noninverting open collector outputs | |
| **74642** | octal bus transceiver with inverting open collector outputs | |
| **74643** | octal bus transceiver with mix of inverting and noninverting three-state outputs | |
| **74644** | octal bus transceiver with mix of inverting and noninverting open collector outputs | |

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| **74645** | octal bus transceiver | |
| **74646** | octal bus transceiver/latch/multiplexer with noninverting three-state outputs | |
| **74647** | octal bus transceiver/latch/multiplexer with noninverting open collector outputs | |
| **74648** | octal bus transceiver/latch/multiplexer with inverting three-state outputs | |
| **74649** | octal bus transceiver/latch/multiplexer with inverting open collector outputs | |
| **74651** | octal bus transceiver/register with inverting three-state outputs | |
| **74652** | octal bus transceiver/register with noninverting three-state outputs | |
| **74653** | octal bus transceiver/register with inverting three-state and open collector outputs | |
| **74654** | octal bus transceiver/register with noninverting three-state and open collector outputs | |
| **74658** | octal bus transceiver with Parity, inverting | |
| **74659** | octal bus transceiver with Parity, noninverting | |
| **74664** | octal bus transceiver with Parity, inverting | |
| **74665** | octal bus transceiver with Parity, noninverting | |
| **74668** | synchronous 4-bit decade Up/down counter | |
| **74669** | synchronous 4-bit binary Up/down counter | |
| **74670** | 4 by 4 register File with three-state outputs | |
| **74671** | 4-bit bidirectional shift register/latch /multiplexer with three-state outputs | |
| **74672** | 4-bit bidirectional shift register/latch/multiplexer with three-state outputs | |
| **74673** | 16-bit serial-in serial-out shift register with output storage registers, three-state outputs | |
| **74674** | 16-bit parallel-in serial-out shift register with three-state outputs | |
| **74677** | 16-bit address comparator with enable | |
| **74678** | 16-bit address comparator with latch | |
| **74679** | 12-bit address comparator with latch | |
| **74680** | 12-bit address comparator with enable | |
| **74681** | 4-bit parallel binary accumulator | |
| **74682** | 8-bit magnitude comparator | |
| **74683** | 8-bit magnitude comparator with open collector outputs | |
| **74684** | 8-bit magnitude comparator | |
| **74685** | 8-bit magnitude comparator with open collector outputs | |
| **74686** | 8-bit magnitude comparator with enable | |
| **74687** | 8-bit magnitude comparator with enable | |
| **74688** | 8-bit equality comparator | |
| **74689** | 8-bit magnitude comparator with open collector outputs | |

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| **74690** | three state outputs | |
| **74691** | 4-bit binary counter/latch/multiplexer with asynchronous reset, three-state outputs | |
| **74692** | 4-bit decimal counter/latch/multiplexer with synchronous reset, three-state outputs | |
| **74693** | 4-bit binary counter/latch/multiplexer with synchronous reset, three-state outputs | |
| **74694** | 4-bit decimal counter/latch/multiplexer with synchronous and asynchronous resets, three-state outputs | |
| **74695** | 4-bit binary counter/latch/multiplexer with synchronous and asynchronous resets, three-state outputs | |
| **74696** | 4-bit decimal counter/register/multiplexer with asynchronous reset, three-state outputs | |
| **74697** | 4-bit binary counter/register/multiplexer with asynchronous reset, three-state outputs | |
| **74698** | 4-bit decimal counter/register/multiplexer with synchronous reset, three-state outputs | |
| **74699** | 4-bit binary counter/register/multiplexer with synchronous reset, three-state outputs | |
| **74716** | programmable decade counter | |
| **74718** | programmable binary counter | |
| **74724** | voltage controlled multivibrator | |
| **74740** | octal buffer/Line driver, inverting, three-state outputs | |
| **74741** | octal buffer/Line driver, noninverting, three-state outputs, mixed enable polarity | |
| **74744** | octal buffer/Line driver, noninverting, three-state outputs | |
| **74748** | 8 to 3-line priority encoder | |
| **74779** | 8-bit bidirectional binary counter (3-state) | |
| **74783** | synchronous address multiplexer | |
| **74790** | error detection and correction (EDAC) | |
| **74794** | 8-bit register with readback | |
| **74795** | octal buffer with three-state outputs | |
| **74796** | octal buffer with three-state outputs | |
| **74797** | octal buffer with three-state outputs | |
| **74798** | octal buffer with three-state outputs | |
| **74804** | hex 2-input NAND drivers | |
| **74805** | hex 2-input NOR drivers | |
| **74808** | hex 2-input AND drivers | |
| **74832** | hex 2-input OR drivers | |
| **74848** | 8 to 3-line priority encoder with three-state outputs | |

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| **74873** | octal transparent latch | |
| **74874** | octal d-type flip-flop | |
| **74876** | octal d-type flip-flop with inverting outputs | |
| **74878** | dual 4-bit d-type flip-flop with synchronous clear, noninverting three-state outputs | |
| **74879** | dual 4-bit d-type flip-flop with synchronous clear, inverting three-state outputs | |
| **74880** | octal transparent latchwith inverting outputs | |
| **74881** | arithmetic logic unit | |
| **74882** | 32-bit lookahead carry generator | |
| **74888** | 8-bit slice processor | |
| **74901** | hex inverting TTL buffer | |
| **74902** | hex non-inverting TTL buffer | |
| **74903** | hex inverting CMOS buffer | |
| **74904** | hex non-inverting CMOS buffer | |
| **74905** | 12-Bit successive approximation register | |
| **74906** | hex open drain n-channel buffers | |
| **74907** | hex open drain p-channel buffers | |
| **74908** | dual CMOS 30 V relay driver | |
| **74909** | quad voltage comparator | |
| **74910** | 256x1 CMOS static RAM | |
| **74911** | 4 digit expandable display controller | |
| **74912** | 6 digit BCD display controller and driver | |
| **74914** | hex schmitt trigger with extended input voltage | |
| **74915** | seven segment to BCD decoder | |
| **74917** | 6 digit Hex display controller and driver | |
| **74918** | dual CMOS 30 V relay driver | |
| **74920** | 256x4 CMOS static RAM | |
| **74921** | 256x4 CMOS static RAM | |
| **74922** | 16-key encoder | |
| **74923** | 20-key encoder | |
| **74925** | 4-digit counter/display driver | |
| **74926** | 4-digit counter/display driver | |
| **74927** | 4-digit counter/display driver | |
| **74928** | 4-digit counter/display driver | |
| **74929** | 1024x1 CMOS static RAM | |
| **74930** | 1024x1 CMOS static RAM | |

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| **74932** | phase comparator | |
| **74933** | address bus comparator | |
| **74934** | =ADC0829 ADC, see corresponding NSC datasheet | |
| **74935** | 3.5-digit digital voltmeter (DVM) support chip for multiplexed 7-segment displays | |
| **74936** | 3.75-digit digital voltmeter (DVM) support chip for multiplexed 7-segment displays | |
| **74937** | =ADC3511 ADC, see corresponding NSC datasheet | |
| **74938** | =ADC3711 ADC, see corresponding NSC datasheet | |
| **74941** | octal bus/line drivers/line receivers | |
| **74945** | 4 digit up/down counter with decoder and driver | |
| **74947** | 4 digit up/down counter with decoder and driver | |
| **74948** | =ADC0816 ADC, see corresponding NSC datasheet | |
| **74949** | =ADC0808 ADC, see corresponding NSC datasheet | |
| **74949** | =ADC0808 ADC, see corresponding NSC datasheet | |
| **741005** | hex inverting buffer with open-collector output | |
| **741035** | hex noninverting buffers with open-collector outputs | |
| **742960** | error detection and correction (EDAC) | |
| **742961** | edac bus buffer, inverting | |
| **742962** | edac bus buffer, noninverting | |
| **742968** | dynamic memory controller | |
| **742969** | memory timing controller for use with EDAC | |
| **742970** | memory timing controller for use without EDAC | |
| **741G3208** | single 3 input OR-AND Gate; | |
| **744002** | dual 4-input NOR gate | |
| **744015** | dual 4-bit shift registers | |
| **744017** | 5-stage ÷10 Johnson counter | |
| **744020** | 14-stage binary counter | |
| **744024** | 7 stage ripple carry binary counter | |
| **744028** | BCD to decimal decoder | |
| **744040** | 12-stage binary ripple counter | |
| **744046** | phase-locked loop and voltage-controlled oscillator | |
| **744049** | hex inverting buffer | |
| **744050** | hex buffer/converter (non-inverting) | |
| **744051** | high-speed CMOS 8-channel analog mulitplexer/demultiplexer | |
| **744052** | dual 4-channel analog multiplexer/demultiplexers | |
| **744053** | triple 2-channel analog multiplexer/demultiplexers | |

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| **744059** | programmable divide-by-N counter | |
| **744060** | 14-stage binary ripple counter with oscillator | |
| **744066** | quad bilateral switches | |
| **744067** | 16-channel analog multiplexer/demultiplexer | |
| **744075** | triple 3-input OR gate | |
| **744078** | 8-input OR/NOR gate | |
| **744094** | 8-bit three-state shift register/latch | |
| **744316** | quad analog switch | |
| **744511** | BCD to 7-segment decoder | |
| **744520** | dual 4-bit synchronous binary counter | |
| **744538** | dual re-triggerable precision monostable  multivibrator | |
| **747007** | hex buffer | |
| **747266** | quad 2-input XNOR gate | |
| **7429841** | 10-bit bus-interface D-type latch with 3-state outputs | |
| **7440103** | Pre-settable 8-bit synchronous down counter | |
| **7440105** | 4-bit by 16-word FIFO register | |