Graphene: Its Fundamentals to Future Applications

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(Invited Paper)

***Abstract*—Currently, graphene is a topic of very active research fields from science to potential applications. For various RF circuit applications, including low-noise amplifiers, the unique ambipolar nature of graphene field-effect-transistors can be utilized for high-performance frequency multipliers, mixers, and high-speed radiometers. Potential integration of graphene on silicon substrates with CMOS compatibility would also benefit future RF systems. The future success of the RF circuit applications depends on vertical and lateral scaling of graphene MOSFETs to minimize parasitics and improve gate modulation efficiency in the channel with zero or a small bandgap. In this paper, we highlight recent progress in graphene materials, devices, and circuits for RF applications. For passive RF applications, we show its transparent electromagnetic shielding in Ku-band and transparent antennas, where its success depends on the quality of materials. We also attempt to discuss future applications and challenges of graphene.**

***Index Terms*—Ambipolar, antenna, CMOS, electromagnetic interference (EMI), field-effect transistor (FET), graphene, interconnects, low-noise amplifier (LNA), mixer, multiplier, nanoelectromechanical systems (NEMS), phase noise, radiometer, RF, sensors, transistor.**

I. Introduction

GRAPHENE IS an atomically thin, but stable form of hexagonal carbon [1], [2] and has attracted a lot of attention in the research community since the seminal papers published in 2004 [3], [4]. Along with its unique electronic properties, graphene has shown interesting optical [5], mechanical [6], and thermal [7] properties, as summarized in Table I. Some of these unique properties have been considered for potential applications such as transparent conductors for touch screens [8], [9] electromagnetic interference (EMI) shielding [10], antennas [11], flexible electronics [12], sensors [13], nanoelectromechanical systems (NEMS) [14], and interconnects [15].

For RF electronic applications considered, graphene exhibits the highest carrier mobility: $> 100\,000$ cm^2 V^{-1} $\cdot$ s^{-1} at room temperature [16]. This is not only $\sim$100 times greater than that of Si, but about ten times greater than state-of-the-art (SOA) semiconductors lattice matched to InP, currently regarded the best high-speed materials. The saturation velocity $(v_{\rm sat})$ of graphene has not been determined clearly yet, but it is estimated to be $\sim$5 times greater than that for Si MOSFETs [17]. With expected large on-state current density and transconductance per gate capacitance compared to Si, graphene has the potential to offer excellent switching characteristics (capacitance/on-state current) and short-circuit current gain cutoff frequency [18]. The atomically thin 2-D graphene channel layer provides, in principle, a path for ultimate vertical scaling of transistors minimizing the short channel effect. Although it is too early to predict, graphene-on-Si field-effect transistors (FETs) [19] could potentially be further developed and processed in a manner compatible with Si CMOS with desirable integration density for system-on-chip applications. While there are numerous challenges to be overcome for graphene to become a mature technology, this material offers unique device and potential circuit applications ranging from conventional unipolar RF electronics such as low-noise amplifiers (LNAs) to unique ambipolar RF electronics such as frequency multipliers, mixers, and high-speed radiometers. With observed constant device transconductance over the gate voltages [20], graphene FETs could potentially offer LNAs with higher dynamic range per given dc power, i.e., output third-order intercept point (OIP3) per given dc power, beyond the antimony-based low-bandgap devices. With graphene FETs biased near the ambipolar point, graphene FETs behave close to ideal "square-law" devices near the ambipolar point, i.e., $I(V_{\rm gs}) \propto V_{\rm gs}^2$, where $V_{\rm gs}$ is the gate voltage. It would greatly suppress odd-order harmonics and/or third-order intermodulation products and improve dynamic range in communications.

TABLE I
Brief Summary of Intrinsic Properties of Graphene

Saturation Velocity (cm/Sec)	4-5 x 10^7
Carrier mobility (cm^2/Vs)	> 100,000
Current density (A/cm^2)	~10^9
Thermal Conductivity (W/m-K)	4800
Optical opacity (%)	2.3% per layer
Young's modulus (Pa)	0.5-1 tera

II. Status of Epitaxial Graphene Transistors

Graphene FETs are being developed on the wafer-scale utilizing graphene-on-Si [19], [21], graphene-on-SiC [20], [22]–[24], and graphene transferred to SiO2 substrates [25]. Several promising device parameters have been demonstrated.

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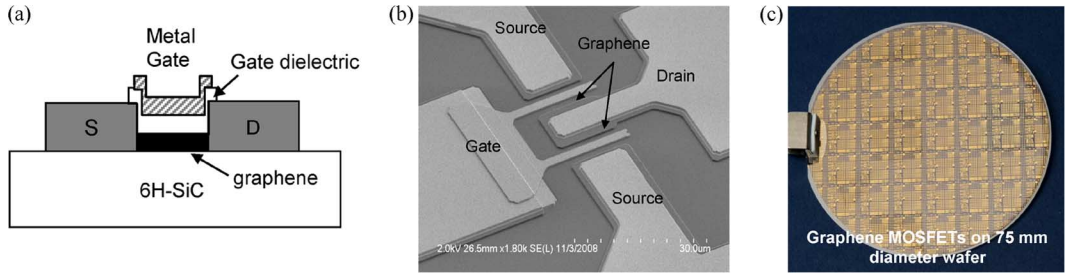

Fig. 1. (a) Schematic of the top-gated graphene FET. (b) SEM photograph of $2f \times 4\ \mu$m graphene FET. (c) Photograph of 75-mm graphene wafer.

For example, epitaxial graphene RF FETs have been demonstrated in a top-gated layout with the highest ever on-state current density of 3 A/mm [24]. On the other hand, the current–voltage characteristics are quasi-linear with weak saturation behaviors, yielding low transconductance (gm) per capacitance (i.e., <140 mS/mm at 3.4 fF/μm^2). It leads to a poor voltage gain defined by $gm/G_{\rm ds}$, where $G_{\rm ds}$ is the output conductance. The ratio of the on-state current $(I_{\rm on})$ over the off-state current $(I_{\rm off})$ $I_{\rm on}/I_{\rm off}$ ratio was also ~4 with field-effect mobility $(\mu_{\rm FE})$ below 200 cm^2/V $\cdot$ s. While graphene field-effect mobility as high as 5400 cm^2/V $\cdot$ s for the electron has been demonstrated [22], it was achieved using 6–7 layers of epitaxial graphene on C-face SiC substrates, resulting in an $I_{\rm on}/I_{\rm off}$ ratio of <2. In the case of graphene FETs fabricated on the Si face of SiC substrates, field-effect mobility has been limited to below 1200 cm^2/V $\cdot$ s, but with an improved $I_{\rm on}/I_{\rm off}$ ratio of ~10 [23].

In [20], top-gated graphene n-FETs and p-FETs from epitaxial graphene layers were demonstrated with improved *I–V* saturation behaviors with a record peak extrinsic transconductance of 770 mS/mm. The epitaxial graphene layers were grown on Si-face 6H-SiC substrates on 75-mm wafers via Si sublimation [26]. The sheet electron carrier density of the epitaxial graphene layer was typically 8.8×10^{12} cm^{-2} at room temperature and had electron mobility of ~ 1192 cm^2/V $\cdot$ s, characterized by noncontact Hall Lehighton 1600. The number of epitaxial graphene layers (nGLs) was found to be one layer on the SiC terraces and two layers on the step edges over the entire 75-mm wafer, as characterized by Raman analysis and transmission electron microscopy analysis.

Fig. 1(a)–(c) shows the graphene FET processed in a layout, where the gate metal is aligned with respect to the ohmic metals in an under lap layout with a gate-to-source/drain separation of <100 nm to minimize the access resistance over a source–drain spacing $(L_{\rm sd})$ of 3 μm. The source access resistance was measured < 0.2 $\Omega \cdot$ mm with the standard end-point measurements using a transfer length method (TLM) structure. Recent TLM shows the ohmic contact resistance below 0.1 $\Omega \cdot$ mm, which is comparable to that of SOA high-speed III–V FETs [27]. A graphene channel width of 4 μm was defined by O_2 plasma etching.

Fig. 2(a) and (b) shows measured room-temperature common-source current–voltage characteristics of a two-gatefinger and 4-μm-wide n-channel graphene FET (denoted as $2f \times 4\ \mu$m), in which excellent drain current saturation was observed. The source-to-drain voltage $(V_{\rm ds})$ increased

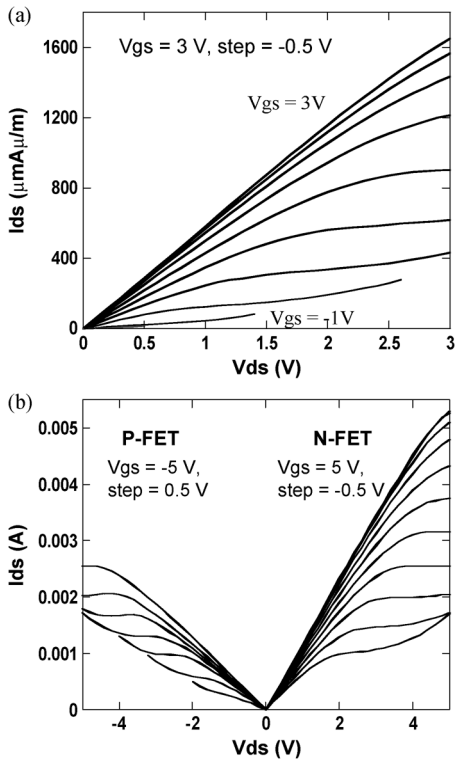

Fig. 2. (a) Measured common-source current–voltage characteristics of $1f \times 4\ \mu$m graphene FET. (b) Both p- and n-channel graphene MOSFET operations.

to 3 V, where the gate-to-source $(V_{\rm gs})$ voltage was stepped from 3 V (top curve) in steps of -0.5 V. At $V{\rm ds} = 1$ V, the maximum current at $V_{\rm gs} = 3$ V was 0.59 A/mm. The minimum current was 0.047 A/mm at $V{\rm gs} = -1$ V, yielding an $I_{\rm max}/I_{\rm min}$ ratio of 13. At $V_{\rm ds} = 0.5$ V, the $I_{\rm on}/I_{\rm off}$ ratio increased to 20 with the on-state current of 0.31 A/mm. At $V{\rm ds} = 3$ V, the on-state current at $V{\rm gs} = 3$ V was measured as high as 1.65 A/mm. The on-resistance was 1.6 $\Omega \cdot$mm. The peak extrinsic gm of 770 mS/mm was measured at $V{\rm ds} = 3.05$ V, which is the highest ever amongst epitaxial graphene FETs. Fig. 3 shows extracted effective mobility $(\mu_{\rm eff})$ and field-effect mobility of graphene n-FETs versus the effective electric field $E_{\rm eff}$. In comparison, the universal and field-effect mobility of Si n-MOSFETs [28] and strained Si n-MOSFETs on SiGe-on-oxide [29] are shown. While both the $\mu_{\rm eff}$ and $\mu_{\rm FE}$ of the graphene n-FETs depend on $E_{\rm eff}$, both values were higher than 1000 cm^2/V $\cdot$ s over a wide range of the effective electric field up to 1.6 MV/cm. The peak field-effect

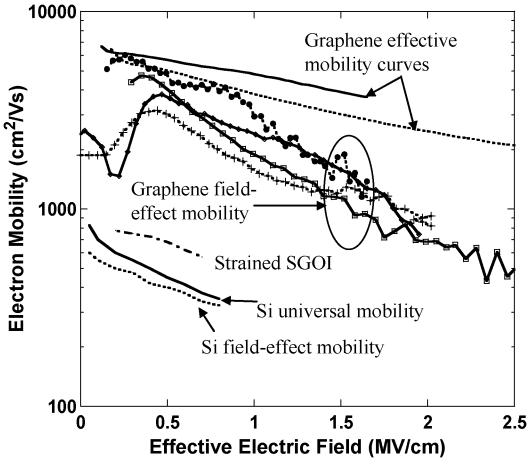

Fig. 3. Measured effective carrier mobility and field-effect mobility of graphene n-FETs compared with those of Si n-MOSFET and strained Si on SiGe-on-insulator (SGOI) MOSFET.

mobility values ranged from 3200 to 6000 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. A record field-effect mobility of 6000 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ was obtained at an effective electric field of 0.27 MV/cm. The measured field-effect mobility of graphene n-FETs was at least seven times higher than that of ITRS Si n-MOSFETs and ∼80 times higher than ultra-thin-body silicon-on-insulator (SOI) n-MOSFETs. The peak field-effect mobility of graphene p-FETs was also determined to be 3200 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ at an effective electric field of 0.2 MV/cm.

While graphene provides both n- and p-channel FETs with high field-effect mobilities and high transconductance, the graphene FETs are not fully pinched off due to their zero-bandgap nature. This leads to a very high subthreshold current. The observed high output conductance or low output resistance (R_{ds}) also results in a voltage gain on the order of 1. The bandgap engineering of graphene channels is necessary to further improve dc *I–V* characteristics with full saturation characteristics, as the graphene devices are developed with short-channel layouts. The bandgap of graphene channels can be opened up to ∼0.2 eV. Its saturation velocity can be reduced to $\sim 2.5 \times 10^7$ cm/s from 4.5×10^7 cm/s in the case of the zero-bandgap graphene channel.

III. Graphene FET RF Performance

The RF performance of graphene FETs has improved over the last several years. In 2009, an extrinsic cutoff frequency (f_T) and an extrinsic maximum oscillation frequency (f_{MAX}) of 4.2 and 14 GHz were reported with a 2-μm gate length (L_g) [24]. The speed performance was not optimized due to the overlap capacitance between the gate and ohmic metal pads. In 2010, graphene FETs with a 240-nm gate length were reported with de-embedded f_T/f_{MAX} of 100 GHz/10 GHz, while no extrinsic f_T/f_{MAX} prior to the de-embedding were reported [30]. With graphene FETs processed with self-aligned nanowire gate with a gate length of 140 nm, de-embedded f_t of 300 GHz was claimed while the extrinsic f_T of 2.4 GHz was measured [31].

As an example of graphene FET RF performance, Fig. 4(a) shows measured $|H_{21}|$ and unilateral gain (U) of the 2×12 μm graphene FETs with source–drain spacing (L_{sd}) of 1 μm. The

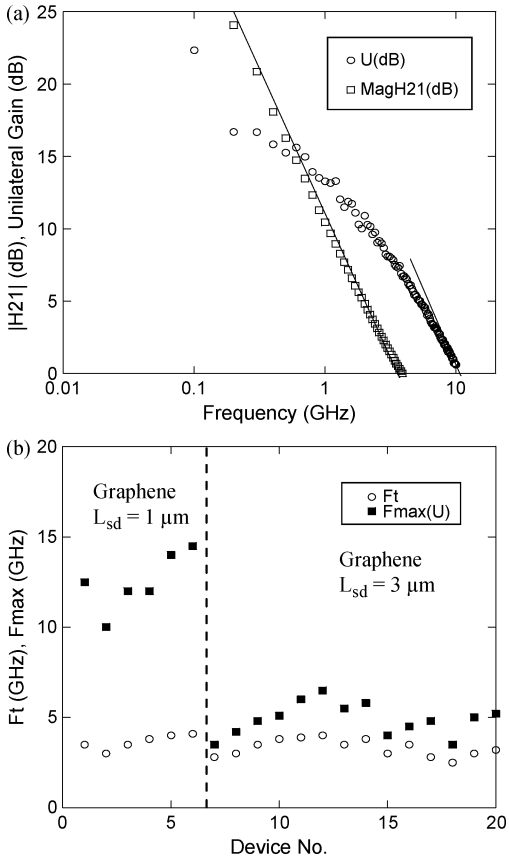

Fig. 4. (a) Measured extrinsic $|H_{21}|$ and unilateral gain (U) are shown as a function of frequencies at $V\mathrm{ds} = 5$ V and $V\mathrm{gs} = -2.5$ V of 2×12 μm graphene MOSFETs with $L\mathrm{ds} = 1$ μm. (b) Plot of measured extrinsic f_T and f_{max} of the graphene FETs is shown. The gate length is 2 μm. The highest f_T and f_{max} are 4.2 and 14 GHz, respectively.

S-parameters were measured at $V_{\mathrm{ds}} = 5$ V and $V\mathrm{gs} = -2.5$ V. An extrinsic cutoff frequency (f_T) of 4.1 GHz was extracted, yielding an extrinsic $f_T \cdot L_g$ of 8.2 GHz $\cdot$ μm. The extrinsic gm was 195 mS/mm. A maximum oscillation frequency (f_{MAX}) of 11.5 GHz was extracted from the Mason's unilateral gain (U) with a slope of -20 dB/decade. Fig. 4(b) shows a plot of extrinsic f_T and f_{MAX} measured from the graphene FETs. For a graphene FET with $L_{\mathrm{sd}} = 3$ μm, the extrinsic gm improved to 148 mS/mm at $V\mathrm{ds} = 9$ V, yielding the extrinsic f_T and f_{MAX} of 4.4 and 6 GHz, respectively. For a graphene FET with $L_{\mathrm{sd}} = 1$ μm, the f_T and f_{MAX} were 4.2 and 14 GHz, respectively, at $V\mathrm{ds} = 7$ V. With a source access resistance of 1.9 $\Omega \cdot$ mm, the intrinsic gm becomes 205 mS/mm. This yields an intrinsic f_T of 5 GHz with an intrinsic $f_T \cdot L_g$ of 10 GHz $\cdot$ μm, which is slightly better than 8.9 GHz $\cdot$ μm from the bulk Si NMOS.

Currently, the RF performance of graphene FETs has not come close to what was predicted by the intrinsic saturation velocity of the graphene channel $(4.5 \times 10^7$ cm/s) or the predicted ballistic transport velocity of 5×10^7 cm/s. The theoretical carrier transport velocity provides an $f_T \cdot L_g$ product > 50 GHz $\cdot$ μm, which is far from the currently observed values of $f_T \cdot L_g$ products. While graphene FETs are laterally scaled with a smaller channel length [30], the ohmic contact resistance should be further improved below 0.1 $\Omega \cdot$ mm to be comparable to SOA high-speed HEMT devices. Vertical scaling of

the gate dielectric has been difficult due to a poor nucleation of high-k films using an atomic layer deposition [32]. In addition, there are several aspects of current graphene FETs to be improved including: 1) relatively high channel resistance of 500 to 1000 Ω/sq; 2) channel mobility and carrier velocity degradation due to acoustic phonon scattering and optical phonons from the gate dielectrics; and 3) traps in the gate dielectrics and defects in the graphene channels. The total transit delay (τ) of graphene FETs is given by

$$\tau = \frac{(C_{\rm gs}+C_{\rm gd})}{gm} + \frac{(C_{\rm gs}+C_{\rm gd})\cdot(R_s+R_d)}{gm\cdot R_{\rm ds}} + C_{\rm gd}\cdot(R_s+R_d)$$

where $C_{\rm gs}$ and $C_{\rm gd}$ are gate-to-source and gate-to-drain capacitance, respectively. R_s and R_d are source and drain access resistance, respectively, which consist of both ohmic contact resistance and channel resistance. The ohmic contact resistance to epitaxial graphene wafers has been improved to $\sim 0.1\ \Omega\cdot$mm [27]. The extrinsic cutoff frequency is expected to improve as the quality of the epitaxial graphene layer, gate dielectric layer, transconductance, and transistor fabrication processing improve with reduced parasitic charging delay such as $(Rs+Rd)*C{\rm gd}$ [33]. In most RF applications, $f_{\rm MAX}$ is very important to provide amplifiers with gain. The formula for $f_{\rm MAX}$ is shown as follows:

$$f_{\rm MAX} = \frac{f_T/2}{\sqrt{(R_g+R_i+R_S)/R_{\rm ds}+2\pi R_g C_{\rm gd} f_T}}.$$

Thus far, the reported extrinsic $f_{\rm MAX}$ values of reported graphene FETs have been below 20 GHz. The weak *I–V* saturation leads to a smaller output resistance $(R_{\rm ds})$, transconductance, and higher $C_{\rm gd}$ compared to other semiconductor FETs with a finite bandgap. In order to maintain high $f_{\rm MAX}$ in short-channel graphene FETs, channel engineering to reduce band-to-band tunneling will be desired [34], as demonstrated, for instance, with graphene nanoribbon FETs [35].

IV. Graphene FET Ambipolar RF Applications

Unlike Si, SiGe, and III–IV semiconductor materials, graphene has a unique ambipolar characteristic, where excellent field-effect mobility for both electron and holes can be obtained. For instance, field-effect mobility of 6000 cm^2/V $\cdot$ s for electrons and 3200 cm^2/V $\cdot$ s for holes was obtained [20]. Several potential applications for these unique ambipolar graphene FETs have been under evaluation [36]–[40]. These include frequency multipliers, mixers, radiometer, and oscillators. Frequency multiplication or mixing is based on the nonlinearity of graphene FETs near the ambipolar point. If graphene FETs behave as ideal "square-law" devices near the ambipolar point, i.e., $I(V_g) \propto V_g^2$, it would greatly suppress odd-order harmonics and/or third-order intermodulation products and improve dynamic range in communications. A suppression of odd-order signals $(f, 3f, 5f, \ldots)$ compared to the second harmonic $(2f)$ was shown in the frequency multiplication experiments up to 200 kHz with $\sim$10-dB suppression [36][37], and above gigahertz [38].

Fig. 5(a) shows a schematic of the frequency multiplication process in the case of the ambipolar transfer curve. Fig. 5(b) shows measured transfer curves of $2f \times 25\ \mu$m graphene FETs with the Dirac point at $V_{\rm gs} = -1.4$ V. The inset to Fig. 5(b) shows measured RF output spectra consisting of strong even-order harmonic signals with odd-order harmonics suppressed by $>$25 dB, supporting "square-law" device operation at the ambipolar point. The phase-noise measurement was reported with a carrier-to-noise degradation $(\Delta{\rm CNR})$ of 6 dB, which implies noiseless frequency multiplication without additional $1/f$ noise up-conversion during the nonlinear process [38]. Capitalizing on the ambipolar nature of graphene FETs, ambipolar mixers were demonstrated in the gigahertz range [39], [40]. The conversion loss is typically in the order of 20–30 dB, which has to be solved in order to make ambipolar frequency doublers and mixers competitive technologies.

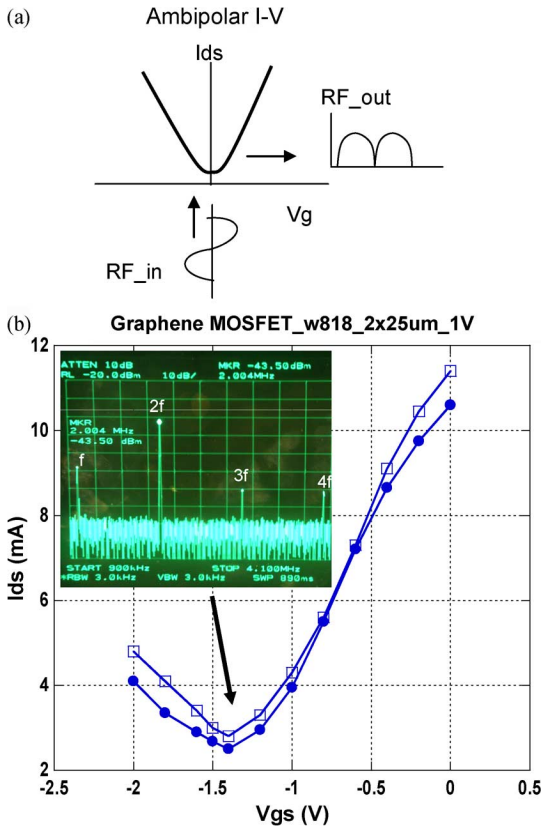

Fig. 5. (a) Schematic of frequency multiplication process is shown with RF output spectra consisting of even-order harmonic signals only. (b) Measured transfer curves of two $2f \times 25\ \mu$m graphene FETs at $V{\rm ds} = 1$ V is shown with the ambipolar point at $V{\rm gs} = -1.5$ V. Output spectra of the graphene FETs driven under the $1f = 1$ MHz, 0-dBm RF input signal are shown at the ambipolar point.

V. Graphene LNAs

In order to achieve high sensitivity of the signal of interest in heavily RF cluttered environments, high-sensitivity and high dynamic-range LNAs with low intermodulation distortion of incoming RF signals are highly desired. In general, for the receiver chain, the high linearity or OIP3 is achieved with high dc power dissipation and increased overhead on system cooling. Table II shows a comparison of broadband and linear LNAs [41]–[46] with different transistor technologies in terms of the LNA linearity figure of merit (OIP3/$P{\rm dc}$). In general, the lower bandgap

TABLE II
COMPARISON OF BROADBAND AND LINEAR LNAs

Technology	Bandwidth (GHz)	NF (dB)	Gain/DC power (mW)	OIP3/Pdc per LNA stage
90 nm CMOS	0.5-6.2	2.1-3.1	24.4/42	3.7
InP HEMT	4-12	1.3	28/41	NA
InSb HEMT	0.3-11	0.9-2.6	30/7.5	<1
MESFET	6-12	~5	8/692	8-24
GaAs HBT	5-11	NA	7.5/158	14
InP HBT	44-50	NA	5.5/120	21
Graphene	Graphene as delta-doped FETs with high mobility channel			

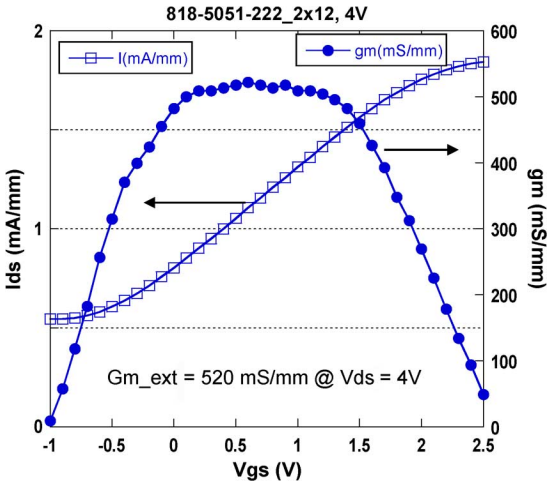

Fig. 6. Measured extrinsic transconductance curve of graphene FETs is shown at $V\mathrm{ds} = 4$ V, showing linear *I–V* (constant gm).

semiconductor such as InSb-based HEMTs offer LNAs with reduced power dissipation and the lattice matched InP HEMTs offer excellent noise figure (NF). The doped channel transistors such as MESFET and HBTs offer far superior LNA linearity figure of merit, OIP3/Pdc. For FETs, the OIP3 can be derived as $\mathrm{OIP3} \approx (gm^3/gm'') \cdot G_p$, where gm'' is the second derivative of gm, and G_p is the power gain. The gm linearity and high gm value is a key to improve OIP3 in high-performance FET-based LNAs. We have further investigated gm of graphene FETs. Fig. 6 shows a recently demonstrated gm linearity of graphene MOSFETs with a constant gm value as high as 520 mS/mm [27]. It would be interesting to see if graphene FETs, as viewed as delta-doped FETs, could potentially offer LNAs with higher dynamic range per given dc power beyond the antimony-based low-bandgap devices.

VI. GRAPHENE FOR PASSIVE RF APPLICATIONS

With excellent optical transparency, conductivity, and in-plane thermal conductivity, graphene can be used for passive RF components such as interconnects [47], heat spreaders [48],

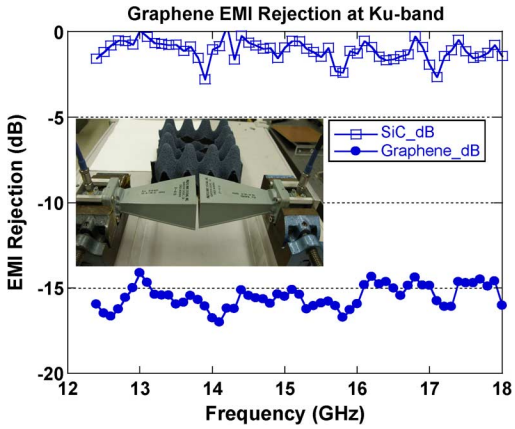

Fig. 7. Ku-band RF rejection of a few layers of graphene is shown.

transparent antennas [11], and RF/EMI shielding. Fig. 7 shows RF rejection through a few layers of epitaxial graphene at 12–18 GHz. An average of 15-dB rejection was demonstrated with >70% visible transparency.

VII. CONCLUSION

While it is in the early stage of development to clearly forecast its impact, graphene FETs could potentially offer performance benefits in RF systems including LNAs, frequency multipliers, mixers, and high-speed radiometers. The future success of the RF circuit applications depends on high-quality material growth on large-wafer scale, vertical and lateral scaling of graphene MOSFETs to minimize parasitics and improved gate modulation efficiency in the channel, a bandgap engineering of graphene channels in the MOSFETs, and innovative circuit concepts. It would very interesting to see if graphene microwave and millimeter-wave FETs would be integrated onto Si substrates or in 3-D integrated stacks.

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REFERENCES

[1] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Mater.*, vol. 6, pp. 183–191, 2007.
[2] N. P. Guisinger and M. S. Arnold, "Beyond silicon: Carbon-based nanotechnology," *MRS Bull.*, vol. 35, pp. 281–321, Apr. 2010.
[3] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, pp. 666–669, 2004.
[4] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Ultrathin epitaxial graphite: 2-D electron gas properties and a route toward graphene-based nanoelectronics," *J. Phys. Chem. B*, vol. 108, pp. 19912–19916, 2004.
[5] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, and A. K. Geim, "Fine structure constant defines visual transpreancy of graphene," *Science*, vol. 320, p. 1308, 2008.

[6] C. Lee, X. Wei, J. W. Kysar, and J. Hone, "Measurement of the elastic properties and intrinsic strength of monolayer graphene," *Science*, vol. 321, pp. 385–388, 2008.
[7] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Lett.*, vol. 8, pp. 902–907, 2008.
[8] S. Bae, H. K. Kim, X. Xu, J. Balakrishnan, T. Lei, Y. I. Song, Y. J. Kim, B. Ozyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," *Nature Nanotech.*, vol. 5, pp. 574–578, 2010.
[9] K. S. Kim *et al.*, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature*, vol. 457, pp. 706–710, 2009.
[10] J. S. Moon, unpublished.
[11] J. M. Jornet and I. F. Akyildiz, "Graphene-based nano-antennas for electromagnetic nanocommunications in the terahertz band," in *Proc. 4th Eur. Antennas Propag. Conf.*, 2010, pp. 1–5.
[12] G. Eda, G. Fanchini, and M. Chhowalla, "Large-area ultrathin films of reduced graphene oxide as a transparent and flexible electronic material," *Nature Nanotechnol.*, vol. 3, pp. 270–274, 2008.
[13] F. Schedin, A. K. Geim, S. V. Morozov, E. W. Hill, P. Blake, M. I. Katsnelson, and K. S. Novoselov, "Detection of individual gas molecules adsorbed on graphene," *Nature Mater.*, vol. 6, pp. 652–655, 2007.
[14] J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, and P. McEuen, "Electromechanical resonators from graphene sheets," *Science*, vol. 315, pp. 490–493, 2007.
[15] R. Murali, K. Brenner, Y. Yang, T. Beck, and J. D. Meindl, "Resistivity of graphene nanoribbon interconnects," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 611–613, Jun. 2009.
[16] S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, "Giant intrinsic carrier mobilities in graphene and its bilayer," *Phys. Rev. Lett.*, vol. 100, pp. 16602–16604, 2008.
[17] A. Akturk and N. Goldsman, "Electron transport and fullband electron-phonon interactions in graphene," *J. Appl. Phys.*, vol. 103, 2008, Art. ID 053702.
[18] J. S. Moon, D. Curtis, M. Hu, D. Wong, P. M. Campbell, G. Jernigan, J. Tedesco, B. VanMil, R. Myers-Ward, C. Eddy, Jr., D. K. Gaskill, J. Robinson, M. Fanton, and P. Asbeck, "Development toward wafer-scale graphene electronics," in *1st Int. Graphene and Emerging Mater. for Post-CMOS Appl. in 215th Electrochem. Soc. Meeting Symp.*, 2009, pp. 35–40.
[19] J. S. Moon, D. Curtis, S. Bui, T. Marshall, D. Wheeler, I. Valels, S. Kim, E. Wang, X. Weng, and M. Fanton, "Top-gated graphene FETs on using graphene on silicon (111) wafers," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1193–1195, Nov. 2010.
[20] J. S. Moon, D. Curtis, S. Bui, M. Hu, D. K. Gaskill, J. L. Tedesco, P. Asbeck, G. G. Jernigan, B. VanMil, R. Myers-Ward, C. Eddy, Jr., and P. M. Campbell, "Top-gated epitaxial graphene FETs on Si-face SiC wafers with a peak transconductance of 600 mS/mm," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 260–262, Apr. 2010.
[21] H.-C. Kang, H. Karasawa, Y. Miyamoto, H. Handa, H. Fukidome, T. Suemitsu, M. Suemitsu, and T. Otsuji, "Epitaxial graphene top-gate FETs on silicon substrates," in *Int. Semicond. Device Res. Symp.*, 2009, pp. 1–2.
[22] Y. Q. Wu, P. D. Ye, M. A. Capano, Y. Xuan, Y. Sui, M. Qi, J. A. Cooper, T. Shen, D. Pandey, G. Prakash, and R. Reifenberger, "Top-gated graphene field-effect transistors formed by decomposition of SiC," *Appl. Phys. Lett.*, vol. 92, 2008, Art. ID 092102.
[23] J. Kedzierski, P.-L. Hsu, P. Healey, P. W. Wyatt, C. L. Keast, M. Sprinkle, C. Berger, and W. A. de Heer, "Epitaxial graphene transistors on SiC substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2078–2085, Aug. 2008.
[24] J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P. M. Campbell, G. Jernigan, J. Tedesco, B. VanMil, R. Myers-Ward, C. Eddy, Jr., and D. K. Gaskill, "Epitaxial graphene RF field-effect transistors on Si-face 6H-SiC substrates," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 650–652, Jun. 2009.
[25] J. Kedzierski, P.-L. Hsu, A. Reina, J. Kong, P. Healey, P. Wyatt, and C. Keast, "Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 745–747, Jul. 2009.
[26] D. K. Gaskill, G. Jernigan, P. Campbell, J. L. Tedesco, and J. S. Moon, "Epitaxial graphene growth on SiC wafers," *ECS Trans.*, vol. 19, pp. 117–124, 2009.
[27] J. S. Moon, "Graphene-on-SiC and graphene-on-Si MOSFETs for RF applications," in *GOMACTech Conf.*, Mar. 2011, pp. 1–4.
[28] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I—Effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.
[29] Z.-Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadas, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates," *IEEE Electron Device Lett.*, vol. 22, no. 7, pp. 321–323, Jul. 2001.
[30] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Gill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, p. 662, 2010.
[31] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, pp. 305–308, 2010.
[32] S.-Y. Kim, J.-H. Nah, I.-S. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field effect transistor with Al2O3 dielectric," *Appl. Phys. Lett.*, vol. 94, 2009, Art. ID 062107.
[33] J. S. Moon, D. Wong, M. Hu, P. Hashimoto, M. Antcliffe, C. McGuire, M. Micovic, and P. Willadson, "55% PAE and high power Ka-band GaN HEMTs with linearized transconductance cia n+ GaN source contact ledge," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 834–837, Aug. 2008.
[34] F. Schwierz, "Graphene transistors," *Nature Nanotechnol.*, vol. 5, pp. 487–496, 2010.
[35] N. Meng, J. F. Fernandez, E. Pichonat, O. Lancry, D. Vignaud, G. Dambrine, and H. Happy, "RF characterization of epitaxial graphene nano ribbon field effect transistor," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2011, pp. 1–3.
[36] H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene frequency multiplier," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 547–549, May 2009.
[37] Z. Wang, Z. Zhang, H. Xu, L. Ding, S. Wang, and L. Peng, "A high-performance top-gate graphene field-effect transistor based frequency doubler," *Appl. Phys. Lett.*, vol. 96, pp. 173104–173104-3, 2010.
[38] J. S. Moon, D. Curtis, D. Zehnder, S. Kim, D. K. Gaskill, G. G. Jernigan, R. L. Myers-Ward, C. R. Eddy, P. M. Campbell, K.-M. Lee, and P. Asbeck, "Low-phase noise graphene FETs in ambipolar RF applications," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 270–272, Mar. 2011.
[39] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 906–908, Sep. 2010.
[40] J. S. Moon, "Graphene MOSFETs for RF applications," presented at the GOMACTech Conf., Mar. 2010.
[41] B. G. Perumana, J.-H. Zhan, S. Taylor, and J. Laskar, "A 5 GHz, 21 dBm output IP3 resistive feedback LNA in 90-nm CMOS," in *33rd Eur. Solid State Circuits Conf.*, 2007, pp. 372–375.
[42] R. Limacher, A. Auf der Maur, H. Meier, A. Megej, A. Orzati, and W. Bachtold, "4–12 GHz InP HEMT-based MMIC low-noise amplifiers," in *Proc. IPRM*, 2004, pp. 28–31.
[43] B. Y. Ma, J. Bergman, P. Chen, J. Hacker, G. Sullivan, G. Nagy, and B. Brar, "InAs/InSb HEMT and its application to ultra-low-power wide-band high-gain low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4448–4455, Dec. 2006.
[44] S. L. G. Chu, J. C. Hwang, A. Bertand, M. J. Schindler, W. Struble, R. Binder, and W. Hoke, "High linearity monolithic broadband pseudomorphic spiked-doped MESFET amplifiers," in *IEEE GaAs IC Symp.*, 1992, pp. 211–214.
[45] B. L. Nelson, D. K. Umemoto, C. B. Perry, R. Dixit, B. R. Allen, M. E. Kim, and A. K. Oki, "High linearity low DC power GaAs HBT broadband amplifier to 11 GHz," in *GaAs IC Symp. Tech. Dig.*, 1989, pp. 79–82.
[46] K. W. Kobayashi, J. C. Cowles, L. T. Tran, A. Gutierrez-Aitken, M. Nishimoto, J. H. Elliott, T. R. Block, A. K. Oki, and D. C. Streit, "A 44-GHz high Ip3 InP HBT MMIC amplifier for low DC power millimeter-wave receiver applications," *IEEE. Solid-State Circuits*, vol. 34, no. 9, pp. 1188–1195, Sep. 1999.
[47] X. Chen, D. Akinwande, K.-J. Lee, G. F. Close, S. Yasuda, B. C. Paul, S. Fujita, J. Kong, and H.-S. P. Wong, "Fully integrated graphene and carbon nanotube interconnects for gigahertz high-speed CMOS electronics," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 3137–3143, Nov. 2010.

[48] S. Subrina, D. Kotchetkov, and A. A. Balandin, "Heat removal in silicon-on-insulator integrated circuits with graphene lateral heat spreaders," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1281–1283, Dec. 2009.

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