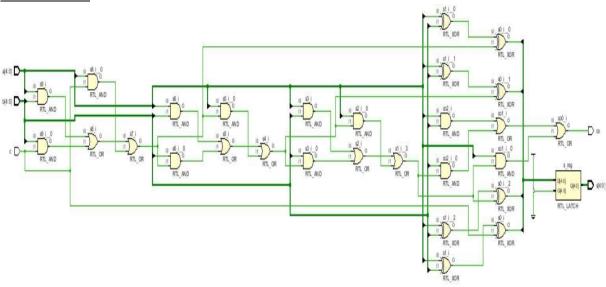
Practical 7

Aim: Write a VHDL Code to Implement 16 bit adder using behavioral modeling with generic

Code:

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
entity adder 16b bh is
generic(N : integer:=15);
  Port (a: in STD_LOGIC_VECTOR (15 downto 0);
       b: in STD LOGIC VECTOR (15 downto 0);
       c: in STD LOGIC;
       s: out STD LOGIC VECTOR (15 downto 0);
       co: out STD LOGIC);
end adder 16b bh;
architecture Behavioral of adder 16b bh is
begin
process(a,b,c)
variable i:integer:=0;
variable c1:std logic vector( N+1 downto 0);
begin
c1(0) := c;
11: for i in 0 to N loop
 s(i) \le a(i) xor b(i) xor c1(i);
  c1(i+1):=(a(i) \text{ and } b(i)) \text{ or } (b(i) \text{ and } c1(i)) \text{ or } (a(i) \text{ and } c1(i));
  end loop 11;
 co <= c1(N+1);
  end process;
end Behavioral;
```

RTL DIAGRAM:



Test bench Code:

library IEEE; use IEEE.STD_LOGIC_1164.ALL; entity Tb_adder_16b_bh is generic(N:integer:=15); -- Port (); end Tb_adder_16b_bh; architecture Behavioral of Tb_adder_16b_bh is component adder_16b_bh is Port (a:in STD_LOGIC_VECTOR (N downto 0); b: in STD_LOGIC_VECTOR (N downto 0); c: in STD_LOGIC; s : out STD_LOGIC_VECTOR (N downto 0); co: out STD_LOGIC); end component adder_16b_bh; signal a1: STD_LOGIC_VECTOR (N downto 0);

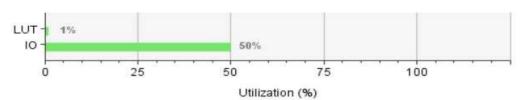
signal b1: STD_LOGIC_VECTOR (N a1<="11111111111111"; b1<="1010101010101010"; downto 0); signal c1 : STD LOGIC; wait for 10ns; signal s1: STD_LOGIC_VECTOR (N downto 0); c1<='1'; a1<="000000000000000"; signal c01 : STD_LOGIC; begin b1<="000000000000000"; X1:adder_16b_bh port wait for 10ns; map(a1,b1,c1,s1,c01); a1<="11111111111111"; process b1<="000000000000000"; begin c1<='0': wait for 10ns; a1<="0000000000000000"; b1<="00000000000000"; a1<="11111111111111"; wait for 10ns; b1<="11111111111111"; wait for 10ns; a1<="11111111111111"; b1<="000000000000000"; a1<="11111111111111"; wait for 10ns; b1<="1010101010101010"; wait for 10ns; a1<="11111111111111"; end process; b1<="11111111111111"; wait for 10ns; end Behavioral;

SIMULATION WAVEFORM:

		100 0		32.000 ns											
#	Name	Value	0 ns	10 ns	20 ns	30	ns	40 ns	50 ns	60 ns	70 ns	80 ns	90 ns	100 ns	110 ns
1	> 100 a1[15:0]	ffff	0000	*	tttt	-		0000	1111			0000	ffff		
2	> ⁽⁸⁰ b1[15:0]	aaaa	C	000	ffff	\times	aaaa	00	000	ffff	aaaa	00	00	ffff	aaaa
3	₩ c1	0													
4	∨ ^(N) s1[15:0]	aaa9	0000	ffff	fffe	\mathbf{x}	aaa9	0001	0000	ffff	aaaa	0000	ffff	fffe	aaa9
5	18 [15]	1													
6	₺ [14]	0													
7	18 [13]	1													
8	₩ [12]	0													
9	ll [11]	1													
10	₩ [10]	0				L									
11	1 [9]	1													
12	18 [8]	0													
13	U [7]	1													
14	18 [6]	0													
15	₩ [5]	1													
16	₩ [4]	0													
17	18 [3]	1													
18	₩ [2]	0													
19	le [1]	0													
20	U [0]	1													
21	18 c01	1													
22	16 N	15								15					

SYNTHESIS SUMMARY:





Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	E
4 Path 1	00	10	11	3	a[0]	со	9.480	4.612	4.868	00	input port clock	
4 Path 2	00	10	11	3	a[0]	s[14]	9.480	4.612	4.868	00	input port clock	
Path 3	∞	10	11	3	a[0]	s[15]	9.474	4.606	4.868	00	input port clock	
4 Path 4	∞	9	10	3	a[0]	s[12]	8.895	4.494	4.401	00	input port clock	
4 Path 5	00	9	10	3	a[0]	s[13]	8.895	4.494	4.401	00	input port clock	
Path 6	00	8	9	3	a[0]	s[10]	8.310	4.376	3.934	00	input port clock	
4 Path 7	00	8	9	3	a[0]	s[11]	8.310	4.376	3.934	00	input port clock	
4 Path 8	00	7	8	3	a[0]	s[8]	7.725	4.258	3.467	00	input port clock	
4 Path 9	00	7	8	3	a[0]	s[9]	7.725	4.258	3.467	00	input port clock	
Path 10	00	6	7	3	a[0]	s[6]	7.140	4.140	3.000	00	input port clock	

Maximum Combinational Delay: 9.480nSec