Sardar Vallabhbhai National Institute of Technology, Surat
Electronics Engineering Department

M.TECH. I (EC), SEMESTER I (Specialization: VLSI & Embedded)

HARDWARE DISCRIPTION LANGUAGES (EC623)

List of Practicals
Part-1 (VHDL as Coding Language)

Sr. No.	Aim
1	Write a VHDL code to implement basic gates.
2	Write a VHDL code for : a. 3x8 decoder using behavioral modelling b. 8x3 encoder using structural modelling c. 1x8 Demultiplexer using behavioral modelling d. 8x1 mux using structural modelling
3	Write a VHDL Code to implement Half Adder. Also write VHDL code for Full Adder with the instance of implemented Half adder.
4	Write a VHDL code for 4 bit ripple carry adder using loop statement.
5	Write a VHDL Code to implement D Flipflop and JK Flipflop.
6	Write a VHDL code to a. Implement 4- bit up-down counter using JK flip flop. b. Implement 4-bit serial in-parallel out shift register. c. Implement 4-bit ripple adder using generate statement.
7	Write VHDL code to implement 16 bit adder using behavioral modeling with generic.
8	Write a VHDL code to implement 8 bit up down counter using behavioral modeling.

Note:

- Write down testbench for each module/VHDL Code for Behavioural simulation.
- Synthesize the VHDL code using Xilinx Vivado Tool.