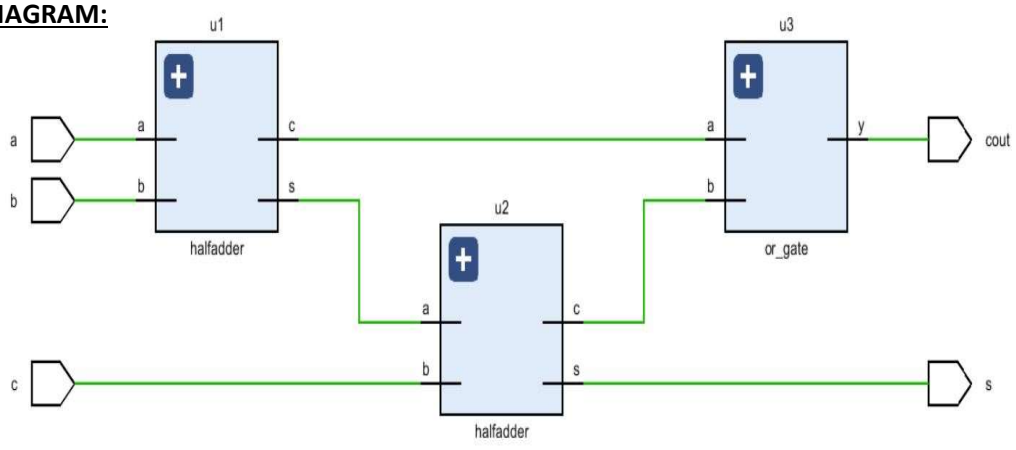
Practical 3

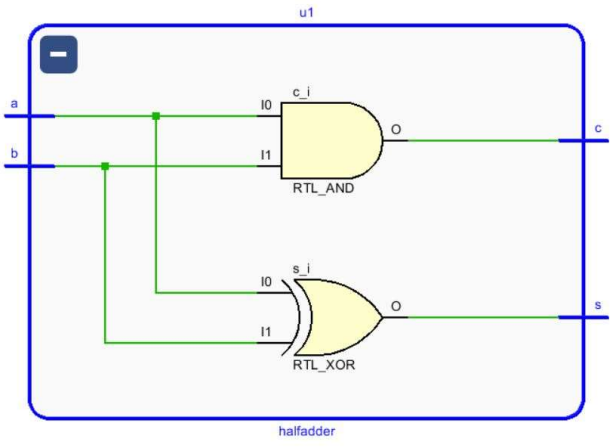
Aim: Write a VHDL Code to implement Half Adder. Also write VHDL code for Full Adder with the instance of implemented Half adder

Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity fulladder is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
c : in STD_LOGIC;
s : out STD_LOGIC;
cout : out STD_LOGIC);
end fulladder;

architecture Behavioral of fulladder is
component halfadder is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
s : out STD_LOGIC;
c : out STD_LOGIC);
end component halfadder;

component or_gate is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
y : out STD_LOGIC);
end component or_gate;

signal x,c1,c2:std_logic;

begin
u1:halfadder port map(a,b,x,c1);
u2:halfadder port map(x,c,s,c2);
u3:or_gate port map(c1,c2,cout);


end Behavioral;
```

RTL DIAGRAM:

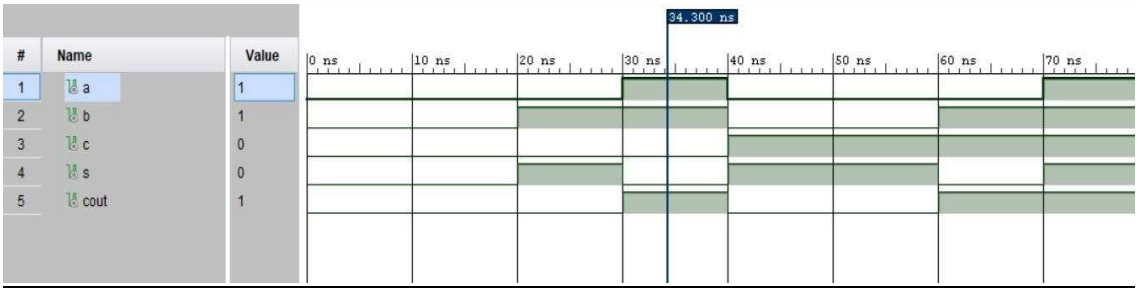




Test bench Code :

```
library IEEE;
use
IEEE.STD_LOGIC_1164.ALL;
entity Tb_fulladder is
--  Port ( );
end Tb_fulladder;

architecture Behavioral of
Tb_fulladder is
component fulladder is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
c : in STD_LOGIC;
s : out STD_LOGIC;
cout : out STD_LOGIC);
end component fulladder;
signal
a,b,c,s,cout:std_logic;
begin
u1:fulladder port
map(a,b,c,s,cout);
process
begin
a<='0';
b<='0';
c<='0';
wait for 10ns;
a<='0';
b<='0';
c<='1';
wait for 10ns;
a<='0';
b<='1';
c<='0';
wait for 10ns;
a<='0';
b<='1';
c<='1';
wait for 10ns;
a<='1';
b<='0';
c<='0';
wait for 10ns;
a<='1';
b<='0';
c<='1';
wait for 10ns;
a<='1';
b<='1';
c<='0';
wait for 10ns;
a<='1';
b<='1';
c<='1';
wait;
end process;
end Behavioral;
```

SIMULATION WAVEFORM :



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	4	2	b	cout	5.377	3.778	1.599	∞	input port clock
Path 2	∞	3	4	2	b	s	5.351	3.752	1.599	∞	input port clock

SYNTHESIS SUMMARY:

Resource	Utilization	Available	Utilization %
LUT	1	17600	0.01
IO	5	100	5.00

Maximum Combinational Delay: 5.377nSec