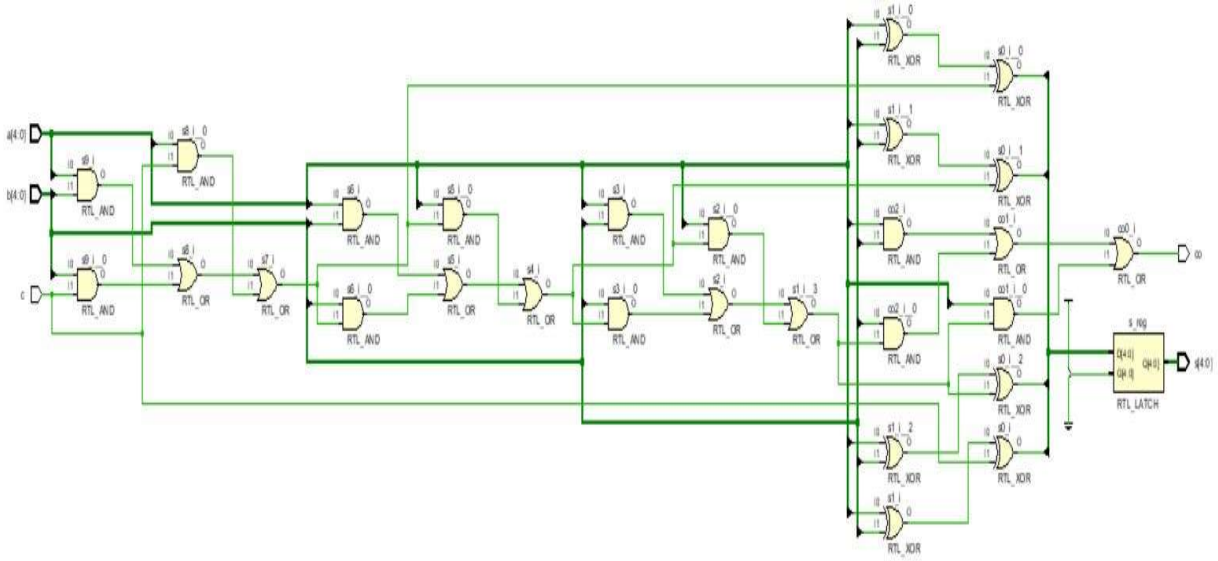
# Practical 7

**Aim:** Write a VHDL Code to Implement 16 bit adder using behavioral modeling with generic

**Code:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity adder_16b_bh is
generic(N : integer:=15);
   Port ( a : in STD_LOGIC_VECTOR (15 downto 0);
          b : in STD_LOGIC_VECTOR (15 downto 0);
          c : in STD_LOGIC;
          s : out STD_LOGIC_VECTOR (15 downto 0);
          co : out STD_LOGIC);
end adder_16b_bh;

architecture Behavioral of adder_16b_bh is

begin
process(a,b,c)
variable i:integer:=0;
variable c1:std_logic_vector( N+1 downto 0);
begin
c1(0):= c;
l1:for i in 0 to N loop

  s(i)<=a(i) xor b(i) xor c1(i);
  c1(i+1):= (a(i) and b(i)) or (b(i) and c1(i)) or (a(i) and c1(i));
  end loop l1;
  co<=c1(N+1);
  end process;
end Behavioral;
```

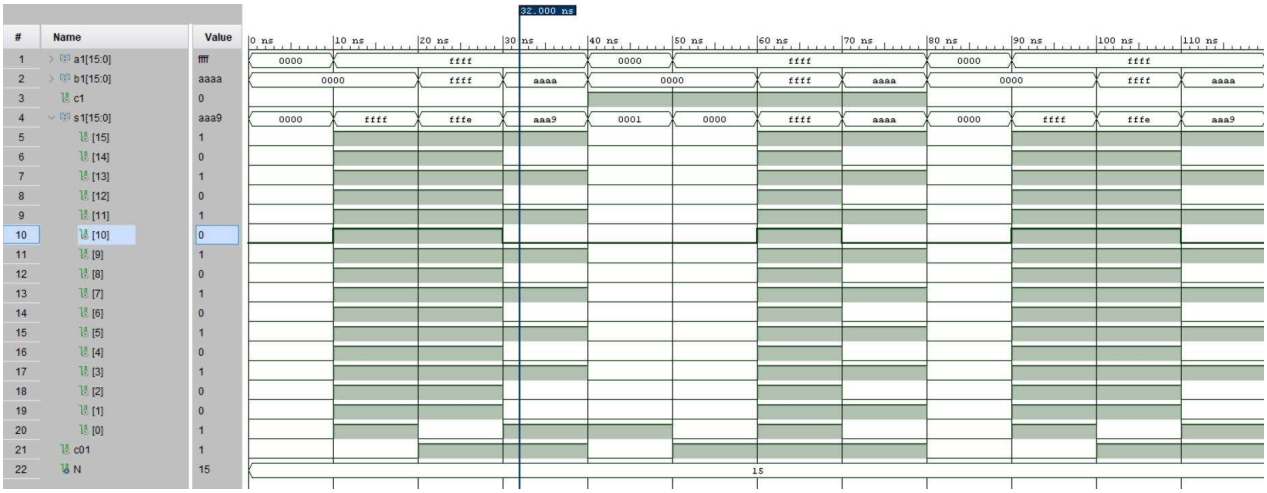
## RTL DIAGRAM:



## Test bench Code :

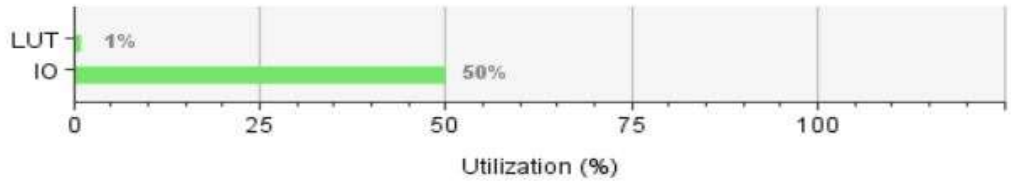
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Tb_adder_16b_bh is
generic(N : integer:=15);
--  Port ( );
end Tb_adder_16b_bh;

architecture Behavioral of
Tb_adder_16b_bh is
component adder_16b_bh is
   Port (  a : in
STD_LOGIC_VECTOR (N downto
0);
        b : in STD_LOGIC_VECTOR
(N downto 0);
        c : in STD_LOGIC;
        s : out STD_LOGIC_VECTOR
(N downto 0);
        co : out STD_LOGIC);
end component adder_16b_bh;

 signal a1 : STD_LOGIC_VECTOR (N
downto 0);
 signal b1 : STD_LOGIC_VECTOR (N
downto 0);
 signal c1 : STD_LOGIC;
 signal s1 : STD_LOGIC_VECTOR (N
downto 0);
 signal c01 : STD_LOGIC;
begin
X1:adder_16b_bh port
map(a1,b1,c1,s1,c01);
process
begin
c1<='0';
a1<="0000000000000000";
b1<="0000000000000000";
wait for 10ns;

a1<="1111111111111111";
b1<="0000000000000000";
wait for 10ns;

a1<="1111111111111111";
b1<="1111111111111111";
wait for 10ns;

a1<="1111111111111111";
b1<="1010101010101010";
wait for 10ns;

c1<='1';
a1<="0000000000000000";
b1<="0000000000000000";
wait for 10ns;

a1<="1111111111111111";
b1<="0000000000000000";
wait for 10ns;

a1<="1111111111111111";
b1<="1111111111111111";
wait for 10ns;

a1<="1111111111111111";
b1<="1010101010101010";
wait for 10ns;
end process;

end Behavioral;
```

**SIMULATION WAVEFORM :**




**SYNTHESIS SUMMARY:**

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 16 | 17600 | 0.09 |
| IO | 50 | 100 | 50.00 |




| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | D |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Path 1 | ∞ | 10 | 11 | 3 | a[0] | co | 9.480 | 4.612 | 4.868 | ∞ | input port clock | |
| Path 2 | ∞ | 10 | 11 | 3 | a[0] | s[14] | 9.480 | 4.612 | 4.868 | ∞ | input port clock | |
| Path 3 | ∞ | 10 | 11 | 3 | a[0] | s[15] | 9.474 | 4.606 | 4.868 | ∞ | input port clock | |
| Path 4 | ∞ | 9 | 10 | 3 | a[0] | s[12] | 8.895 | 4.494 | 4.401 | ∞ | input port clock | |
| Path 5 | ∞ | 9 | 10 | 3 | a[0] | s[13] | 8.895 | 4.494 | 4.401 | ∞ | input port clock | |
| Path 6 | ∞ | 8 | 9 | 3 | a[0] | s[10] | 8.310 | 4.376 | 3.934 | ∞ | input port clock | |
| Path 7 | ∞ | 8 | 9 | 3 | a[0] | s[11] | 8.310 | 4.376 | 3.934 | ∞ | input port clock | |
| Path 8 | ∞ | 7 | 8 | 3 | a[0] | s[8] | 7.725 | 4.258 | 3.467 | ∞ | input port clock | |
| Path 9 | ∞ | 7 | 8 | 3 | a[0] | s[9] | 7.725 | 4.258 | 3.467 | ∞ | input port clock | |
| Path 10 | ∞ | 6 | 7 | 3 | a[0] | s[6] | 7.140 | 4.140 | 3.000 | ∞ | input port clock | |

Maximum Combinational Delay: 9.480nSec