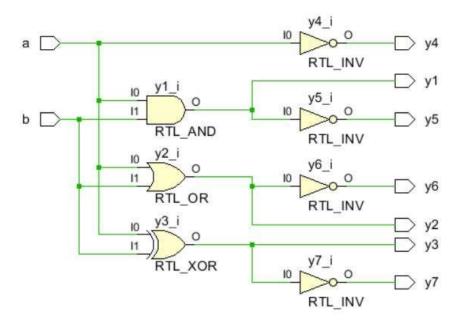
Practical 1

Aim: Write a VHDL code to implement basic gates.

Code:

```
y7: out STD LOGIC);
library IEEE;
                                                   end basic gates;
use IEEE.STD_LOGIC_1164.ALL;
                                                   architecture Behavioral of basic gates is
entity basic gates is
Port (a: in STD LOGIC;
                                                   begin
b: in STD LOGIC;
                                                   y1 \le a and b;
y1: out STD LOGIC;
                                                   y2 \le a \text{ or } b;
y2 : out STD LOGIC;
                                                   y3 \le a \text{ xor } b;
y3 : out STD_LOGIC;
                                                   y4 \le not a;
y4 : out STD_LOGIC;
                                                   y5 \le not (a and b);
y5 : out STD LOGIC;
                                                   y6 \le not (a or b);
y6: out STD LOGIC;
                                                   y7 \le not (a xor b);
                                                   end Behavioral;
```

RTL DIAGRAM:



library IEEE; y6 : out STD_LOGIC; wait for 10ns; use y7 : out STD_LOGIC); IEEE.STD_LOGIC_1164.ALL; a<='1'; entity Tb_basic_gates is end component b<='0'; wait for 10ns; -- Port (); basic_gates; end Tb_basic_gates; signal a<='0'; architecture Behavioral of b<='1'; a,b,y1,y2,y3,y4,y5,y6,y7:st Tb_basic_gates is d_logic; wait for 10ns; component basic_gates is begin Port (a : in STD_LOGIC; x1:basic_gates port a<='1'; b: in STD_LOGIC; map(a,b,y1,y2,y3,y4,y5,y6, b<='1'; y1: out STD_LOGIC; wait; y7); y2 : out STD_LOGIC; process y3: out STD_LOGIC; begin end process; y4 : out STD_LOGIC; a<='0'; end Behavioral;

y5 : out STD_LOGIC; b<='0';

SIMULATION WAVEFORM:

#	Name	Value	0 ns	5 ns	10 ns	15 ns	20 ns	25 ns	30 ns	35 ns	40 ns
1	18 a	0									
2	la b	1				į.					
3	1∆ y1	0									
4	18 y2	1									
5	lå y3	1									
6 7	l8 y4	1									
7	18 y5	1									
8	18 y6	0									
9	1 8 y7	0									
			H								

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	00	3	4	7	а	y1	5.377	3.778	1.599	00	input port clock
Path 2	00	3	4	6	b	уЗ	5.377	3.778	1.599	00	input port clock
Path 3	00	3	4	6	b	у6	5.377	3.778	1.599	00	input port clock
Path 4	00	3	4	6	b	y2	5.351	3.752	1.599	00	input port clock
Path 5	00	3	4	7	a	у4	5.351	3.752	1.599	00	input port clock
Path 6	00	3	4	7	а	у5	5.351	3.752	1.599	00	input port clock
Path 7	00	3	4	6	b	y7	5.351	3.752	1.599	00	input port clock

SYNTHESIS SUMMARY:

Resource	Utilization	Available	Utilization %
LUT	4	17600	0.02
Ю	9	100	9.00

Maximum Combinational Delay: 5.377nSec