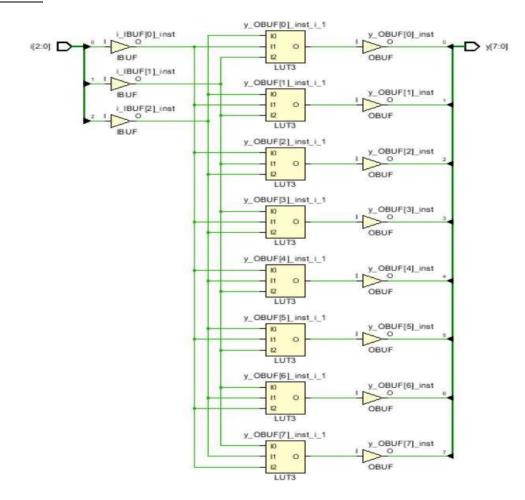
Practical 2

Aim: Write a VHDL code to implement 3x8 decoder using behavioral modelling

```
Code:
                                                  case(i) is
library IEEE;
                                                 when "000" => y<="00000001";
use IEEE.STD LOGIC_1164.ALL;
                                                 when "001" => y<="00000010";
                                                 when "010" => y<="00000100";
entity Decoder 3x8 is
                                                 when "011" \Rightarrow y<="00001000";
  Port (i : in STD_LOGIC_VECTOR (2 downto 0); when "100" => y<="00010000";
      y: out STD_LOGIC_VECTOR (7 downto 0))when "101" => y<="00100000";
end Decoder 3x8;
                                                 when "110" \Rightarrow y<="01000000";
                                                  when "111" \Rightarrow y<="10000000";
                                                 when others =>y<="10000000";
architecture Behavioral of Decoder 3x8 is
begin
                                                 end case;
process(i)
                                                 end process;
begin
                                                 end Behavioral;
```

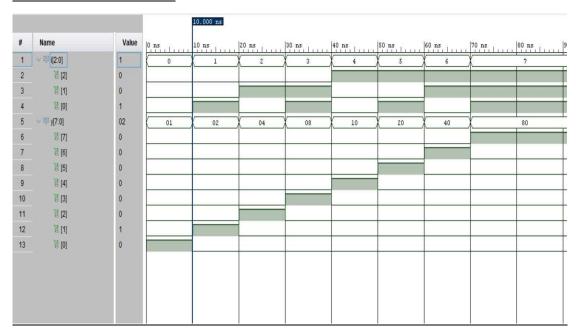
RTL DIAGRAM:



Test bench Code:

library IEEE; i <="001"; use IEEE.STD LOGIC 1164.ALL; wait for 10ns; entity Tb_Decoder_3x8 is -- Port (); i <="010"; end Tb_Decoder_3x8; wait for 10ns; architecture Behavioral of Tb_Decoder_3x8 i <="011"; wait for 10ns; component Decoder_3x8 is Port (i:in STD_LOGIC_VECTOR (2 downto i <="100"; wait for 10ns; y: out STD_LOGIC_VECTOR (7 downto 0)); end component Decoder_3x8; i <="101"; signal i:std_logic_vector(2 downto 0); wait for 10ns; signal y:std_logic_vector(7 downto 0); i <="110"; begin wait for 10ns; x1:Decoder_3x8 port map(i,y); process i <="111"; begin wait; i <="000"; end process; wait for 10ns; end Behavioral;

SIMULATION WAVEFORM:



| Name | Slack ^1 | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock |
|----------|----------|--------|--------|-------------|------|------|-------------|-------------|-----------|-------------|------------------|
| Path 1 | 00 | 3 | 4 | 8 | i[0] | y[1] | 5.377 | 3.778 | 1.599 | 00 | input port clock |
| Path 2 | 00 | 3 | 4 | 8 | i[0] | y[3] | 5.377 | 3.778 | 1.599 | 00 | input port clock |
| Path 3 | 00 | 3 | 4 | 8 | i[0] | y[5] | 5.377 | 3.778 | 1.599 | 00 | input port clock |
| 4 Path 4 | 00 | 3 | 4 | 8 | i[2] | y[7] | 5.377 | 3.778 | 1.599 | 00 | input port clock |
| Path 5 | 00 | 3 | 4 | 8 | i[1] | y[0] | 5.351 | 3.752 | 1.599 | 00 | input port clock |
| ∿ Path 6 | 00 | 3 | 4 | 8 | i[2] | y[2] | 5.351 | 3.752 | 1.599 | 00 | input port clock |
| Path 7 | 00 | 3 | 4 | 8 | i[1] | y[4] | 5.351 | 3.752 | 1.599 | 00 | input port clock |
| Path 8 | 00 | 3 | 4 | 8 | i[0] | y[6] | 5.351 | 3.752 | 1.599 | 00 | input port clock |

SYNTHESIS SUMMARY:

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT | 4 | 17600 | 0.02 |
| 10 | 11 | 100 | 11.00 |

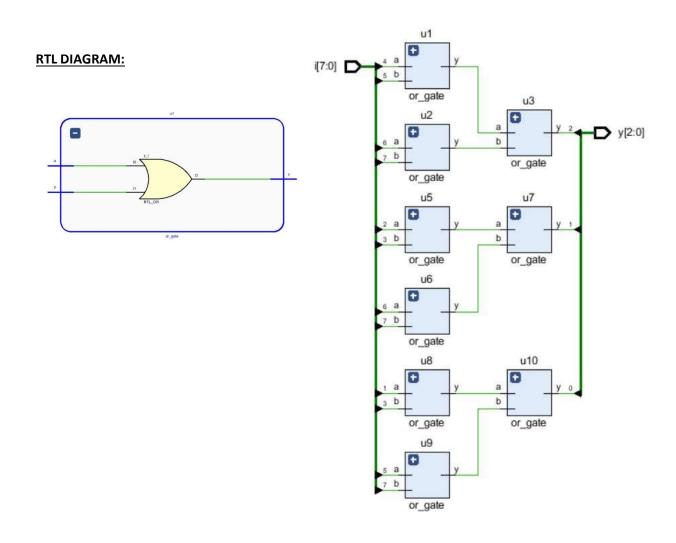
Maximum Combinational Delay: 5.377nSec

<u>Aim</u>: Write a VHDL code to implement 8x3 encoder using structural modelling

Code:

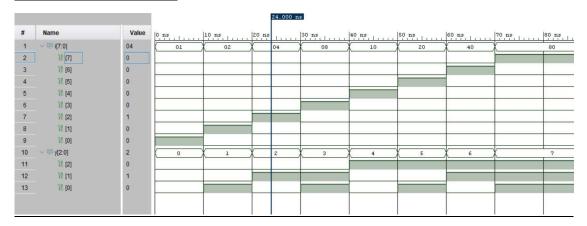
```
y: out STD LOGIC);
library IEEE;
                                                  end component or gate;
use IEEE.STD_LOGIC_1164.ALL;
                                                  signal x: std logic vector(0 to 5);
                                                  begin
entity Encoder 8x3 is
  Port (i: in STD LOGIC VECTOR (7 downto 0);
      y: out STD_LOGIC_VECTOR (2 downto 0))µ1:or_gate port map(i(4),i(5),x(0));
                                                  u2:or_gate port map(i(6),i(7),x(1));
end Encoder 8x3;
                                                  u3:or gate port map(x(0),x(1),y(2));
architecture Behavioral of Encoder 8x3 is
                                                  u5:or gate port map(i(2),i(3),x(2));
                                                  u6:or gate port map(i(6),i(7),x(3));
component or gate
Port (a: in STD LOGIC;
                                                  u7:or gate port map(x(2),x(3),y(1));
                                                  u8:or gate port map(i(1),i(3),x(4));
     b: in STD LOGIC;
                                                  u9:or gate port map(i(5),i(7),x(5));
                                                  u10:or_gate\ port\ map(x(4),x(5),y(0));
```

end Behavioral;



Test bench Code: end component i<="00000100"; library IEEE; wait for 10ns; Encoder 8x3; use i<="00001000"; signal i: IEEE.STD_LOGIC_1164.ALL; STD_LOGIC_VECTOR (7 wait for 10ns; entity Tb_Encoder_8x3 is downto 0); i<="00010000"; -- Port (); signal y: wait for 10ns; end Tb_Encoder_8x3; STD_LOGIC_VECTOR (2 i<="00100000"; wait for 10ns; downto 0); architecture Behavioral of i<="01000000"; begin Tb Encoder 8x3 is x:Encoder_8x3 port wait for 10ns; component Encoder_8x3 map(i,y); i<="10000000"; is process wait; Port (i:in begin end process; STD_LOGIC_VECTOR (7 downto 0); i<="0000001"; end Behavioral; y:out wait for 10ns; STD_LOGIC_VECTOR (2 i<="0000010"; downto 0)); wait for 10ns;

SIMULATION WAVEFORM:



| Name | Slack | A1 | Levels | Routes | High Fanout | From | То | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock |
|--------|-------|----|--------|--------|-------------|------|------|-------------|-------------|-----------|-------------|------------------|
| Path 1 | | 00 | 3 | 4 | 2 | i[5] | y[0] | 5.351 | 3.752 | 1.599 | 00 | input port clock |
| Path 2 | | 00 | 3 | 4 | 2 | i[6] | y[1] | 5.351 | 3.752 | 1.599 | 00 | input port clock |
| Path 3 | | 00 | 3 | 4 | 2 | i[6] | y[2] | 5.351 | 3.752 | 1.599 | 00 | input port clock |

SYNTHESIS SUMMARY:

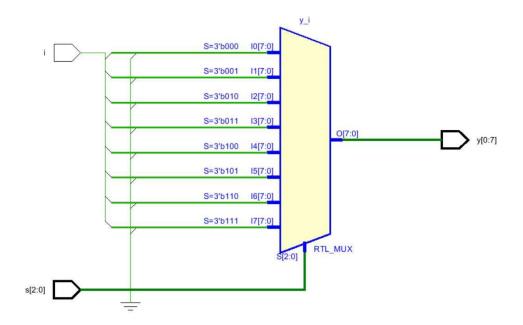
| Resource | Utilization | Available | Utilization % | |
|----------|-------------|-----------|----------------------|--|
| LUT | 3 | 17600 | 0.02 | |
| 10 | 10 | 100 | 10.00 | |

Maximum Combinational Delay: 5.351nSec

Code:

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
entity Demux1x8 is
Port (i: in STD LOGIC;
y: out STD LOGIC VECTOR (0 to 7);
s: in STD LOGIC VECTOR (2 downto 0));
end Demux1x8;
architecture Behavioral of Demux1x8 is
begin
process(i,s)
begin
case(s) is
when "000" => y(0) \le i;
y(1 \text{ to } 7) \le "0000000";
when "001" => y(1) \le i;
y(0) \le 0';
y(2 to 7)<="000000";
when "010" \Rightarrow y(2)<=i;
y(0 \text{ to } 1) \le 00";
y(3 \text{ to } 7) \le "00000";
when "011" => y(3) <= i;
y(0 \text{ to } 2) \le 000";
y(4 \text{ to } 7) \le "0000";
when "100" => y(4) <= i;
y(0 \text{ to } 3) \le 0000";
y(5 \text{ to } 7) \le 000";
when "101" => y(5) \le i;
y(0 \text{ to } 4) \le "00000";
y(6 \text{ to } 7) \le 00";
when "110" => y(6) <= i;
y(0 \text{ to } 5) \le "000000";
y(7) \le 0';
when "111" => y(7) <= i;
y(0 \text{ to } 6) \le "0000000";
when others => y <= "000000000";
end case;
end process;
end Behavioral;
```

RTL DIAGRAM:



```
Test bench Code:
                                                  wait for 10 ns;
library IEEE;
                                                  s<="010";
use IEEE.STD LOGIC 1164.ALL;
                                                  wait for 10 ns;
entity Tb_Demux1x8 is
                                                  s<="011";
-- Port ();
                                                  wait for 10 ns;
end Tb_Demux1x8;
                                                  s<="100";
architecture Behavioral of Tb_Demux1x8 is
                                                  wait for 10 ns;
component Demux1x8 is
                                                  s<="101";
  Port (i: in STD_LOGIC;
                                                  wait for 10 ns;
     y: out STD_LOGIC_VECTOR (0 to 7);
                                                  s<="110";
     s: in STD_LOGIC_VECTOR (2 downto
                                                  wait for 10 ns;
0));
                                                  s<="111";
end component Demux1x8;
                                                  wait for 50 ns;
signal i : STD_LOGIC;
signal y: STD_LOGIC_VECTOR (0 to 7);
                                                  i<='1';
signal s: STD_LOGIC_VECTOR (2 downto 0);
                                                  s<="000";
begin
                                                  wait for 10 ns;
x1:Demux1x8 port map(i,y,s);
                                                  s<="001";
process
                                                  wait for 10 ns;
begin
                                                  s<="010";
i<='0';
                                                  wait for 10 ns;
s<="000";
                                                  s<="011";
wait for 10 ns;
                                                  wait for 10 ns;
s<="001";
                                                  s<="100";
```

 $\begin{array}{lll} \text{wait for 10 ns;} & \text{s}<="111";\\ \text{s}<="101"; & \text{wait;}\\ \text{wait for 10 ns;} & \text{end process;}\\ \text{s}<="110"; & \text{end Behavioral;}\\ \text{wait for 10 ns;} & \end{array}$

SIMULATION WAVEFORM:

| | 57. | 92 | | | 132.000 ns | | | | | | |
|----|-------------------------|-------|--------|--------|------------|--------|--------|--------|--------|--------|--------|
| # | Name | Value | 110 ns | 120 ns | 130 ns | 140 ns | 150 ns | 160 ns | 170 ns | 180 ns | 190 ns |
| 1 | 18 i | 1 | | | | | | | | | |
| 2 | ∨ ⁰²⁰ y[0:7] | 40 | 00 | 80 | 40 | 20 | 10 | 08 | 04 | 02 | 01 |
| 3 | 18 [0] | 0 | | | | | | | | | |
| 4 | 18 [1] | 1 | | | | | | | | | |
| 5 | 18 [2] | 0 | | | | | | | | | |
| 6 | 18 [3] | 0 | | | | | | | | | |
| 7 | 18 [4] | 0 | | | | | | | | | |
| 8 | 18 [5] | 0 | | | | | | | | | |
| 9 | 18 [6] | 0 | | | | | | | | | |
| 10 | 18 [7] | 0 | | | | | | | | | |
| 11 | ∨ 00 s[2:0] | 1 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 12 | 18 [2] | 0 | | | | | | | | | |
| 13 | 1 8 [1] | 0 | | | | | | | | | |
| 14 | 18 [0] | 1 | | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |

| Name | Slack ^1 | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock |
|----------|----------|--------|--------|-------------|------|------|-------------|-------------|-----------|-------------|------------------|
| Path 1 | 00 | 3 | 4 | 8 | s[1] | y[0] | 5.379 | 3.780 | 1.599 | 00 | input port clock |
| Path 2 | 00 | 3 | 4 | 8 | s[0] | y[3] | 5.379 | 3.780 | 1.599 | 00 | input port clock |
| Path 3 | 00 | 3 | 4 | 8 | s[2] | y[4] | 5.379 | 3.780 | 1.599 | 00 | input port clock |
| ┡ Path 4 | 00 | 3 | 4 | 8 | s[2] | y[7] | 5.379 | 3.780 | 1.599 | 00 | input port clock |
| Path 5 | 00 | 3 | 4 | 8 | s[2] | y[1] | 5.351 | 3.752 | 1.599 | .00 | input port clock |
| Path 6 | 00 | 3 | 4 | 8 | s[2] | y[2] | 5.351 | 3.752 | 1.599 | 00 | input port clock |
| Path 7 | 00 | 3 | 4 | 8 | i | y[5] | 5.351 | 3.752 | 1.599 | 00 | input port clock |
| Path 8 | 00 | 3 | 4 | 8 | s[1] | y[6] | 5.351 | 3.752 | 1.599 | 00 | input port clock |

SYNTHESIS SUMMARY:

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT | 4 | 17600 | 0.02 |
| 10 | 12 | 100 | 12.00 |

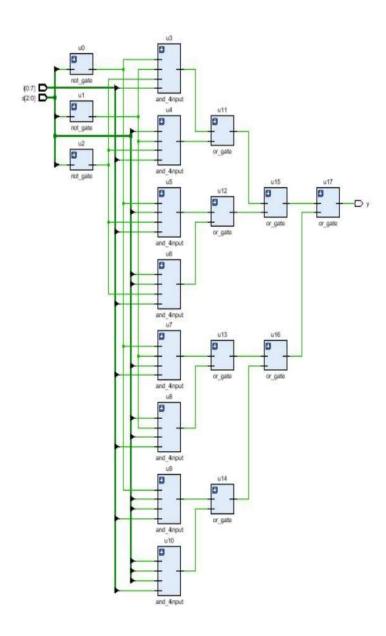
Maximum Combinational Delay: 5.379nSec

Code:

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
entity Mux 8x1 is
  Port ( i : in STD_LOGIC_VECTOR (0 to 7);
      s: in STD LOGIC VECTOR (2 downto 0);
      y: out STD LOGIC);
end Mux 8x1;
architecture Behavioral of Mux 8x1 is
component or gate is
  Port (a: in STD LOGIC;
      b: in STD LOGIC;
      y: out STD LOGIC);
end component or gate;
component and 4input is
 Port (a1: in STD LOGIC;
      a2: in STD LOGIC;
      a3: in STD LOGIC;
      a4: in STD LOGIC;
      y: out STD LOGIC);
end component and 4input;
component not gate is
  Port (a: in STD LOGIC;
      y: out STD LOGIC);
end component not gate;
signal sb:std logic vector(0 to 2);
signal x:std logic vector(0 to 13);
u0:not gate port map(s(0),sb(0));
u1:not gate port map(s(1),sb(1));
u2:not gate port map(s(2),sb(2));
u3:and 4input port map(sb(0),sb(1),sb(2),i(0),x(0));
u4:and 4input port map(s(0),sb(1),sb(2),i(1),x(1));
u5:and 4input port map(sb(0),s(1),sb(2),i(2),x(2));
u6:and 4input port map(s(0), s(1), sb(2), i(3), x(3));
u7:and_4input port map(sb(0),sb(1),s(2),i(4),x(4));
u8:and 4input port map(s(0),s(1),s(2),i(5),x(5));
u9:and 4input port map(sb(0),s(1),s(2),i(6),x(6));
u10:and 4input port map(s(0), s(1), s(2), i(7), x(7));
u11:or gate port map(x(0),x(1),x(8));
u12:or gate port map(x(2),x(3),x(9));
```

```
u13:or_gate port map(x(4),x(5),x(10));
u14:or_gate port map(x(6),x(7),x(11));
u15:or_gate port map(x(8),x(9),x(12));
u16:or_gate port map(x(10),x(11),x(13));
u17:or_gate port map(x(12),x(13),y);
end Behavioral;
```

RTL DIAGRAM:

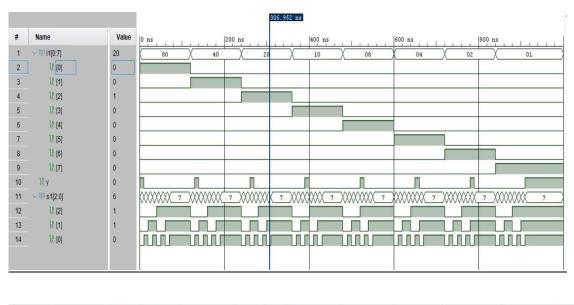


Test bench Code:

| library IEEE; | wait for 10ns; | s1<="001"; |
|----------------------------|-----------------------------|-----------------|
| use | s1<="111"; | wait for 10ns; |
| IEEE.STD_LOGIC_1164.ALL; | wait for 50ns; | s1<="010"; |
| entity Tb_Mux_8x1 is | | wait for 10ns; |
| Port (); | i1<="01000000"; | s1<="011"; |
| end Tb_Mux_8x1; | s1<="000"; | wait for 10ns; |
| architecture Behavioral of | wait for 10ns; | s1<="100"; |
| Tb_Mux_8x1 is | s1<="001"; | wait for 10ns; |
| component Mux_8x1 is | wait for 10ns; | s1<="101"; |
| Port (i : in | s1<="010"; | wait for 10ns; |
| STD_LOGIC_VECTOR (0 to | wait for 10ns; | s1<="110"; |
| 7); | s1<="011"; | wait for 10ns; |
| s : in | wait for 10ns; | s1<="111"; |
| STD_LOGIC_VECTOR (2 | s1<="100"; | wait for 50ns; |
| downto 0); | wait for 10ns; | i1<="00001000"; |
| y : out STD_LOGIC); | s1<="101"; | s1<="000"; |
| end component Mux_8x1; | wait for 10ns; | wait for 10ns; |
| signal | s1<="110"; | s1<="001"; |
| i1:STD_LOGIC_VECTOR (0 | wait for 10ns; | wait for 10ns; |
| to 7); | s1<="111"; | s1<="010"; |
| signal y: std_logic; | wait for 50ns; | wait for 10ns; |
| signal s1: | · | s1<="011"; |
| std_logic_vector(2 downto | i1<="00100000"; | wait for 10ns; |
| 0); | s1<="000"; | s1<="100"; |
| begin | wait for 10ns; | wait for 10ns; |
| u1:Mux_8x1 port | s1<="001"; | s1<="101"; |
| map(i1,s1,y); | wait for 10ns; | wait for 10ns; |
| process | s1<="010"; | s1<="110"; |
| begin | wait for 10ns; | wait for 10ns; |
| i1<="10000000"; | s1<="011"; | s1<="111"; |
| s1<="000"; | wait for 10ns; | wait for 50ns; |
| wait for 10ns; | s1<="100"; | i1<="00000100"; |
| s1<="001"; | wait for 10ns; | s1<="000"; |
| wait for 10ns; | s1<="101"; | wait for 10ns; |
| s1<="010"; | wait for 10ns; | s1<="001"; |
| wait for 10ns; | s1<="110"; | wait for 10ns; |
| s1<="011"; | wait for 10ns; | s1<="010"; |
| wait for 10ns; | s1<="111"; | wait for 10ns; |
| s1<="100"; | wait for 50ns; | s1<="011"; |
| wait for 10ns; | , | wait for 10ns; |
| s1<="101"; | i1<="00010000"; | s1<="100"; |
| wait for 10ns; | s1<="000"; | wait for 10ns; |
| s1<="110"; | wait for 10ns; | s1<="101"; |
| | · · · · · · · · · · · · · · | , |

wait for 10ns; s1<="100"; wait for 10ns; s1<="110"; wait for 10ns; s1<="011"; wait for 10ns; s1<="101"; wait for 10ns; s1<="111"; s1<="100"; wait for 10ns; wait for 50ns; s1<="110"; wait for 10ns; wait for 10ns; s1<="101"; i1<="00000010"; s1<="111"; wait for 10ns; s1<="000"; wait for 50ns; s1<="110"; wait for 10ns; wait for 10ns; s1<="001"; i1<="00000001"; s1<="111"; s1<="000"; wait for 10ns; wait; s1<="010"; wait for 10ns; end process; wait for 10ns; s1<="001"; end Behavioral; s1<="011"; wait for 10ns; wait for 10ns; s1<="010";

SIMULATION WAVEFORM:



| Name | Slack ^ | 1 | Levels | Routes | High Fanout | From | То | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock |
|--------|---------|---|--------|--------|-------------|------|----|-------------|-------------|-----------|-------------|------------------|
| Path 1 | 0 | 0 | 4 | 5 | 1 | i[4] | y | 5.770 | 4.171 | 1.599 | 00 | input port clock |

SYNTHESIS SUMMARY:

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|----------------------|
| LUT | 2 | 17600 | 0.01 |
| Ю | 12 | 100 | 12.00 |

Maximum Combinational Delay: 5.77nSec