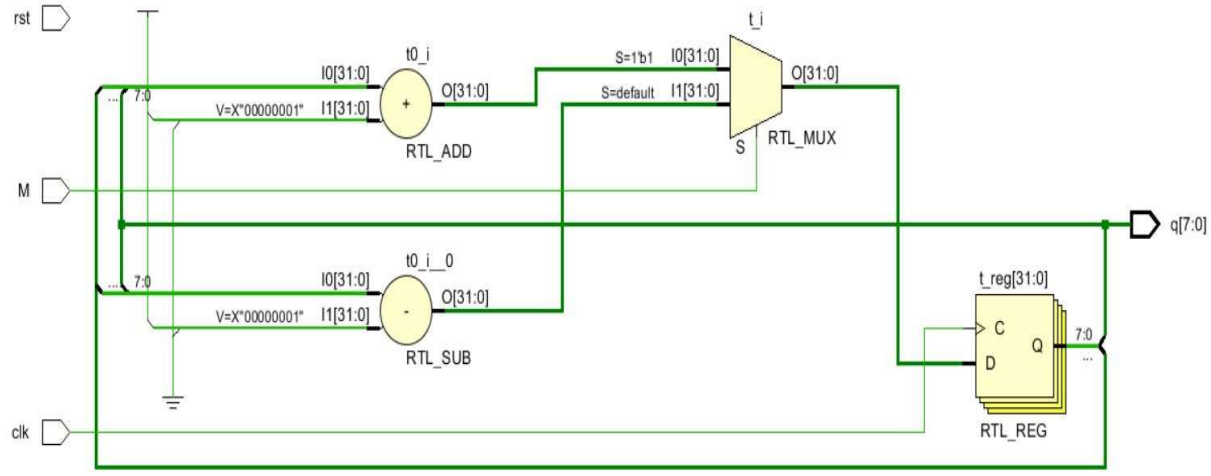
# Practical 8

**Aim:** Write a VHDL Code to implement 8 bit up down counter using behavioral modeling

**Code:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_arith.all;
entity U_D_bh_8B is
   Port ( clk : in STD_LOGIC;
          rst : in STD_LOGIC;
          M : in STD_LOGIC;
          q : out STD_LOGIC_VECTOR (7 downto 0));
end U_D_bh_8B;

architecture Behavioral of U_D_bh_8B is

begin
process(clk,rst,M)
variable t:integer:=0;
variable t1:STD_LOGIC_VECTOR(7 downto 0);
begin
if(rising_edge(clk)) then

  if(M='1') then
  t:=t + 1;
  elsif(m='0') then
  t:=t - 1;
  end if;

 end if;

  t1:= conv_std_logic_vector(t, 8);

q<=t1;
end process;
end Behavioral;
```

**RTL DIAGRAM:**

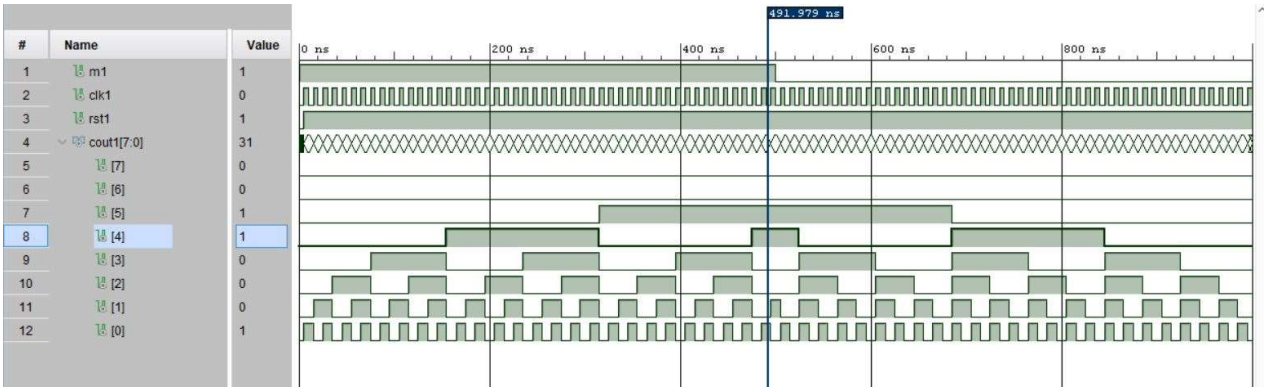



**Test bench Code :**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Tb_U_D_bh_8b is
-- Port ( );
end Tb_U_D_bh_8b;

architecture Behavioral of
Tb_U_D_bh_8b is

component U_D_bh_8b is
   Port ( clk : in STD_LOGIC;
          rst : in STD_LOGIC;
          M : in STD_LOGIC;
          q : out STD_LOGIC_VECTOR
(7 downto 0));
end component U_D_bh_8b;
signal m1,clk1,rst1:std_logic;

signal cout1:std_logic_vector(7
downto 0);


begin
X1:U_D_bh_8b port
map(clk1,rst1,m1,cout1);
process
begin
```

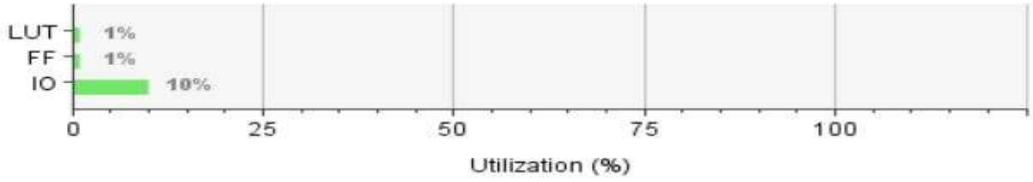
```
rst1<='0';
wait for 5ns;
rst1<='1';
wait;
end process;

process
begin
clk1<='0';
wait for 5ns;
clk1<='1';
wait for 5ns;
end process;

process
begin

m1<='1';--upcount
wait for 500ns;
m1<='0';--downcount
wait;
end process;

end Behavioral;
```

## SIMULATION WAVEFORM :




## SYNTHESIS SUMMARY:

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 7 | 17600 | 0.04 |
| FF | 8 | 35200 | 0.02 |
| IO | 10 | 100 | 10.00 |




| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Path 1 | ∞ | 2 | 2 | 2 | t_reg[0]/C | q[0] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 2 | ∞ | 2 | 2 | 3 | t_reg[1]/C | q[1] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 3 | ∞ | 2 | 2 | 3 | t_reg[2]/C | q[2] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 4 | ∞ | 2 | 2 | 3 | t_reg[3]/C | q[3] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 5 | ∞ | 2 | 2 | 3 | t_reg[4]/C | q[4] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 6 | ∞ | 2 | 2 | 3 | t_reg[5]/C | q[5] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 7 | ∞ | 2 | 2 | 3 | t_reg[6]/C | q[6] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 8 | ∞ | 2 | 2 | 2 | t_reg[7]/C | q[7] | 4.076 | 3.276 | 0.800 | ∞ | |
| Path 9 | ∞ | 4 | 5 | 7 | M | t_reg[5]/D | 2.804 | 2.004 | 0.800 | ∞ | input port clock |
| Path 10 | ∞ | 4 | 5 | 7 | M | t_reg[7]/D | 2.785 | 1.985 | 0.800 | ∞ | input port clock |

Maximum Combinational Delay: 4.076nSec