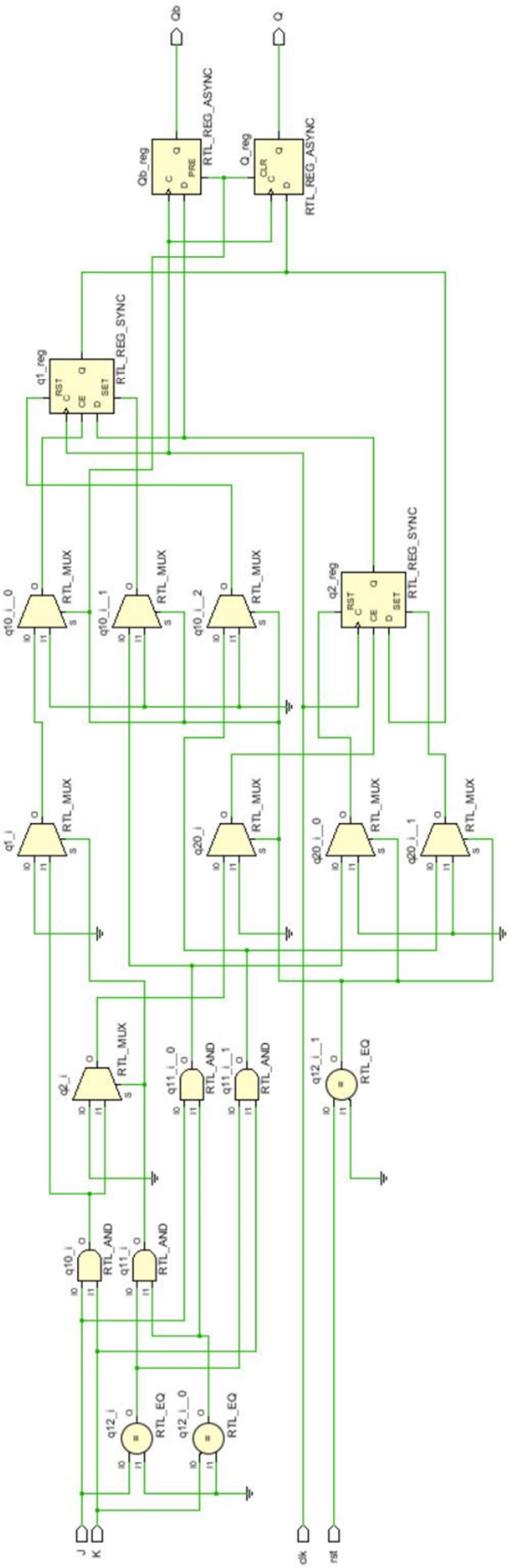
Practical 5

Aim: Write a VHDL Code to implement JK Flipflop

Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity JK_FF is
    Port ( clk : in STD_LOGIC;
           rst : in STD_LOGIC;
           J : in STD_LOGIC;
           K : in STD_LOGIC;
           Q : out STD_LOGIC;
           Qb : out STD_LOGIC);
end JK_FF;

architecture Behavioral of JK_FF is
signal q1:std_logic:='0';
signal q2:std_logic:='1';

begin

   process(rst,clk,J,K)
      begin
      if (rst='0') then
         Q<='0';
         Qb<='1';
     elsif(rising_edge(clk)) then
          if(J = '1' and  K = '0')then
          q1<='1';
          q2<='0';
elsif(J = '0' and K = '1') then
          q1<='0';
          q2<='1';
elsif(J = '0' and K = '0') then
          q1<= q1;
          q2<=q2;
elsif(J ='1' and K ='1') then
           q1<= q2;
           q2<= q1;
          end if;
          Q<=q1;
          Qb<=q2;
     end if;
    end process;

end Behavioral;
```

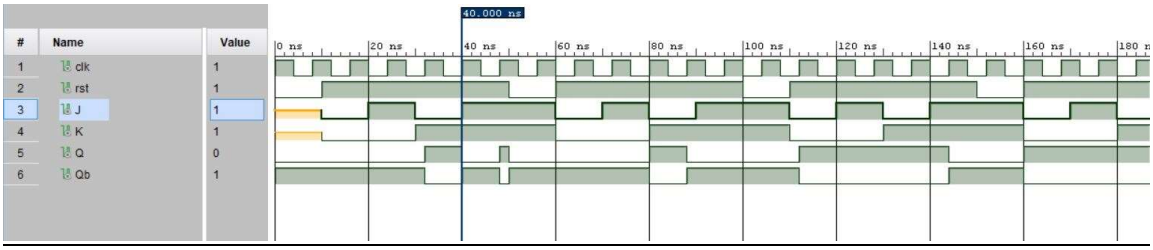
RTL DIAGRAM:


Qb
Q
Qb_reg
Q_reg
RTL_REG_ASYNC
RTL_REG_ASYNC
q1_reg
RTL_REG_SYNC
q2_reg
RTL_REG_SYNC
q10_i_0
q10_i_1
q10_i_2
RTL_MUX
q1_i
q20_i
q20_i_0
q20_i_1
q2_i
RTL_MUX
q11_i_0
q11_i_1
RTL_AND
q12_i_1
RTL_EQ
q10_i
q11_i
RTL_AND
q12_i
q12_i_0
RTL_EQ
J
K
clk
rst

Test bench Code :

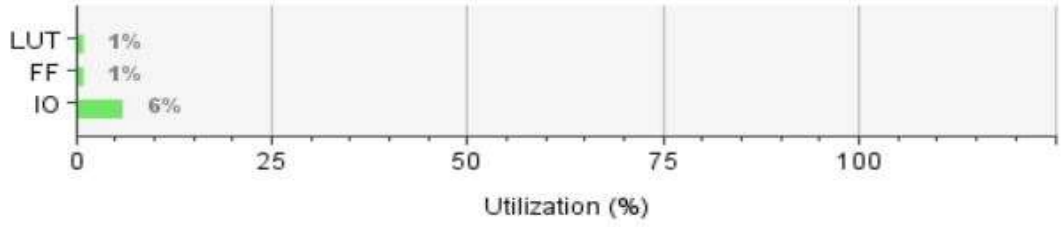
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Tb_JK_FF is
-- Port ( );
end Tb_JK_FF;

architecture Behavioral of
Tb_JK_FF is

component JK_FF is
Port ( clk : in STD_LOGIC;
       rst : in STD_LOGIC;
       J : in STD_LOGIC;
       K : in STD_LOGIC;
       Q : out STD_LOGIC;
       Qb : out STD_LOGIC);
end component JK_FF;
signal clk,rst,J,K,Q,Qb:std_logic;
begin
x1:JK_FF port
map(clk,rst,J,K,Q,Qb);

  process
  begin

  clk<='1';
  wait for 4ns;
  clk<='0';
  wait for 4ns;
  end process;

   process
   begin
   rst<='0';
   wait for 10ns;
   rst<='1';
   J<='0';
   K<='0';
   wait for 10ns;

   J<='1';
   K<='0';
   wait for 10ns;

   J<='0';
   K<='1';
   wait for 10ns;

   J<='1';
   K<='1';
   wait for 10ns;

  end process;

end Behavioral;
```

SIMULATION WAVEFORM :



SYNTHESIS SUMMARY:

Resource	Utilization	Available	Utilization %
LUT	2	17600	0.01
FF	4	35200	0.01
IO	6	100	6.00



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	2	1	Q_reg/C	Q	4.076	3.276	0.800	∞	
Path 2	∞	2	2	1	Qb_reg/C	Qb	4.076	3.276	0.800	∞	
Path 3	∞	2	3	3	rst	Q_reg/CLR	2.693	1.106	1.587	∞	input port clock
Path 4	∞	2	3	3	rst	Qb_reg/PRE	2.693	1.106	1.587	∞	input port clock
Path 5	∞	2	3	2	K	q1_reg/D	1.932	1.132	0.800	∞	input port clock
Path 6	∞	2	3	2	J	q2_reg/D	1.906	1.106	0.800	∞	input port clock
Path 7	∞	1	1	3	q1_reg/C	Q_reg/D	0.808	0.456	0.352	∞	
Path 8	∞	1	1	3	q2_reg/C	Qb_reg/D	0.808	0.456	0.352	∞	

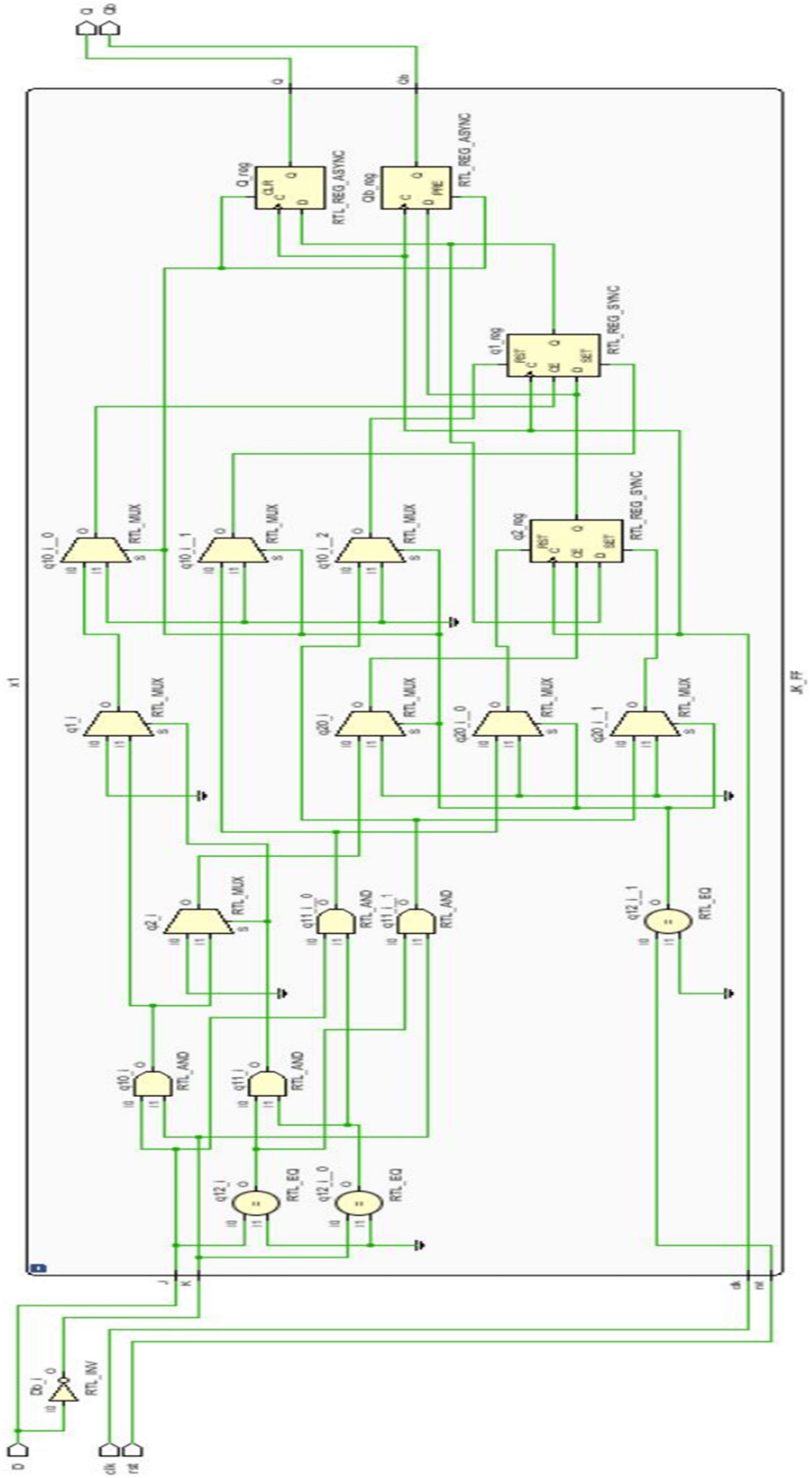
Maximum Combinational Delay: 4.076nSec

Aim: Write a VHDL Code to implement D Flipflop

Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity D_FF is
   Port ( clk : in STD_LOGIC;
          rst : in STD_LOGIC;
          D : in STD_LOGIC;
          Q : out STD_LOGIC;
          Qb : out STD_LOGIC);
end D_FF;

architecture Behavioral of D_FF is
component JK_FF is
Port ( clk : in STD_LOGIC;
          rst : in STD_LOGIC;
          J : in STD_LOGIC;
          K : in STD_LOGIC;
          Q : out STD_LOGIC;
          Qb : out STD_LOGIC);
end component JK_FF;
signal Db:STD_LOGIC;

begin
Db<= not D;
x1:JK_FF port map(clk,rst,D,Db,Q,Qb);


end Behavioral;
```

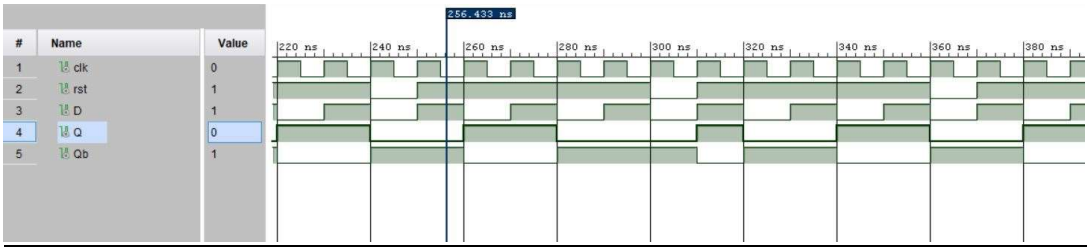
RTL DIAGRAM:


x1
JK_FF
RTL_REG_ASYNC
RTL_REG_SYNC
RTL_MUX
RTL_AND
RTL_EQ
RTL_INV

Test bench Code :

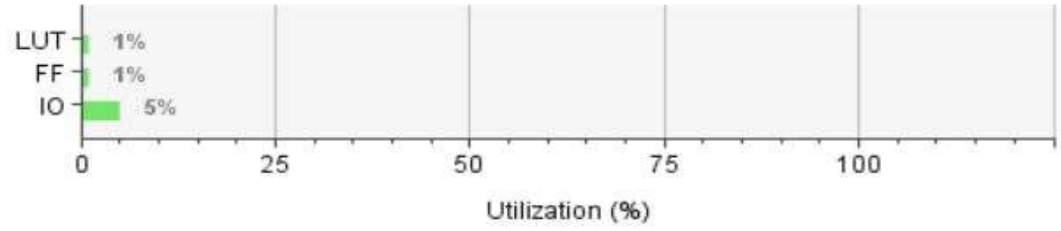
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Tb_D_FF is
-- Port ( );
end Tb_D_FF;

architecture Behavioral of
Tb_D_FF is
component D_FF is
Port ( clk : in STD_LOGIC;
       rst : in STD_LOGIC;
       D : in STD_LOGIC;
       Q : out STD_LOGIC;
       Qb : out STD_LOGIC);
end component D_FF;
signal clk,rst,D,Q,Qb:std_logic;
begin
x1:D_FF port map(clk,rst,D,Q,Qb);
   process
   begin
   clk<='1';
   wait for 5ns;
   clk<='0';
   wait for 5ns;
   end process;
    process
    begin
    rst<='0';
    wait for 10ns;
    rst<='1';
    wait for 50ns;
    end process;
    Process
    begin
    D<='0';
    wait for 10ns;
    D<='1';
    wait for 10ns
   end process;

end Behavioral;
```

SIMULATION WAVEFORM :



SYNTHESIS SUMMARY:

Resource	Utilization	Available	Utilization %
LUT	2	17600	0.01
FF	4	35200	0.01
IO	5	100	5.00



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	2	1	x1/Q_reg/C	Q	4.076	3.276	0.800	∞	
Path 2	∞	2	2	1	x1/Qb_reg/C	Qb	4.076	3.276	0.800	∞	
Path 3	∞	2	3	3	rst	x1/Q_reg/CLR	2.693	1.106	1.587	∞	input port clock
Path 4	∞	2	3	3	rst	x1/Qb_reg/PRE	2.693	1.106	1.587	∞	input port clock
Path 5	∞	2	3	3	rst	x1/q1_reg/D	1.932	1.132	0.800	∞	input port clock
Path 6	∞	2	3	2	D	x1/q2_reg/D	1.906	1.106	0.800	∞	input port clock
Path 7	∞	1	1	2	x1/q1_reg/C	x1/Q_reg/D	0.801	0.456	0.345	∞	
Path 8	∞	1	1	2	x1/q2_reg/C	x1/Qb_reg/D	0.801	0.456	0.345	∞	

Maximum Combinational Delay: 4.076nSec