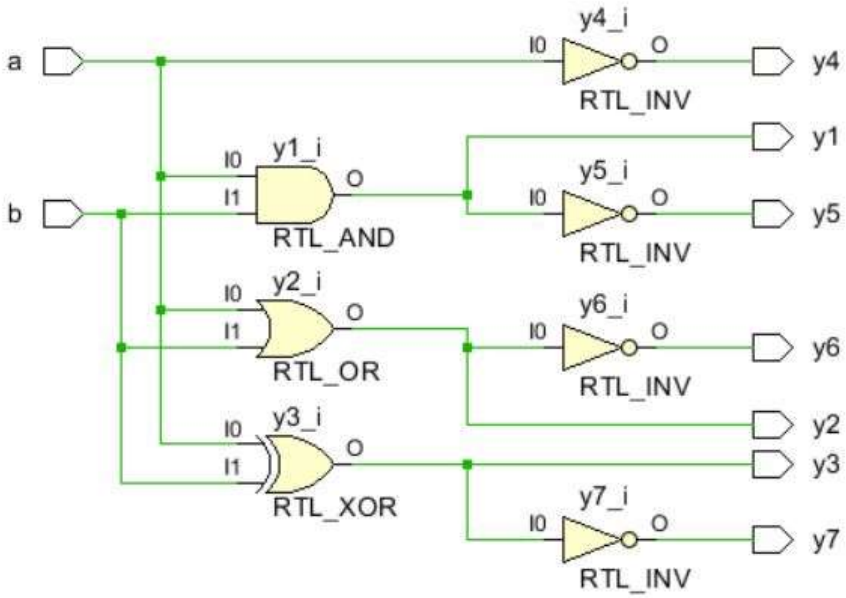
Practical 1

Aim: Write a VHDL code to implement basic gates.

Code:

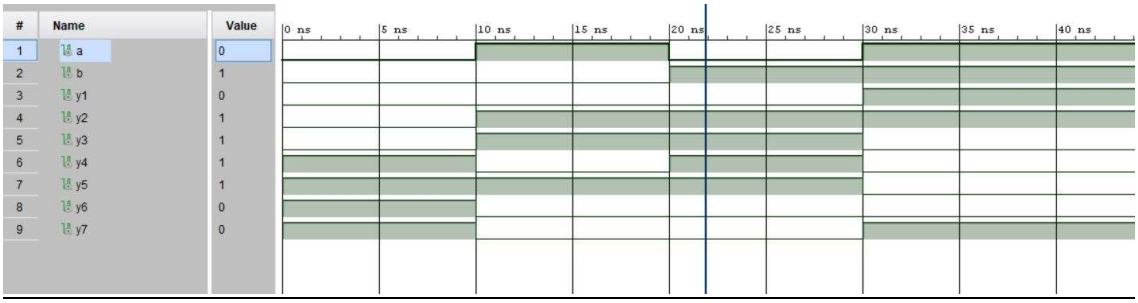
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity basic_gates is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
y1 : out STD_LOGIC;
y2 : out STD_LOGIC;
y3 : out STD_LOGIC;
y4 : out STD_LOGIC;
y5 : out STD_LOGIC;
y6 : out STD_LOGIC;
y7 : out STD_LOGIC);
end basic_gates;

architecture Behavioral of basic_gates is

begin
y1<= a and b;
y2<= a or b;
y3<= a xor b;
y4<= not a;
y5<= not ( a and b);
y6<= not ( a or b);
y7<= not ( a xor b);

end Behavioral;
```

RTL DIAGRAM:



```
library IEEE;
use
IEEE.STD_LOGIC_1164.ALL;
entity Tb_basic_gates is
--  Port ( );
end Tb_basic_gates;

architecture Behavioral of
Tb_basic_gates is
component basic_gates is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
y1 : out STD_LOGIC;
y2 : out STD_LOGIC;
y3 : out STD_LOGIC;
y4 : out STD_LOGIC;
y5 : out STD_LOGIC;
y6 : out STD_LOGIC;
y7 : out STD_LOGIC);

end component
basic_gates;

signal
a,b,y1,y2,y3,y4,y5,y6,y7:st
d_logic;
begin
x1:basic_gates port
map(a,b,y1,y2,y3,y4,y5,y6,
y7);
process
begin
a<='0';
b<='0';
wait for 10ns;

a<='1';
b<='0';
wait for 10ns;

a<='0';
b<='1';
wait for 10ns;

a<='1';
b<='1';
wait;

end process;
end Behavioral;
```

SIMULATION WAVEFORM :



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	4	7	a	y1	5.377	3.778	1.599	∞	input port clock
Path 2	∞	3	4	6	b	y3	5.377	3.778	1.599	∞	input port clock
Path 3	∞	3	4	6	b	y6	5.377	3.778	1.599	∞	input port clock
Path 4	∞	3	4	6	b	y2	5.351	3.752	1.599	∞	input port clock
Path 5	∞	3	4	7	a	y4	5.351	3.752	1.599	∞	input port clock
Path 6	∞	3	4	7	a	y5	5.351	3.752	1.599	∞	input port clock
Path 7	∞	3	4	6	b	y7	5.351	3.752	1.599	∞	input port clock

SYNTHESIS SUMMARY:

Resource	Utilization	Available	Utilization %
LUT	4	17600	0.02
IO	9	100	9.00

Maximum Combinational Delay: 5.377nSec