

## **Practical 4**

**Aim:** Write a VHDL code for 4 bit ripple carry adder using loop statement.

### **Code:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity ripplecarryadder_4bit is
    Port ( a : in STD_LOGIC_VECTOR (0 to 3);
          b : in STD_LOGIC_VECTOR (0 to 3);
          cin : in STD_LOGIC;
          s : out STD_LOGIC_VECTOR (0 to 3);
          cout : out STD_LOGIC);
end ripplecarryadder_4bit;

architecture Behavioral of ripplecarryadder_4bit is

begin

    process(a,b,cin)

        variable i:INTEGER:=0;
        variable c:std_logic_vector(0 to 4):="00000";

        begin
            c(0):=cin;

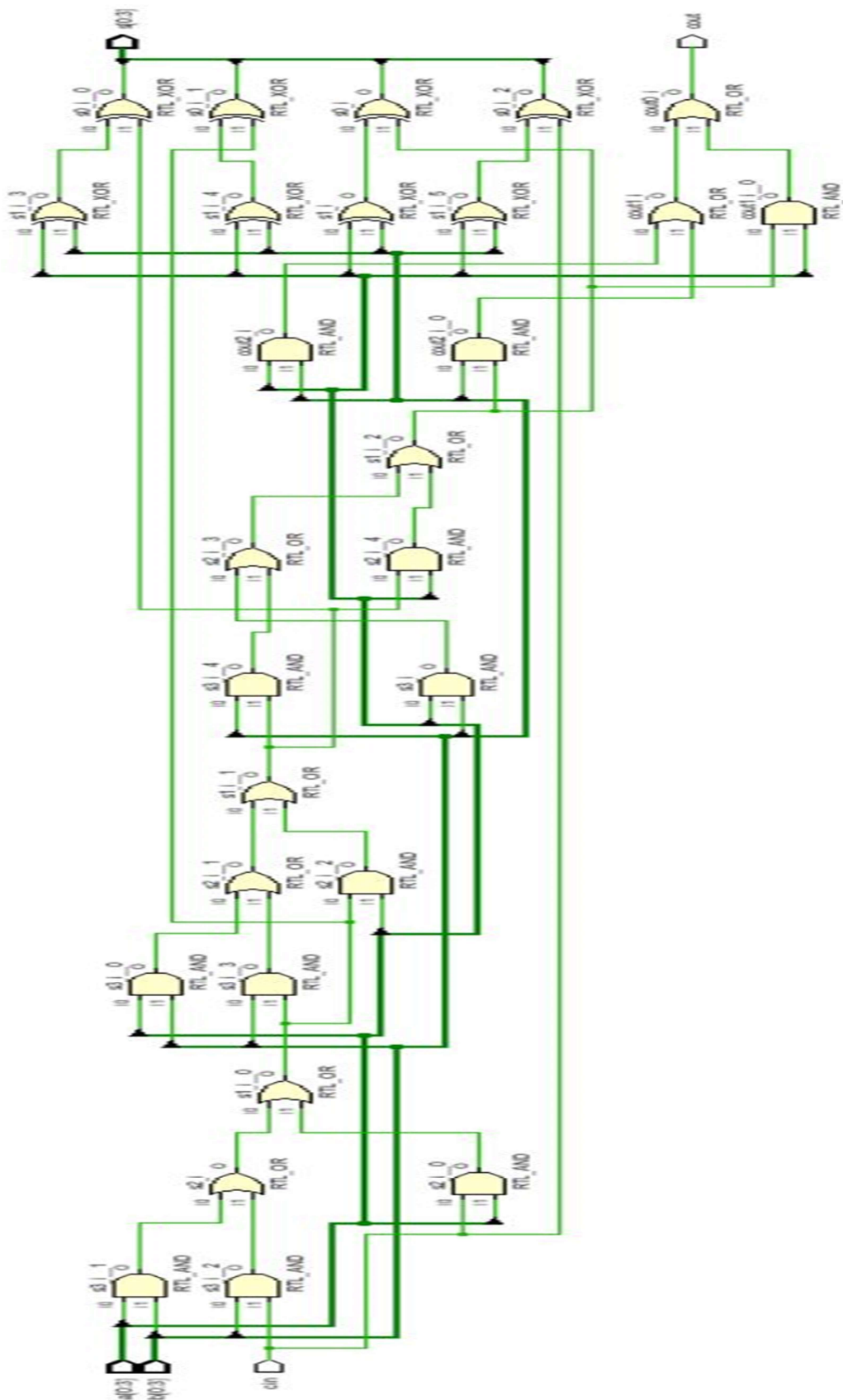
            lop: for i in 0 to 3 loop

                s(i)<=a(i) xor b(i) xor c(i);
                c(i+1):=(a(i) and b(i)) or (b(i) and c(i)) or (c(i) and a(i));

            end loop lop;
            cout <= c(4);
        end process;

    end Behavioral;
```

RTL DIAGRAM:



library	signal a :	b<="0111"	wait for	b<="1000"	wait for	b<="1001"	wait for	b<="1010"	wait for	b<="1011"	wait for
IEEE;	STD_LOG	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;
use	IC_VECT	wait for	b<="1000"	wait for	b<="1001"	wait for	b<="1010"	wait for	b<="1011"	wait for	b<="1100"
IEEE.STD	OR (0 to	b<="1000"	wait for	b<="1001"	wait for	b<="1010"	wait for	b<="1011"	wait for	b<="1100"	wait for
_LOGIC_1	3);	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;
164.ALL;	signal b :	wait for	b<="1001"	wait for	b<="1010"	wait for	b<="1011"	wait for	b<="1100"	wait for	b<="1101"
entity	STD_LOG	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;
Tb_ripple	IC_VECT	b<="1001"	wait for	b<="1010"	wait for	b<="1011"	wait for	b<="1100"	wait for	b<="1101"	wait for
carryadd	OR (0 to	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;
er_4bit	is 3);	wait for	b<="1010"	wait for	b<="1011"	wait for	b<="1100"	wait for	b<="1101"	wait for	b<="1110"
-- Port (	signal cin	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;
);	:STD_LO	b<="1010"	wait for	b<="1011"	wait for	b<="1100"	wait for	b<="1101"	wait for	b<="1110"	wait for
end	GIC;	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;
Tb_ripple	signal s :	wait for	b<="1011"	wait for	b<="1100"	wait for	b<="1101"	wait for	b<="1110"	wait for	b<="1111"
carryadd	STD_LOG	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;
er_4bit;	IC_VECT	b<="1011"	wait for	b<="1100"	wait for	b<="1101"	wait for	b<="1110"	wait for	b<="1111"	wait for
	;	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;	50ns;
	OR (0 to	wait for	b<="1100"	wait for	b<="1101"	wait for	b<="1110"	wait for	b<="1111"	wait for	
architect	3);	10ns;	;	10ns;	;	10ns;	;	10ns;	;	50ns;	a<="1010"
ure	signal	b<="1100"	wait for	b<="1101"	wait for	b<="1110"	wait for	b<="1111"	wait for	;	;
Behavior	cout	;	10ns;	;	10ns;	;	10ns;	;	50ns;	a<="1001"	b<="0000"
al of	:STD_LO	wait for	b<="1101"	wait for	b<="1110"	wait for	b<="1111"	wait for	;	;	;
Tb_ripple	GIC;	10ns;	;	10ns;	;	10ns;	;	50ns;	a<="1000"	b<="0000"	wait for
carryadd	begin	b<="1101"	wait for	b<="1110"	wait for	b<="1111"	wait for	;	;	;	10ns;
er_4bit	is	;	10ns;	;	10ns;	;	50ns;	a<="0111"	b<="0000"	wait for	b<="0001"
componen	u1:ripple	wait for	b<="1110"	wait for	b<="1111"	wait for	;	;	;	10ns;	;
nt	carryadd	10ns;	;	10ns;	;	50ns;	a<="0110"	b<="0000"	wait for	b<="0001"	wait for
ripplecar	er_4bit	b<="1110"	wait for	b<="1111"	wait for	;	;	;	10ns;	;	10ns;
yadder_4	port	;	10ns;	;	50ns;	a<="0101"	b<="0000"	wait for	b<="0001"	wait for	b<="0010"
bit is	map(a,b,	wait for	b<="1111"	wait for	;	;	10ns;	;	10ns;	;	;
Port (a	cin,s,cout	10ns;	;	50ns;	a<="0100"	b<="0000"	wait for	b<="0001"	wait for	b<="0010"	wait for
: in	);	b<="1111"	wait for	;	;	10ns;	;	10ns;	;	10ns;	;
STD_LOG	process	;	50ns;	a<="0010"	b<="0000"	wait for	b<="0001"	wait for	b<="0010"	wait for	b<="0011"
IC_VECT	begin	wait for	;	;	10ns;	;	10ns;	;	10ns;	;	10ns;
OR (0 to	cin<='0';	a<="0001"	b<="0000"	wait for	b<="0001"	wait for	b<="0010"	wait for	b<="0011"	wait for	b<="0100"
3);	a<="0000"	;	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;
b :	b<="0000"	b<="0000"	wait for	b<="0001"	wait for	b<="0010"	wait for	b<="0011"	wait for	b<="0100"	wait for
in	;	b<="0000"	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;
STD_LOG	;	wait for	b<="0001"	wait for	b<="0010"	wait for	b<="0011"	wait for	b<="0100"	wait for	b<="0101"
IC_VECT	wait for	10ns;	;	10ns;	;	10ns;	;	10ns;	;	10ns;	;
OR (0 to	10ns;	b<="0001"	wait for	b<="0010"	wait for	b<="0011"	wait for	b<="0100"	wait for	b<="0101"	wait for
3);	b<="0001"	;	10ns;	;</							

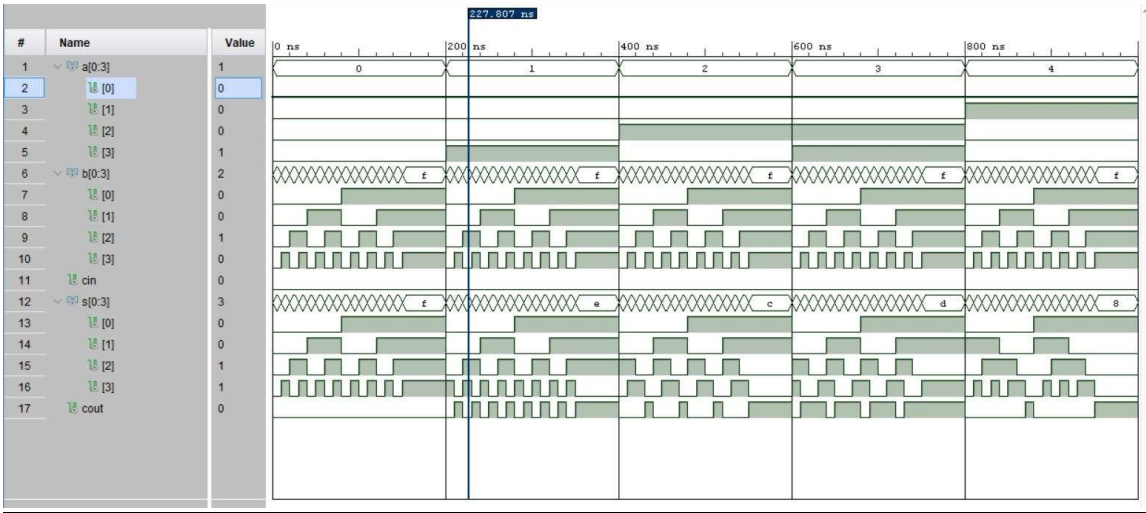
[illegible]

```

b<="0111" wait for wait for b<="1010" wait for b<="0001" b<="1101" wait for b<="0100" a<="1110" wait for b<="0111"
; 10ns; 10ns; ; 10ns; ; ; 10ns; ; 10ns; ;
wait for b<="0011" b<="1111" wait for b<="0110" wait for wait for b<="1001" wait for b<="0000" b<="1100" wait for
10ns; ; ; 10ns; ; 10ns; 10ns; ; 10ns; ; 10ns;
b<="1000" wait for wait for b<="1011" wait for b<="0010" b<="1110" wait for b<="0101" wait for wait for b<="1000"
; 10ns; 50ns; ; 10ns; ; ; 10ns; ; 10ns; ;
wait for b<="0100" ; wait for b<="0111" wait for wait for b<="1010" wait for b<="0001" b<="1101" wait for
10ns; ; a<="1001" 10ns; ; 10ns; 10ns; ; 10ns; ; ; 10ns;
b<="1001" wait for ; b<="1100" wait for b<="0011" b<="1111" wait for b<="0110" wait for wait for b<="1001"
; 10ns; b<="0000" ; 10ns; ; ; 10ns; ; 10ns; ;
wait for b<="0101" ; wait for b<="1000" wait for wait for b<="1011" wait for b<="0010" b<="1110" wait for
10ns; ; wait for 10ns; ; 10ns; 50ns; ; 10ns; ; ; 10ns;
b<="1010" wait for 10ns; b<="1101" wait for b<="0100" wait for b<="0111" wait for wait for b<="1010"
; 10ns; b<="0001" ; 10ns; ; a<="1100" 10ns; ; 10ns; 10ns; ;
wait for b<="0110" ; wait for b<="1001" wait for ; b<="1100" wait for b<="0011" b<="1111" wait for
10ns; ; wait for 10ns; ; 10ns; b<="0000" ; 10ns; ; ; 10ns;
b<="1011" wait for 10ns; b<="1110" wait for b<="0101" ; wait for b<="1000" wait for wait for b<="1011"
; 10ns; b<="0010" ; 10ns; ; wait for 10ns; ; 10ns; 50ns; ;
wait for b<="0111" ; wait for b<="1010" wait for 10ns; b<="0001" ; 10ns; ; a<="1111" 10ns;
10ns; ; wait for 10ns; ; 10ns; b<="1111" wait for ; b<="1001" wait for ; b<="1100"
b<="1100" wait for 10ns; b<="1111" wait for b<="0110" ; wait for b<="1001" wait for ; b<="0000" ;
; 10ns; b<="0011" ; 10ns; ; wait for 10ns; ; 10ns; b<="0000" ;
wait for b<="1000" ; wait for b<="1011" wait for 10ns; b<="1110" wait for b<="0101" ; wait for
10ns; ; wait for 50ns; ; 10ns; b<="0010" ; 10ns; ; wait for 10ns;
b<="1101" wait for 10ns; wait for b<="0111" ; wait for b<="1010" wait for 10ns; b<="1101"
; 10ns; b<="0100" a<="1010" 10ns; ; wait for 10ns; ; 10ns; b<="0001" ;
wait for b<="1001" ; ; b<="1100" wait for 10ns; b<="1111" wait for b<="0110" ; wait for
10ns; ; wait for b<="0000" ; 10ns; b<="0011" ; 10ns; ; wait for 10ns;
b<="1110" wait for 10ns; ; wait for b<="1000" ; wait for b<="1011" wait for 10ns; b<="1110"
; 10ns; b<="0101" wait for 10ns; ; wait for 50ns; ; 10ns; b<="0010" ;
wait for b<="1010" ; 10ns; b<="1101" wait for 10ns; wait for b<="0111" ; wait for
10ns; ; wait for b<="0001" ; 10ns; b<="0100" a<="1101" 10ns; ; wait for 10ns;
b<="1111" wait for 10ns; ; wait for b<="1001" ; ; b<="1100" wait for 10ns; b<="1111"
; 10ns; b<="0110" wait for 10ns; ; wait for b<="0000" ; 10ns; b<="0011" ;
wait for b<="1011" ; 10ns; b<="1110" wait for 10ns; ; wait for b<="1000" ; wait for
50ns; ; wait for b<="0010" ; 10ns; b<="0101" wait for 10ns; ; wait for 50ns;
wait for 10ns; ; wait for b<="1010" ; 10ns; b<="1101" wait for 10ns;
a<="1000" 10ns; b<="0111" wait for 10ns; ; wait for b<="0001" ; 10ns; b<="0100" end
; b<="1100" ; 10ns; b<="1111" wait for 10ns; ; wait for b<="1001" ; process;
b<="0000" ; wait for b<="0011" ; 10ns; b<="0110" wait for 10ns; ; wait for end
; wait for 10ns; ; wait for b<="1011" ; 10ns; b<="1110" wait for 10ns; Behavioral
wait for 10ns; b<="1000" wait for 50ns; ; wait for b<="0010" ; 10ns; b<="0101" ;
10ns; b<="1101" ; 10ns; wait for 10ns; ; wait for b<="1010" ;
b<="0001" ; wait for b<="0100" a<="1011" 10ns; b<="0111" wait for 10ns; ; wait for
; wait for 10ns; ; b<="1100" ; 10ns; b<="1111" wait for 10ns;
wait for 10ns; b<="1001" wait for b<="0000" ; wait for b<="0011" ; 10ns; b<="0110"
10ns; b<="1110" ; 10ns; ; wait for 10ns; ; wait for b<="1011" ;
b<="0010" ; wait for b<="0101" wait for 10ns; b<="1000" wait for 50ns; ; wait for
; 10ns; ; 10ns;

```

**SIMULATION WAVEFORM :**



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	4	5	3	a[0]	cout	5.970	3.904	2.066	∞	input port clock
Path 2	∞	4	5	3	a[0]	s[2]	5.970	3.904	2.066	∞	input port clock
Path 3	∞	4	5	3	a[0]	s[3]	5.964	3.898	2.066	∞	input port clock
Path 4	∞	3	4	3	cin	s[0]	5.351	3.752	1.599	∞	input port clock
Path 5	∞	3	4	3	a[0]	s[1]	5.351	3.752	1.599	∞	input port clock

**SYNTHESIS SUMMARY:**

Resource	Utilization	Available	Utilization %
LUT	4	17600	0.02
IO	14	100	14.00

Maximum Combinational Delay: 5.970nSec