

## Assignment 8

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### Cache Simulator

Cache simulator is written in C++ which gives number of hits and miss ratio for the given address file. The simulator gives the ratio for cache implemented with Direct Mapping function and 2-way set associative function with LRU and FIFO as replacement algorithms.

Bytes/Method	1024	2048	4096	8192	16384
<b>Direct</b>	1.00E+00	1.00E+00	9.87E-07	9.87E-07	2.96E-06
<b>2-Way_LRU</b>	1.00E+00	1.98E-06	1.98E-06	1.98E-06	1.98E-06
<b>2-Way_FIFO</b>	1.00E+00	1.98E-06	1.98E-06	1.98E-06	1.98E-06

The above table displays the hit rate for the different mapping with different replacement algorithms for the given address file. But it can be seen that for the given address file it is not easy to come to any conclusion. So that's why I have also use my own created address file to get a clear observation.

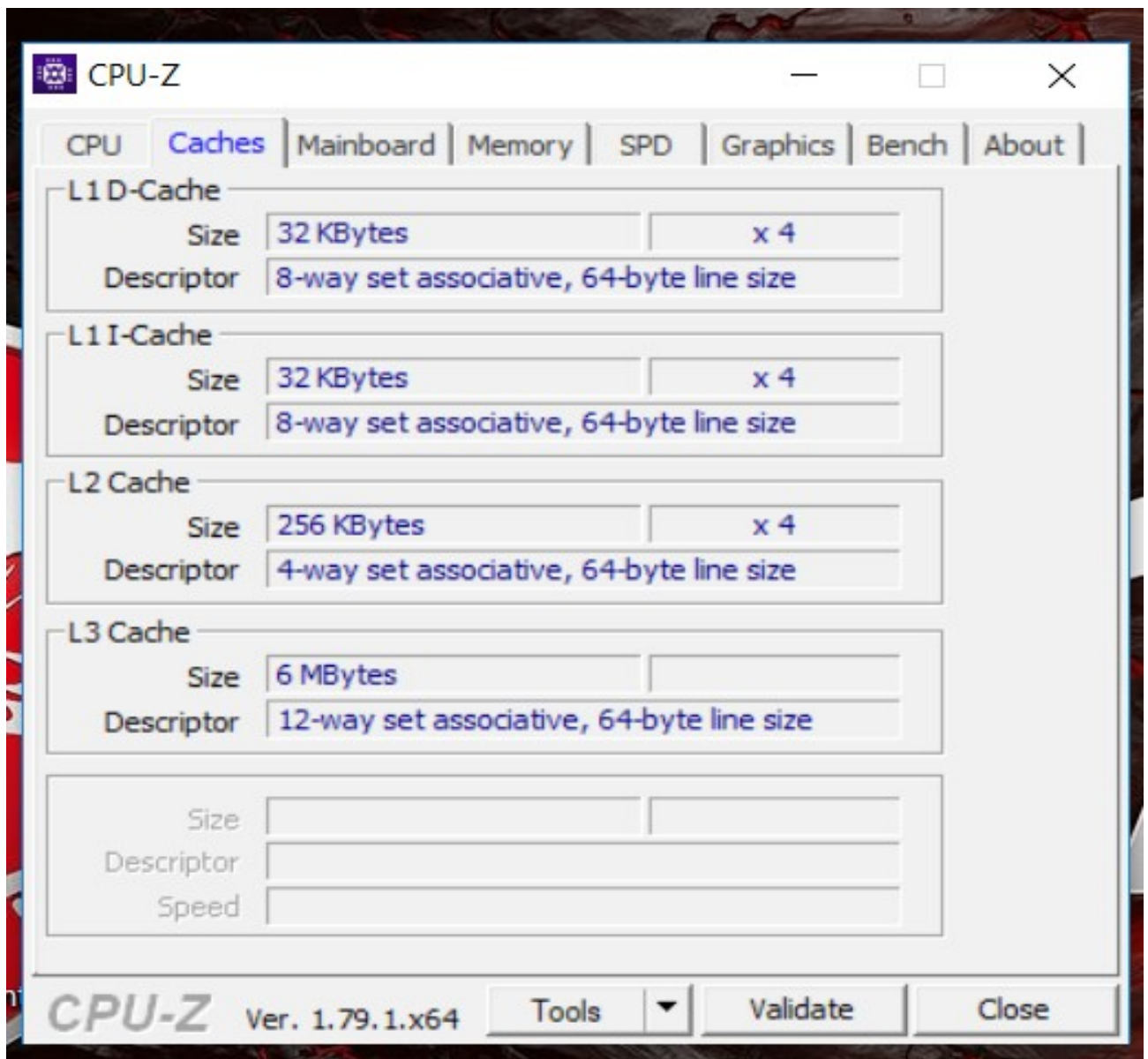
Bytes/Method	1024	2048	4096	8192	16384
<b>Direct</b>	0.5843247	0.5856023	0.5927234	0.5945364	0.5975465
<b>2-Way_FIFO</b>	0.5923465	0.5934566	0.5945623	0.5955654	0.5978451
<b>2-Way_LRU</b>	0.6146626	0.6148957	0.6155656	0.6162155	0.6175646

So from the second table it can be clearly seen that 2-Way LRU method is ahead of the Direct method and 2-way FIFO method.

This is because 2-Way set associative method is a moderation between direct and associative mapping which is complemented by LRU as replacement algorithm which is surely a logical choice over FIFO method.

## Cache Details of my Laptop

```
suryavanshi@MSI-GE63VR-7RE:~$ lscpu
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                 8
On-line CPU(s) list:   0-7
Thread(s) per core:    2
Core(s) per socket:    4
Socket(s):              1
NUMA node(s):          1
Vendor ID:              GenuineIntel
CPU family:             6
Model:                 158
Model name:             Intel(R) Core(TM) i7-7700HQ CPU @ 2.80GHz
Stepping:              9
CPU MHz:               831.071
CPU max MHz:           3800.0000
CPU min MHz:           800.0000
BogoMIPS:              5616.00
Virtualization:         VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              256K
L3 cache:              6144K
NUMA node0 CPU(s):     0-7
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs
bts rep_good nopl xtopology nonstop_tsc cpuid aperfnperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_t
imer aes xsave avx f16c rdrand lahf_lm abn 3dnowprefetch cpuid_fault epb invpcid_single pti tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 avx2 snep bmi2 erms invpcid mpx rdseed adx snap c
lflushopt intel_pt xsaveopt xsavec xgetbv1 xsaves dtherm ida arat pln pts hwp hwp_notify hwp_act_window hwp_epp
```



Details/Cache	Size (in KB)	Type
L1-D	128	8-way set associative
L1-I	128	8-way set associative
L2	1024	4-way set associative
L3	6144	12-way set associative

