CMOS Voltage Controlled Oscillator

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***Abstract*— This paper is a submission for the Analog IC Hackathon conducted by IITH and VSD along with SYNOPSYS in Feb 2022. The proposed circuit is a Voltage Controlled Oscillator that produces a tunable output frequency as a function of input voltage. The VCO is implemented using CMOS (Complementary Metal-Oxide Semiconductor) that's current starved and operate ~ 50MHz.**

1. Reference Circuit Details

The VCO has a 5 inverter stages arranged in a ring oscillator configuration. The inverter delays are controlled through current sources M10 to M19 - which limit the current to the inverters. As a linear current relationship is needed between the bias current and control voltage, a 41k resistor in series with M27 holds the gate voltage of M27 near threshold voltage. M20-M23 form the two buffers that reduce capacitive load that may change oscillation frequency. The referenced design should produce a 7MHz to 105Mhz output for a control voltage range of 400mV to 1.6V with a frequency to voltage constant of 92MHz per volt. VCOs are an important building block in PLL - Phase-Locked Loop, used widely in clock generation for SoC.

Further goals are to develop a dual output - triangular and square waveform

2. Reference Circuit Diagram

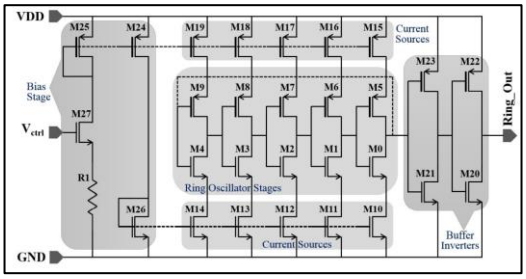

Fig1. Current Starved VCO [1]

3. Reference Circuit Waveforms

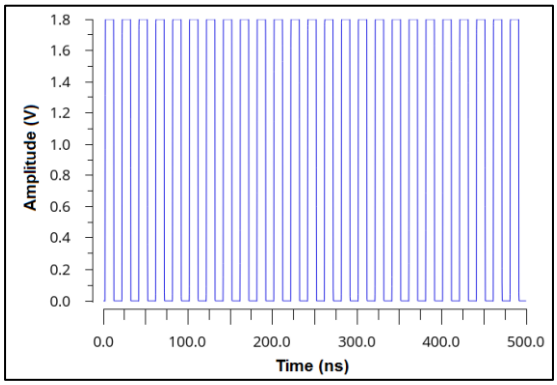

Fig2. Simulation result of VCO [1]

References

[1] Shekhar, Chandra & Qureshi, S. (2018). Design and Analysis of Current Starved VCO Targeting SCL 180 nm CMOS Process. 86-89. 10.1109/iSES.2018.00027.

[2] Razavi, Behzad. Design of analog CMOS integrated circuits. ISBN 0-07-238032-2