Realizing 4:16 Decoder using 2:4 Decoders

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Abstract

Decoders are combinational circuits that take n inputs and give output in 2^n lines, which are high or low in a combination unique to the input. Decoders are made from circuits comprising basic gates, typically NOT gates and AND gates. This paper attempts to construct a 4:16 decoder using 2:4 decoders to understand the modular nature of decoder circuits. The circuit would use CMOS transistor logic, implemented using eSim and SkyWaterPDK.

1. Reference Circuit Details

Each 2:4 decoder submodule has two inputs A and B which produce unique outputs at the 4 output lines D0, D1, D2 and D3. A and B are the MSB and LSB of the input respectively which can select just one output line at a time, in other words only one output line of a decoder can be high at any given time. The Boolean function for each output follows the combination of product terms D0 = A'B', D1 = A'B, D2 = A,B' and D3 = A,B. The inversion of the inputs is achieved using NOT gates and each product term has it's AND gate. NOT gates are implemented using LECTOR technique where two extra transistors are used as leakage control transistors that are connected between the pull-up and pull-down circuit within the logic gate to reduce power consumption by reducing leakage current. In the 4:16 implementation, 5 2:4 decoders are used , where the enable lines of the decoders are connected to the input combination to achieve desired output.

2. Reference Circuit

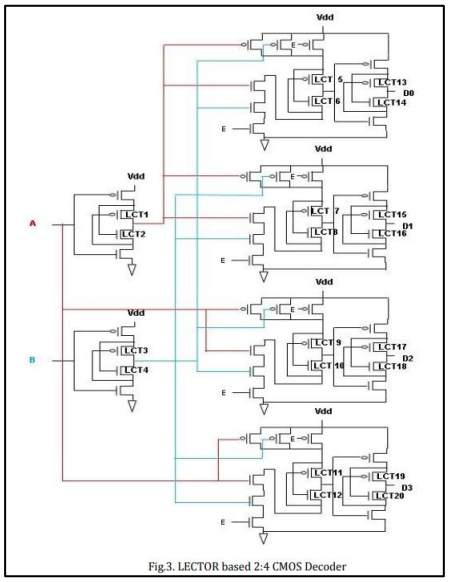

Fig. 1[1]

3. Reference Circuit Waveforms

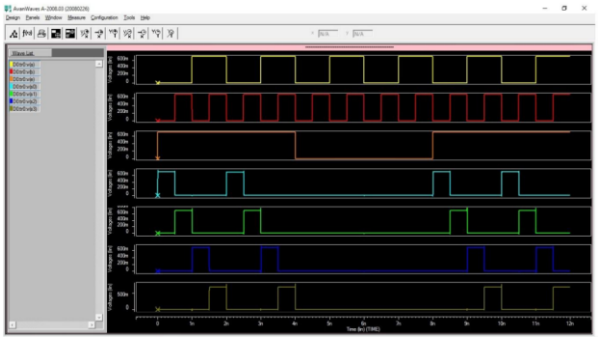

Fig. 2[2]

References

[1]. Rajbeer Singh, Manoj Kumar Bandil "An Analysis of CMOS based Low Power 2:4 Decoder at 32nm node using LECTOR Technique" IRJET, vol. 6, issue. 12, pp. 732, Dec. 2019

[2]. Rajbeer Singh, Manoj Kumar Bandil "An Analysis of CMOS based Low Power 2:4 Decoder at 32nm node using LECTOR Technique" IRJET, vol. 6, issue. 12, pp. 733, Dec. 2019