

**SCHOOL OF ENGINEERING AND TECHNOLOGY**

**Department of Electronics and Communication Engineering**

**EC631 *–* VLSI DESIGN LABORATORY**

**NAME: PREM KUMAR R REG. NO: 1960628 YEAR/BRANCH: 3/ECE SEMESTER: 6th**

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**CHRIST (DEEMED TO BE UNIVERSITY) SCHOOL OF ENGINEERING AND TECHNOLOGY**

## Mysore Road, Kanmanike, Bangalore – 560074

**LABORATORY CERTIFICATE**

This is to certify that **Mr./Ms**. …Prem Kumar R…….……………………… has satisfactorily completed the course of experiments in **EC631 - VLSI Design Laboratory** prescribed by the department of **Electronics and Communication Engineering, CHRIST (Deemed to be University)** for **VI** semester **Bachelor of Technology** Course in the laboratory of this university during the year **2021 – 2022**.

Signature of Staff-In charge

## Signature of Head of the Department

Name of the Candidate ………………………………………….

Register Number ………………………………………………...

Examination Center ……………………………………………...

Date of Practical Examination …………………………………...

Signature of the Examiners:

1.

2.

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## SYLLABUS

**EC631 - VLSI DESIGN LABORATORY**

**LIST OF EXPERIMENTS:**

1. Design Entry and Simulation of Combinational Logic circuits
   1. Basic logic gates
   2. Multiplexer and Demultiplexer
   3. Encoder and Decoder
   4. Half adder and Full adder
   5. Half Subtractor and Full Subtractor
   6. 8 bit adder
   7. 4 bit multiplier
2. Design Entry and Simulation of Sequential Logic Circuits
   1. Flip-Flops
   2. Counters
   3. Registers
3. Synthesis, P&R and Post P&R simulation for all the blocks/codes developed in Expt. No. 1 and No. 2.
4. Design Entry and Simulation of traffic signal controller using Xilinx ISE Design suite and implementing the same on Spartan FPGA.
5. Schematic and Layout of a simple CMOS inverter, parasitic extraction and simulation.
6. Design and simulation of pipelined serial and parallel adder to add/ subtract 8 number of size, 12 bits each in 2's complement.
7. Design and Implement a 4 digit seven segment display.

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO.** | **DATE** | **NAME OF THE EXPERIMENT** | **MARKS OBTAINED** | **SIGNATURE OF STAFF** |
| 1. |  | Design Entry and Simulation of Combinational Logic circuits |  |  |
| 1. a) | 12/01/20  22 | Basic logic gates |  |  |
| 1. b) | 12/01/20  22 | Multiplexer and De-multiplexer |  |  |
| 1. c) |  | Encoder and Decoder |  |  |
| 1. d) |  | Half adder and Full adder |  |  |
| 1. e) |  | Half subtractor and Full subtractor |  |  |
| 1. f) |  | 8-bit adder |  |  |
| 1. g) |  | 4-bit multiplier |  |  |
| 2. |  | Design Entry and Simulation of Sequential Logic Circuits |  |  |
| 2. a) |  | Flip-Flops |  |  |
| 2. b) |  | Counters |  |  |
| 2. c) |  | Registers |  |  |
| 3. |  | Synthesis, P&R and Post P&R simulation for all the blocks/codes developed in Expt. No. 1 and No. 2. |  |  |
| 4. |  | Design Entry and Simulation of traffic signal controllers using Xilinx Vivado |  |  |
| 5. |  | Layout of a simple CMOS inverter and simulation. |  |  |
| 6. |  | Design and Implement a Binary to Seven Segment Display |  |  |

**Completed/Incomplete Staff In-Charge Signature**

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**EX.NO: 1 DESIGN ENTRY AND SIMULATION OF COMBINATIONAL LOGIC CIRCUITS**

## DATE: 12/01/2022

**AIM:**

To verify the functionality and timing of your design or portion of your design. To interpret

Verilog code into circuit functionality and displays logical results of the described HDL to determine correct circuit operation and to create and verify complex functions in a relatively small amount of time.

## TOOLS REQUIRED:

1. Xilinx Vivado Design Suite: WebEdition

## PROCEDURE:

1. Start by clicking **Vivado Design Suite: WebEdition**
2. Go to **File** → **new project** → **Enter project name**, select the top level source as **HDL** & click **next**.
3. Enter **device properties** as

Product Category : General Purpose Family : Kintex 7

Device : xc7k70t Package :fbg484 Speed : -1

Top Level Source Type : HDL Synthesis Tool : XST (VHDL/Verilog) Simulator : ISim (VHDL/Verilog)

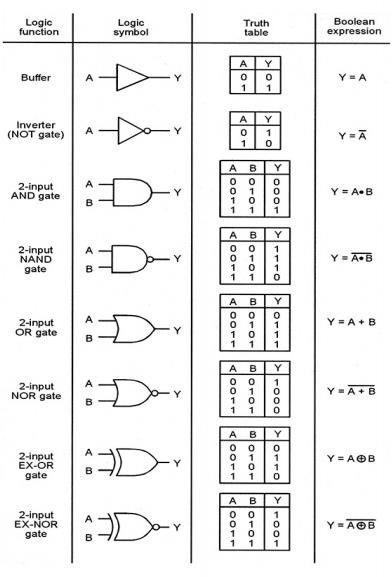
Preferred Language : Verilog & **Click next**.

1. **Right click** the device name (XCS3540) in the source window to create **new source**.
2. Select **Verilog module** and enter **file name** in the new source window & click **next**.
3. Write the **Verilog code** in the **Verilog editor window**.
4. Write the **testbench** by create **new source simulation source.**
5. Run Check syntax through **Process window**→ **synthesize**→ double click **Behavioral Check Syntax**→ and removes error if present, with proper syntax & coding.
6. Click on the symbol of FPGA device and then right click→ click on **new source**.
7. Select the desired parameters for simulating the design. In this case **combinational circuit**

and **simulation time** click **finish**.

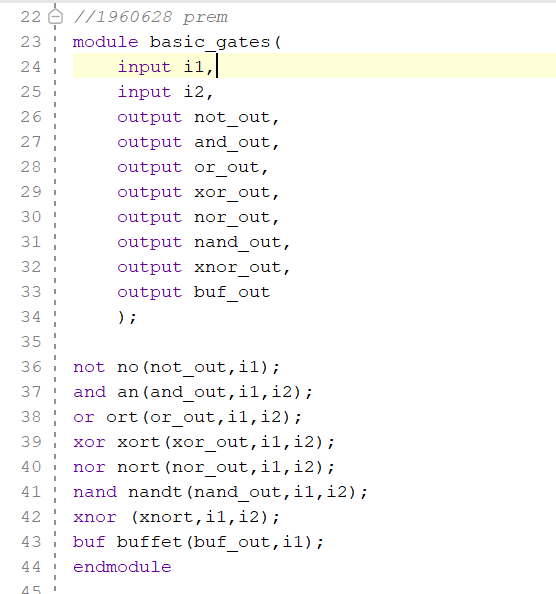
1. Assign **all input signal** (**high or low**) using just **click** on this and save file.
2. From the **source process window**. Click **Behavioral simulation** from drop-down menu.
3. Double click the **Simulation Behavioral Model**.
4. Verify your design in **wave window** by seeing behavior of output signal with respect to input signal.

## BASIC LOGIC GATES:

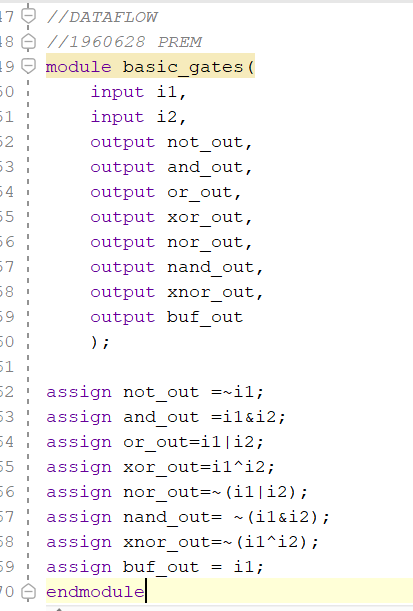


**PROGRAM:**

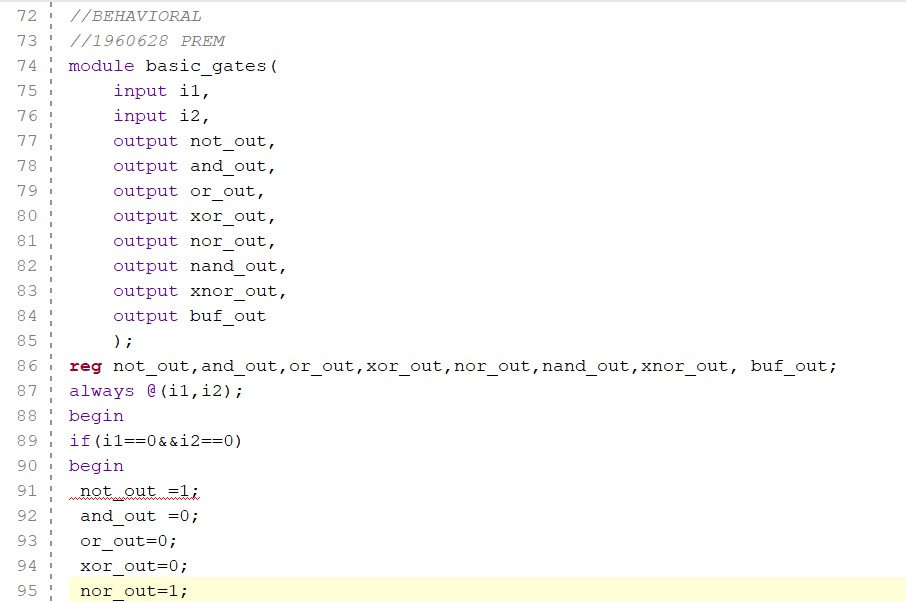
1. **BASIC LOGIC GATES:**
   1. **GATE LEVEL MODELING:**

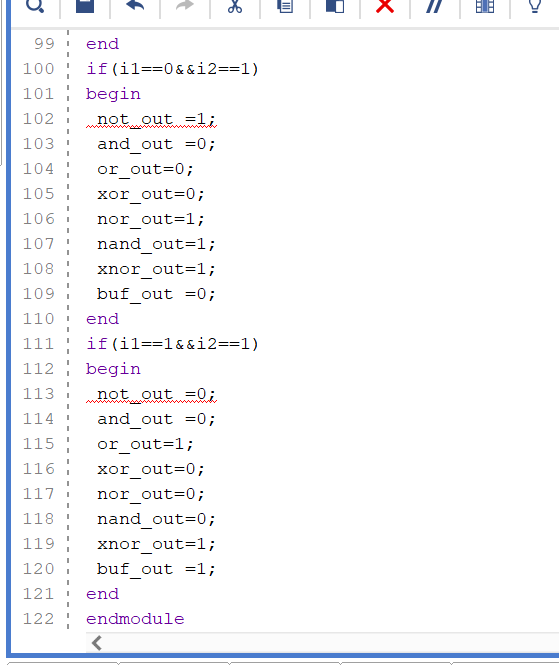


* 1. **DATAFLOW LEVEL MODELING:**

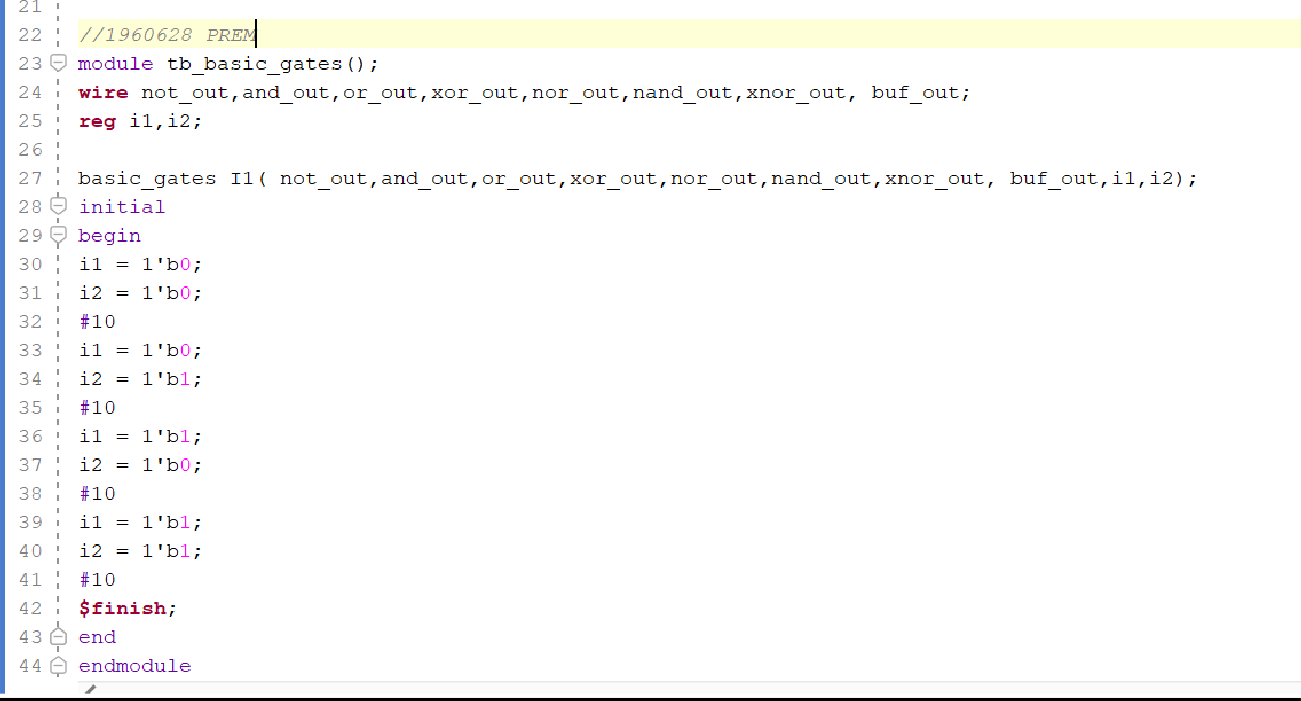


**BEHAVIORAL LEVEL MODELING:**

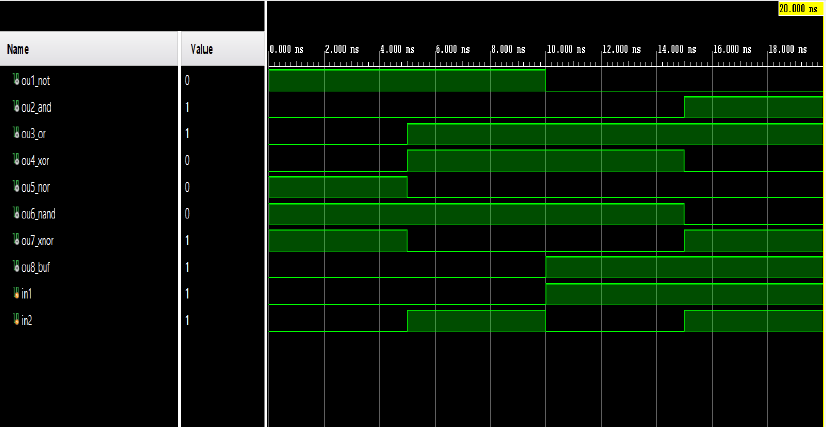




**TEST BENCH:**



**SIMULATION OUTPUT:**



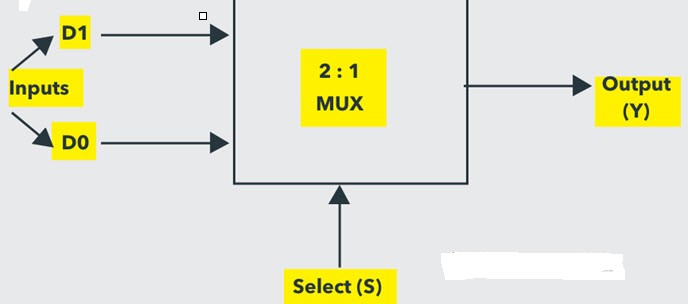
**Result:**

Thus the Verilog code was scripted, simulated and waveforms were verified using Xilinx Vivado Webpack.

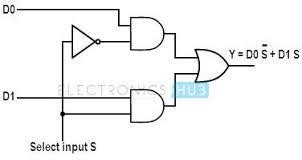
# Multiplexer and Demultiplexer:

**MULTIPLEXER (2x1):**

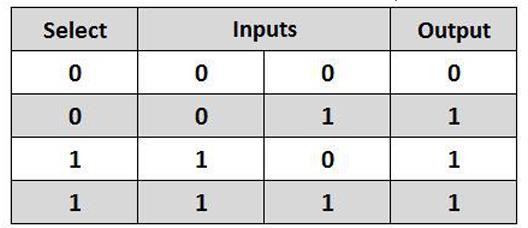
**Logic Symbol**



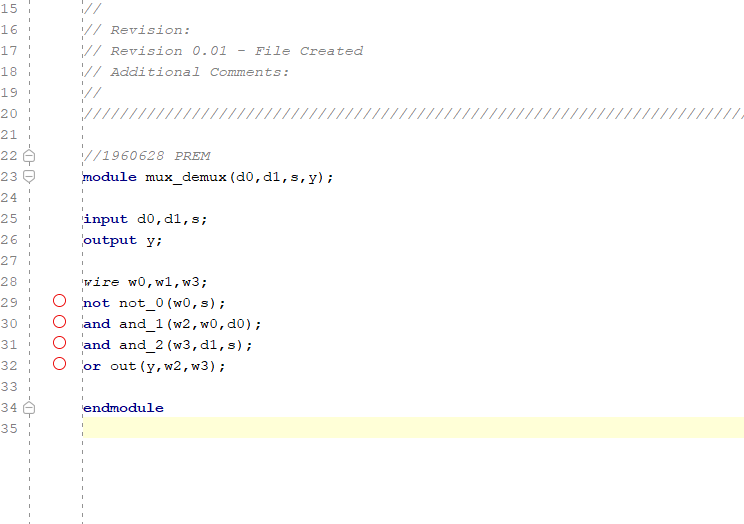
**Logic Circuit**

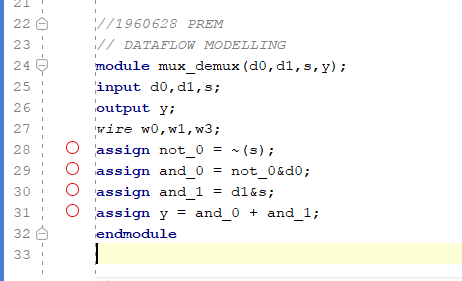


**Truth Table**

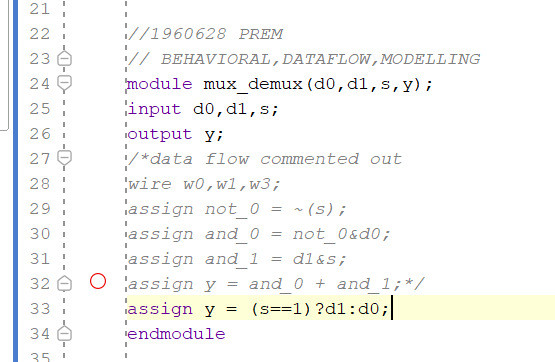


## PROGRAM

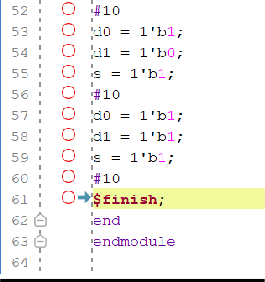
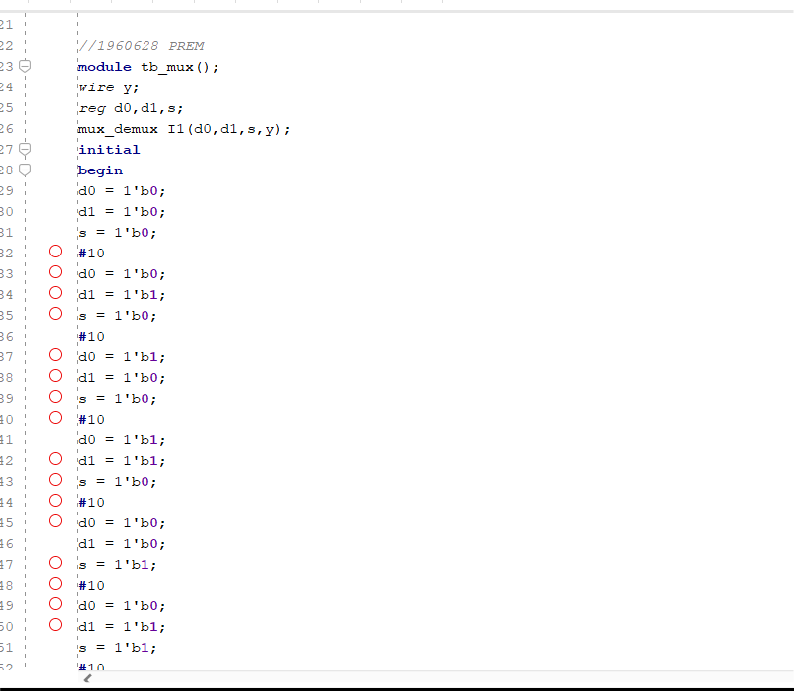
* 1. **GATE LEVEL MODELING:**
  2. **DATAFLOW LEVEL MODELING:**



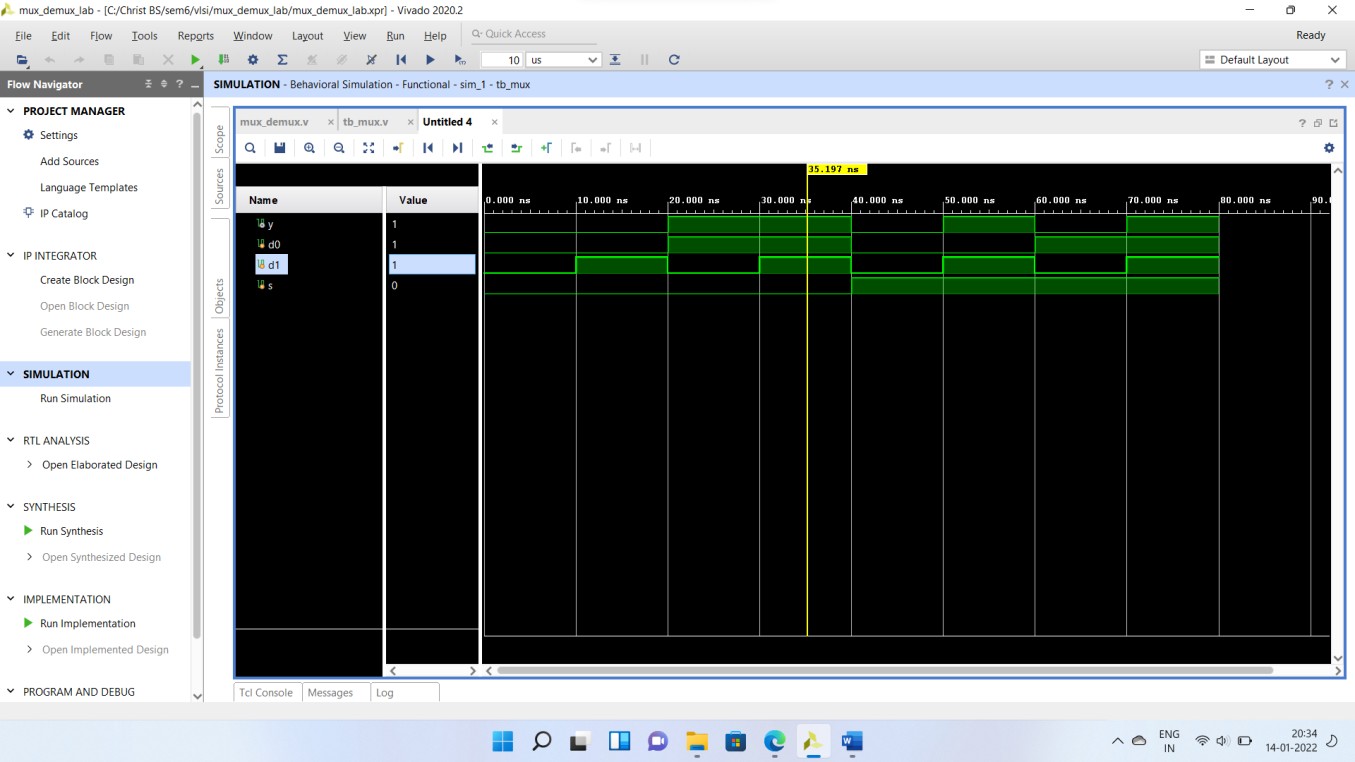
* 1. **BEHAVIORAL LEVEL MODELING:**



**TESTBENCH**

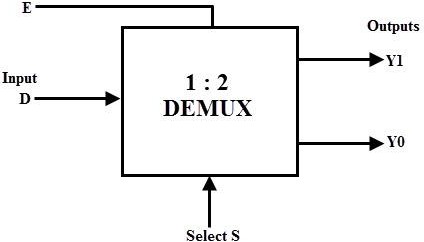


## SIMULATION OUTPUT

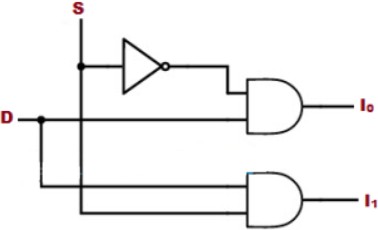


**DE-MULTIPLEXER (1x2):**

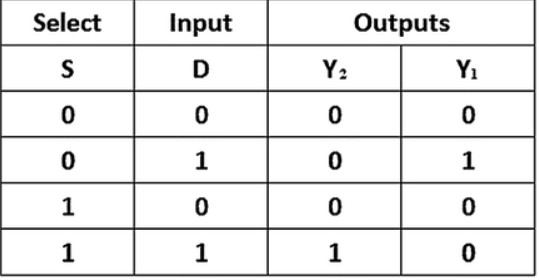
**Logic Symbol**



## Logic Circuit

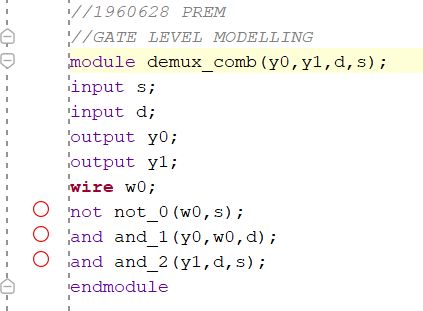


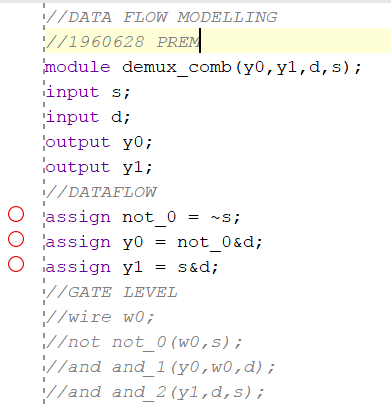
**Truth Table**



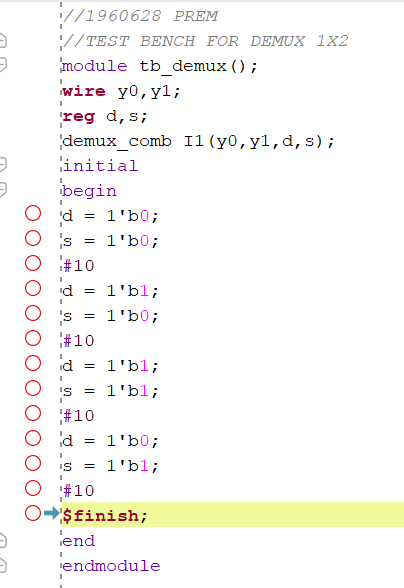
**PROGRAM**

1. **GATE LEVEL MODELING:**

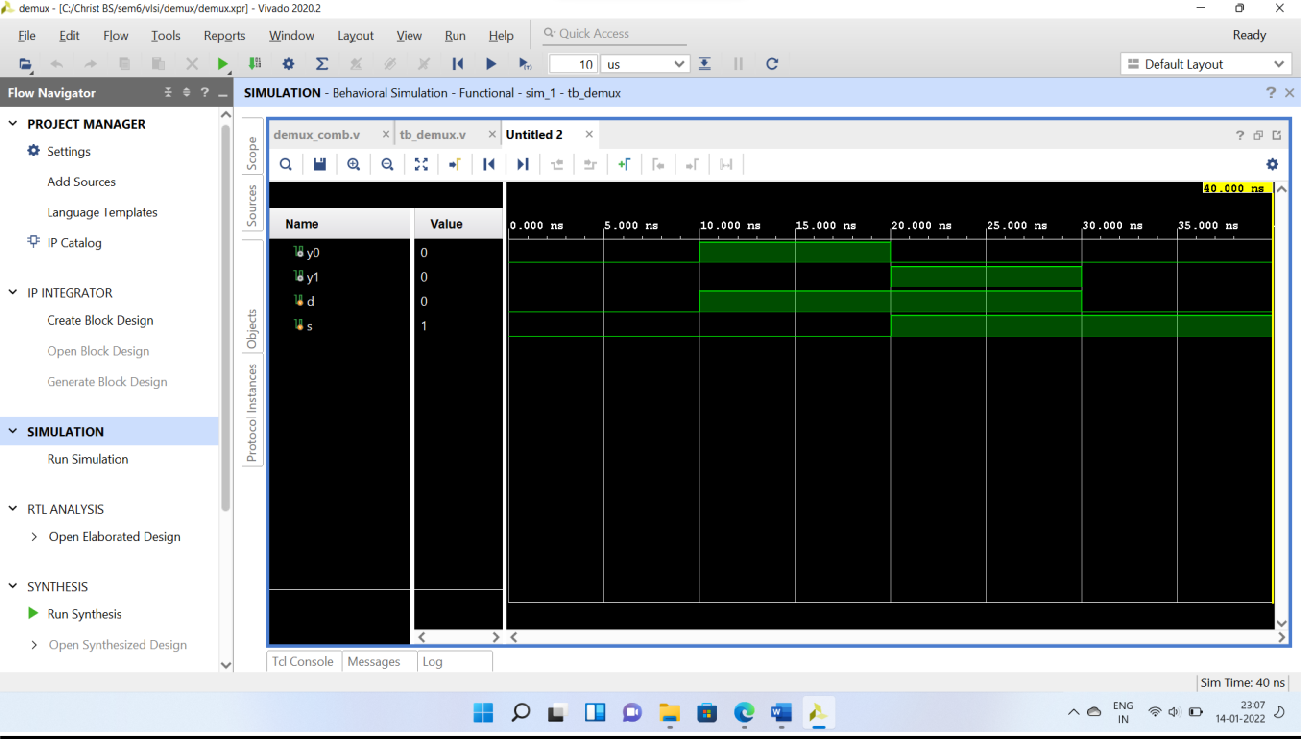


1. **DATAFLOW LEVEL MODELING:**

**TESTBENCH**



**SIMULATION OUTPUT**



**RESULT :** A Mux and Demux were modelled in the Xilinx Vivado simulator and their output was verified.