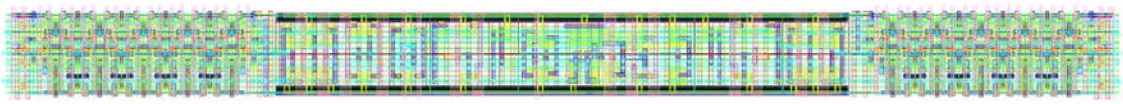
# EEE 525

# Lab 4

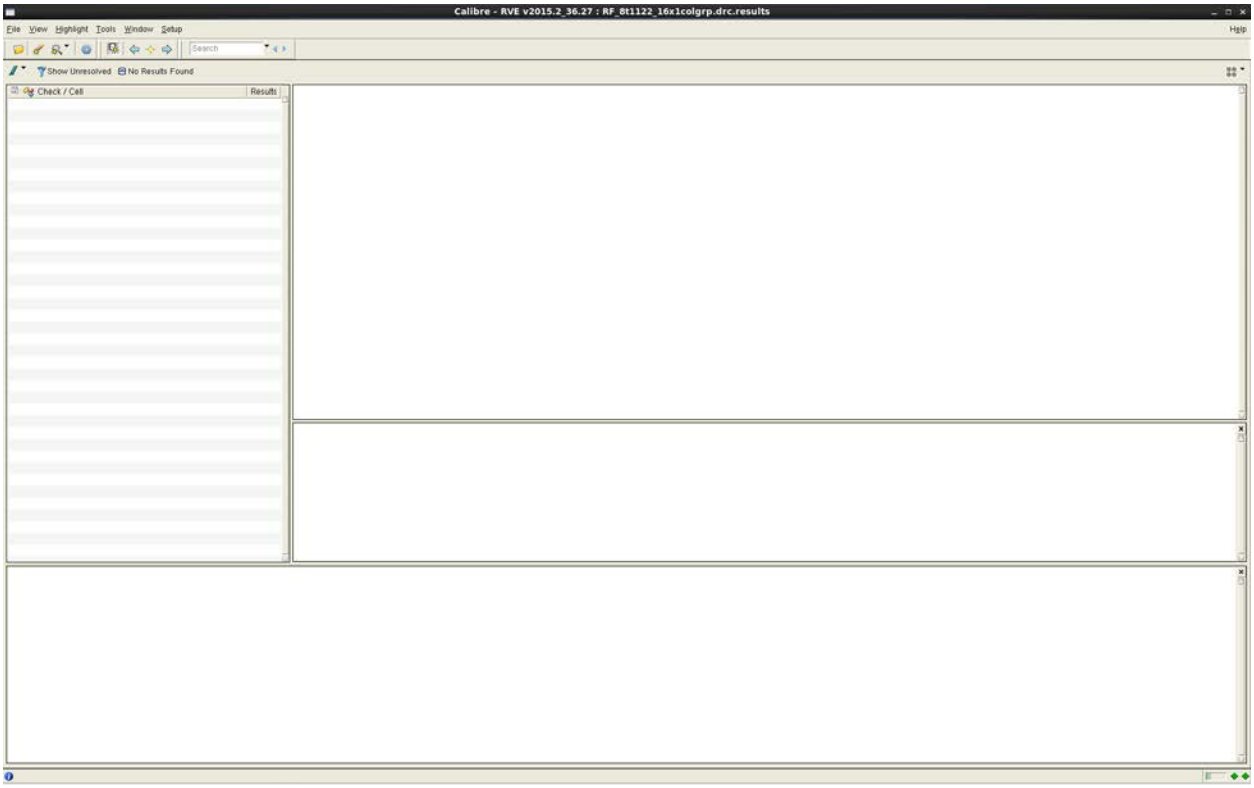
Name: Vishal Srivastava ID No.:1209824652

1. Snapshot of the layout for 16×1 column group.

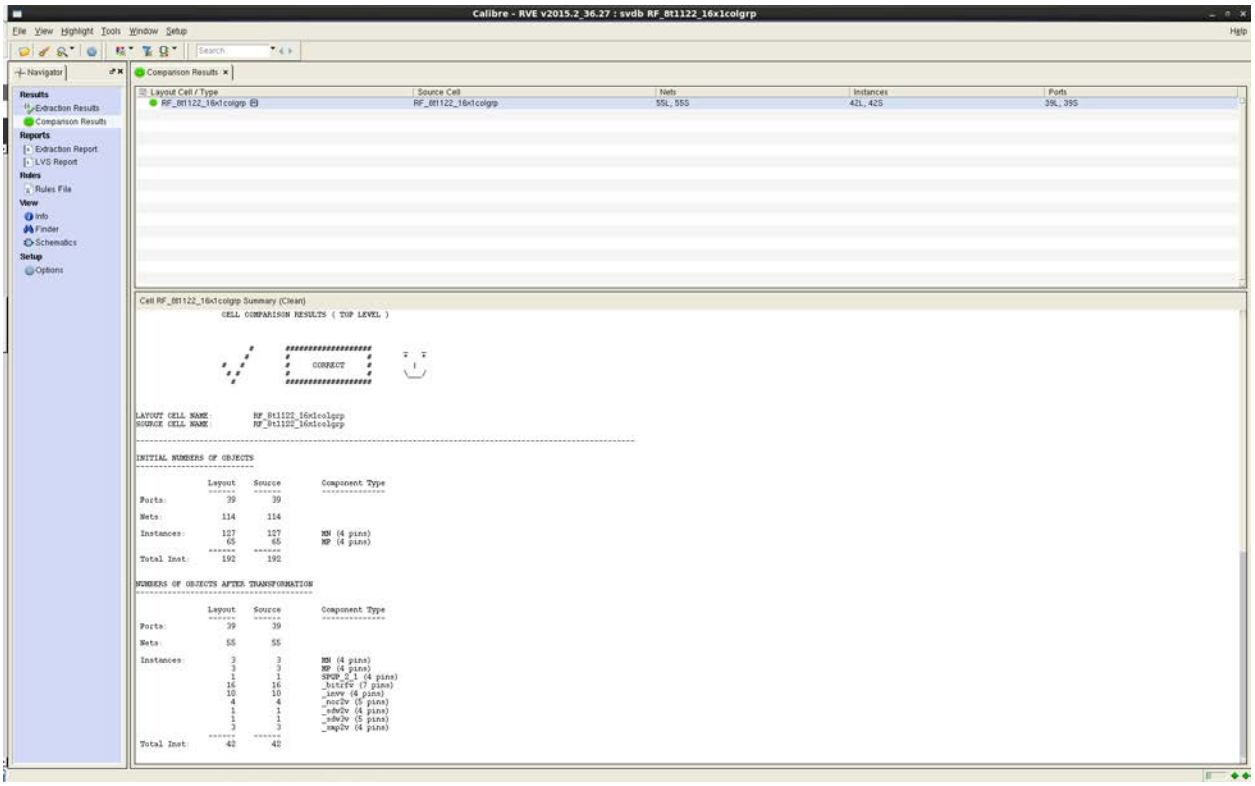


2. DRC and LVS clean snapshots for the 16×1 column group.

DRC


Calibre - RVE v2015.2_36.27 : RF_8t1122_16x1colgrp.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
No Results Found
Check / Cell
Results

LVS




3. Concisely explain the decoder design, justifying your design decisions.

The 4x16 Decoder is based on one 3x18 decoder with de-multiplexed outputs for word0-word7 and word8-word15 with up and down logic. The up and down logic is based on the en and A3 which is the MSB of the input bus.

Up=A3 * en

Down=(~A3) * en

These up and down direct the output of 3x8 decoder to either lower word0-word7 or word8-word15.

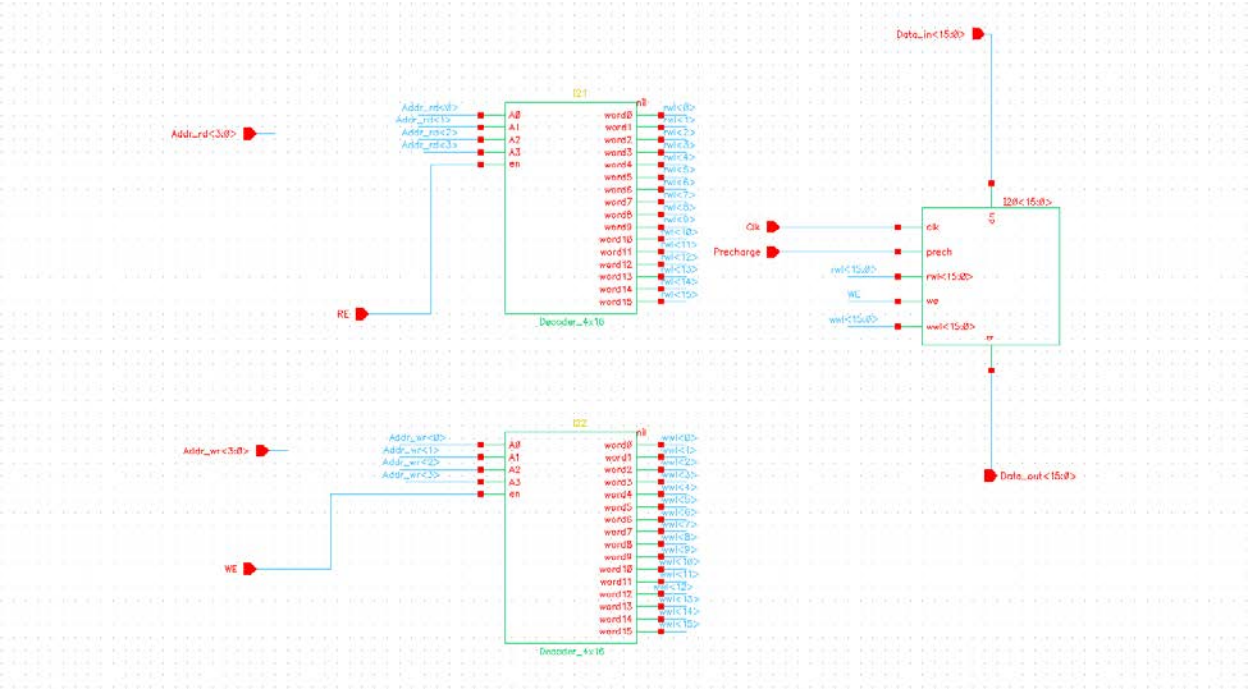
4. Truth table for your decoder.

| En | A3 | A2 | A1 | A0 | Up | Down | $Word_0$ | $Word_1$ | $Word_2$ | $Word_3$ | $Word_4$ | $Word_5$ | $Word_6$ | $Word_7$ | $Word_8$ | $Word_9$ | $Word_{10}$ | $Word_{11}$ | $Word_{12}$ | $Word_{13}$ | $Word_{14}$ | $Word_{15}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | x | x | x | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

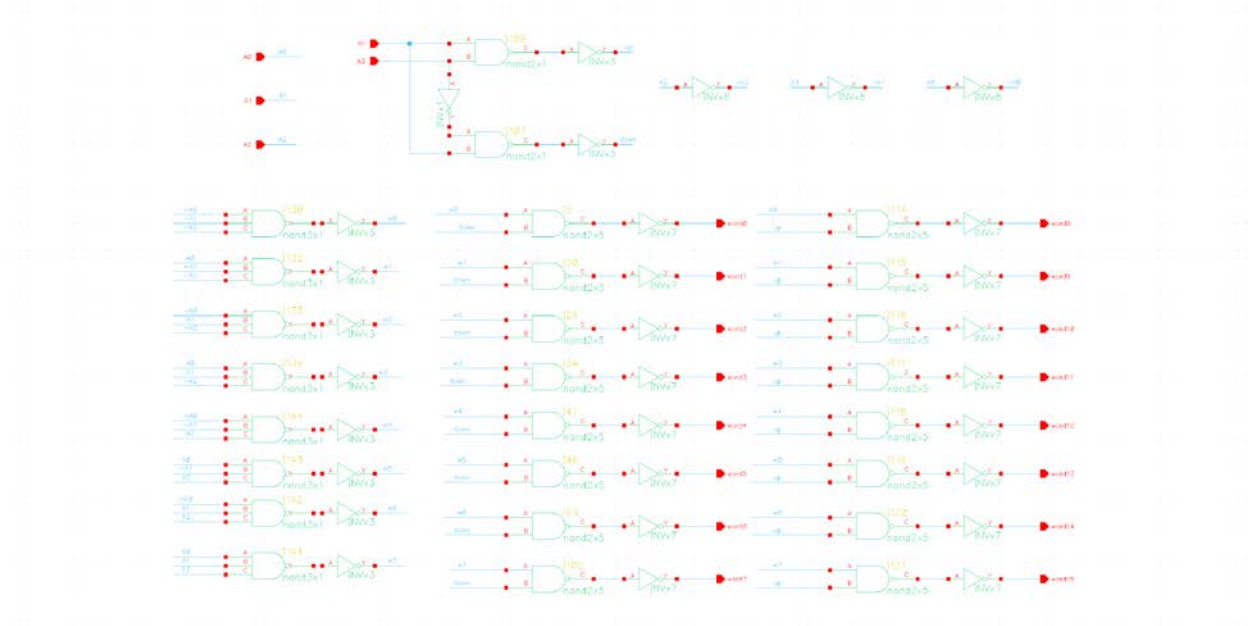
5. Snapshots of the schematic (use white background and visible sizing).

Schematic:

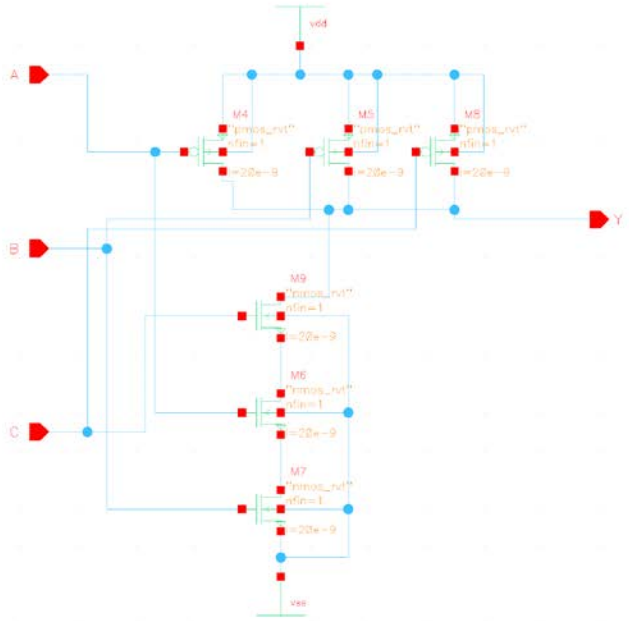
Register File



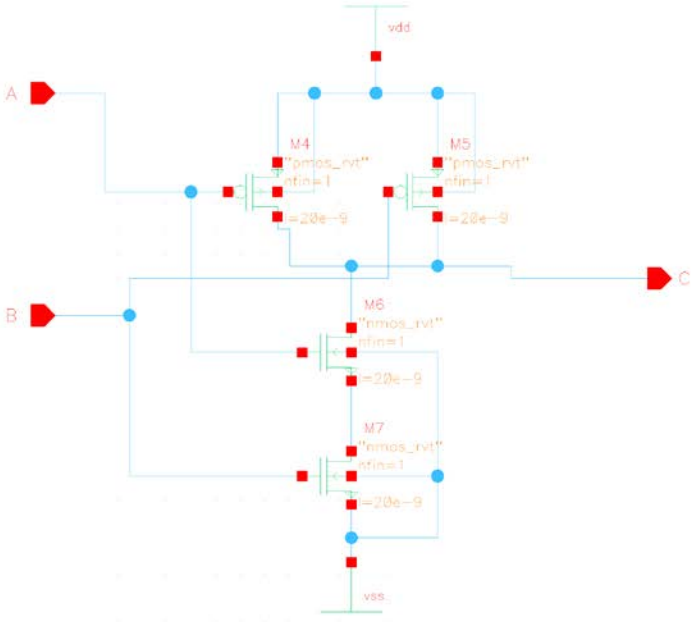

Decoder4x16



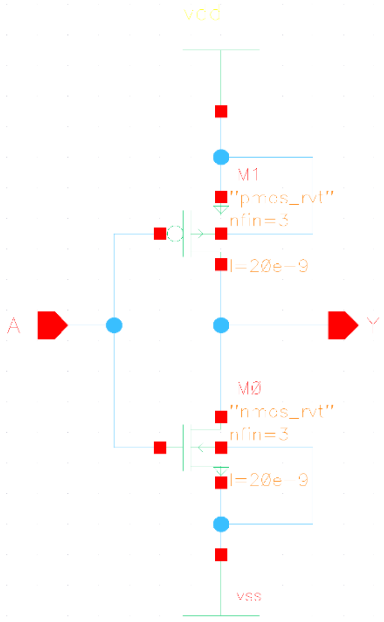
Nand 3x1



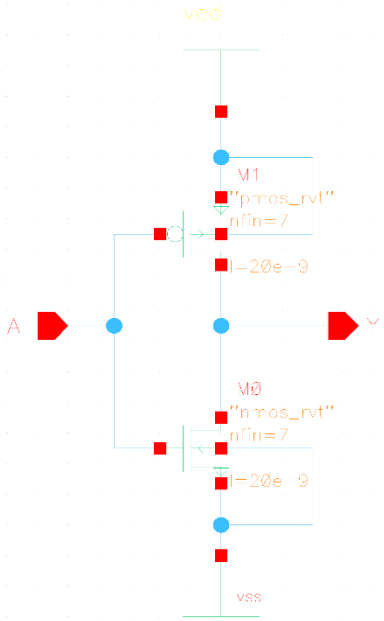

Nand2x1



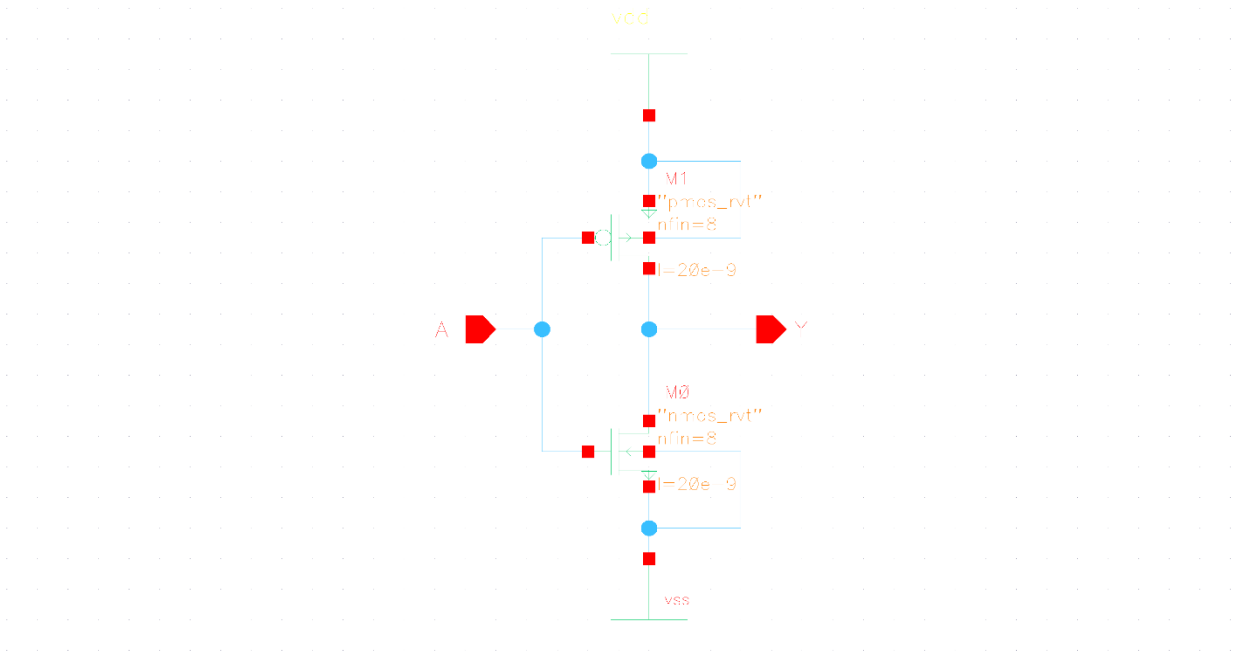

Invx3


vcc
M1
"pmos_rvt"
nfin=3
l=20e-9
A
Y
M0
"nmos_rvt"
nfin=3
l=20e-9
vss

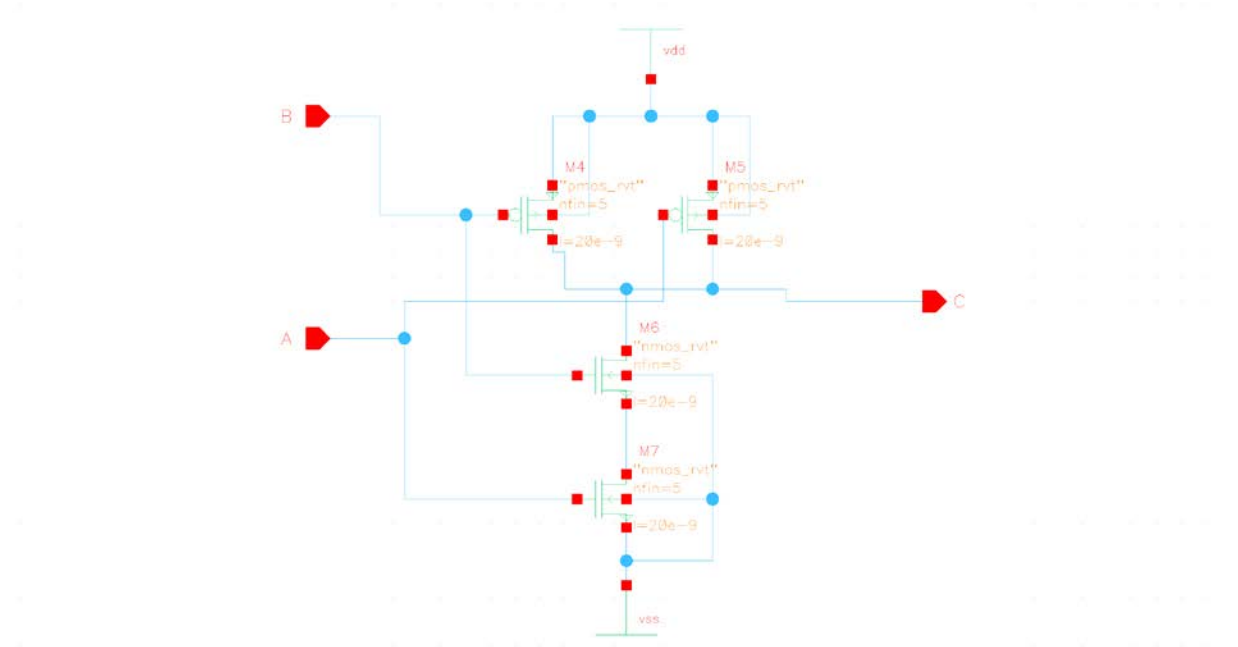
Invx7


vcc
M1
"pmos_rvt"
nfin=7
l=20e-9
A
Y
M0
"nmos_rvt"
nfin=7
l=20e-9
vss

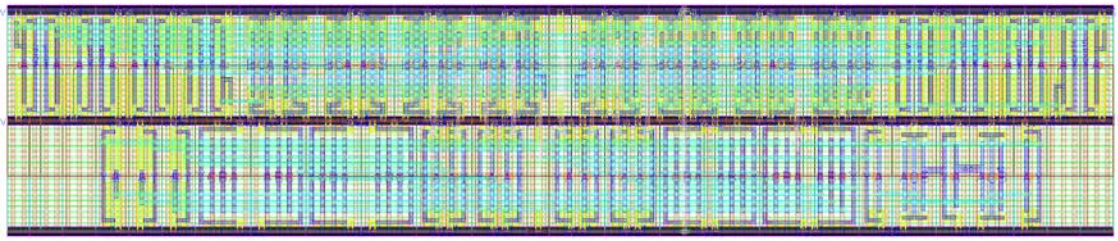
Invx8



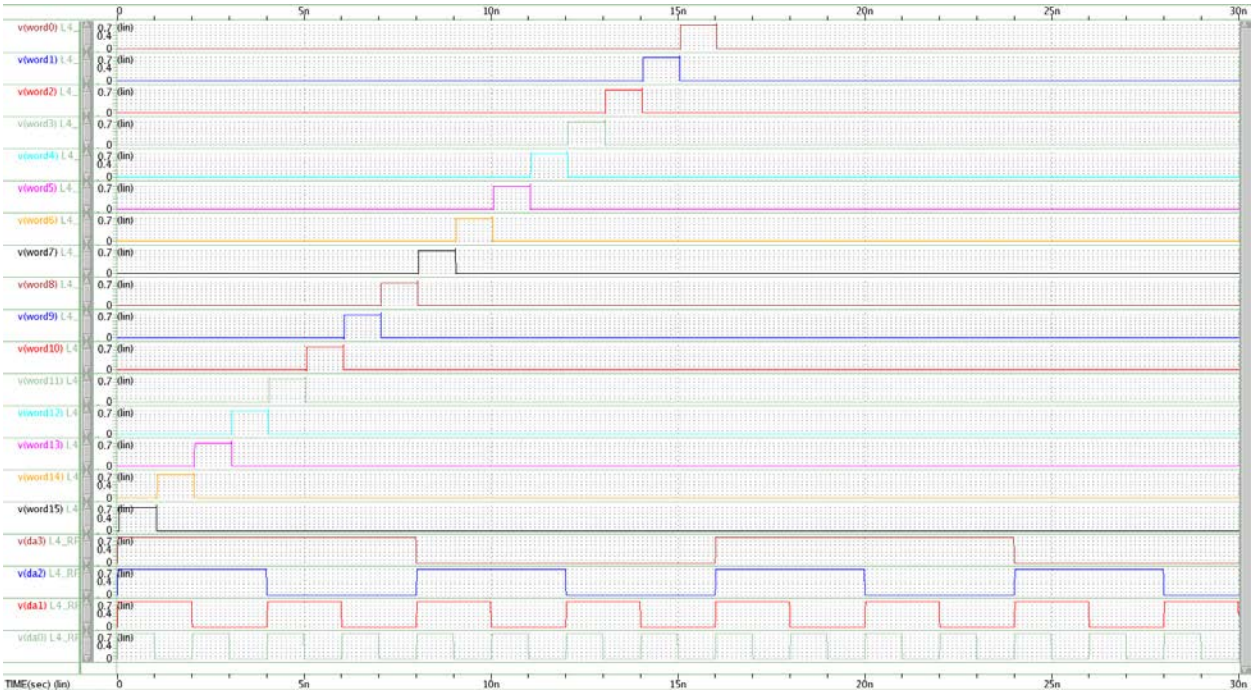

Nand2x5




6. Snapshots of the decoder layout.

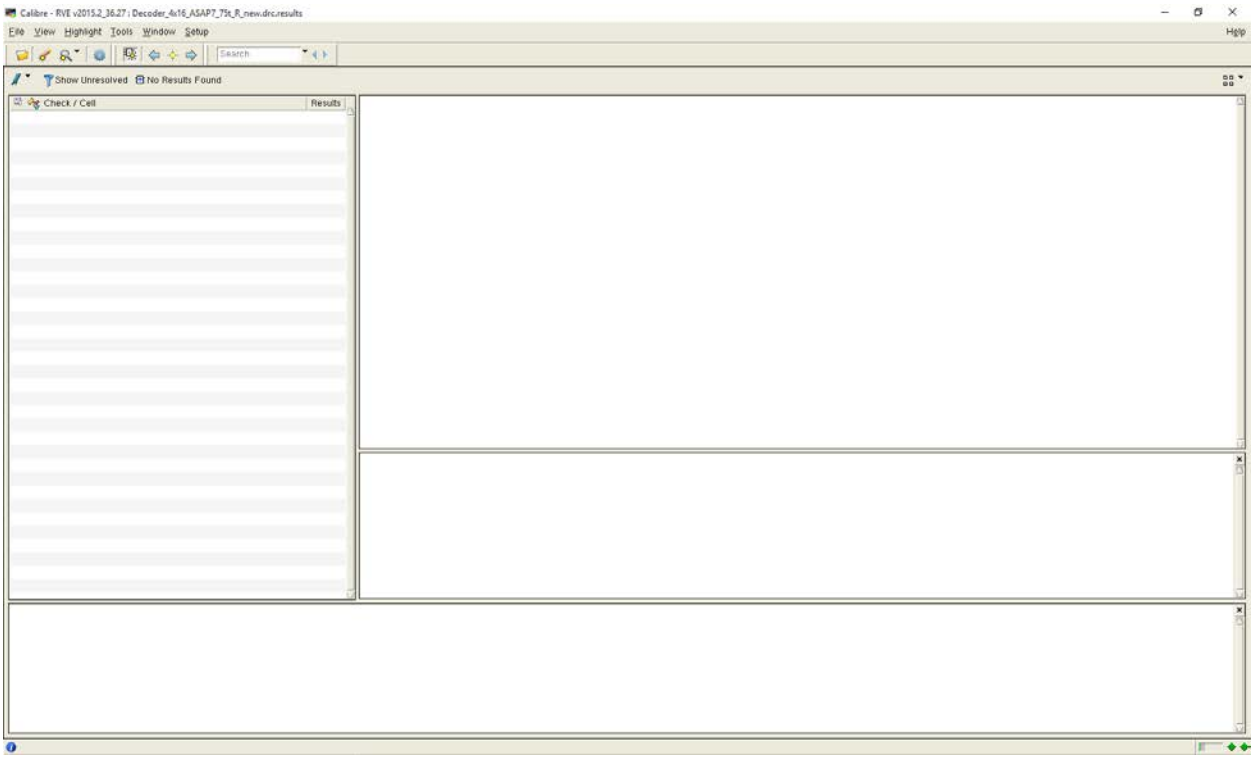


7. Waveforms showing full functionality of your decoder (from post-layout simulations).

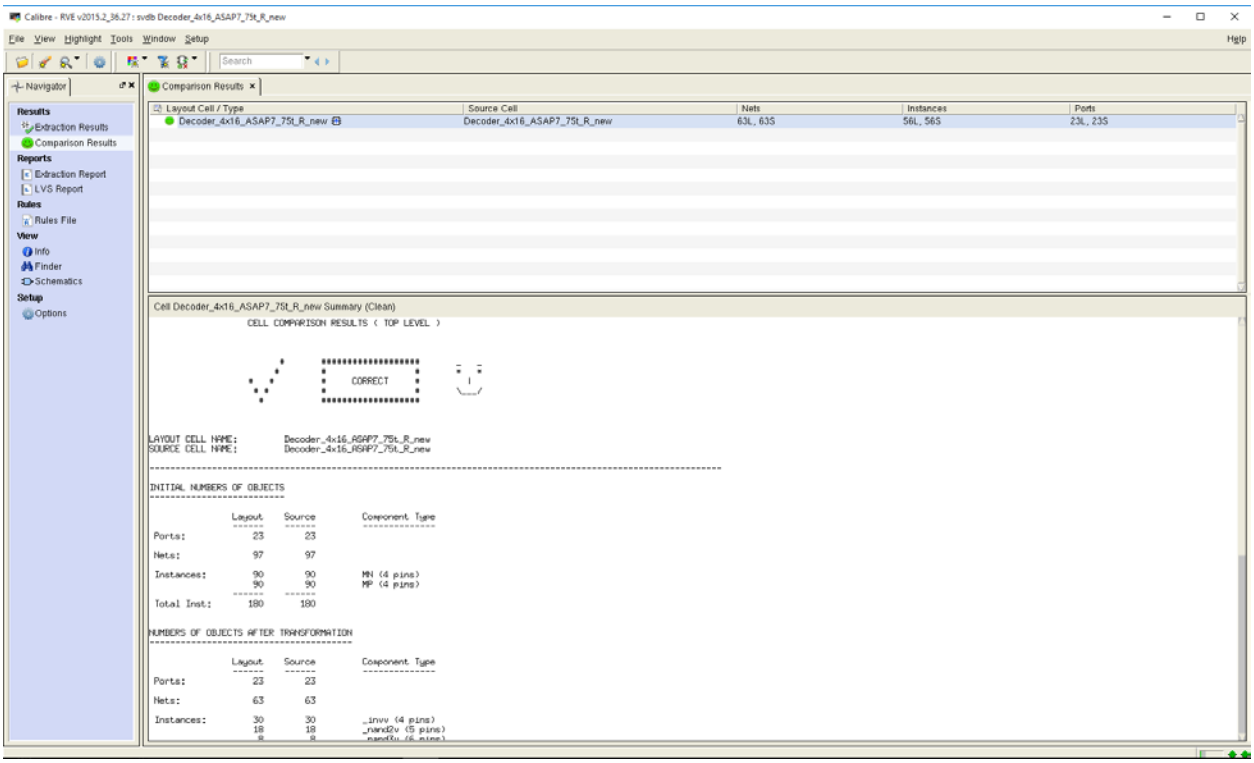


8. DRC and LVS clean snapshots for your decoder.

DRC:

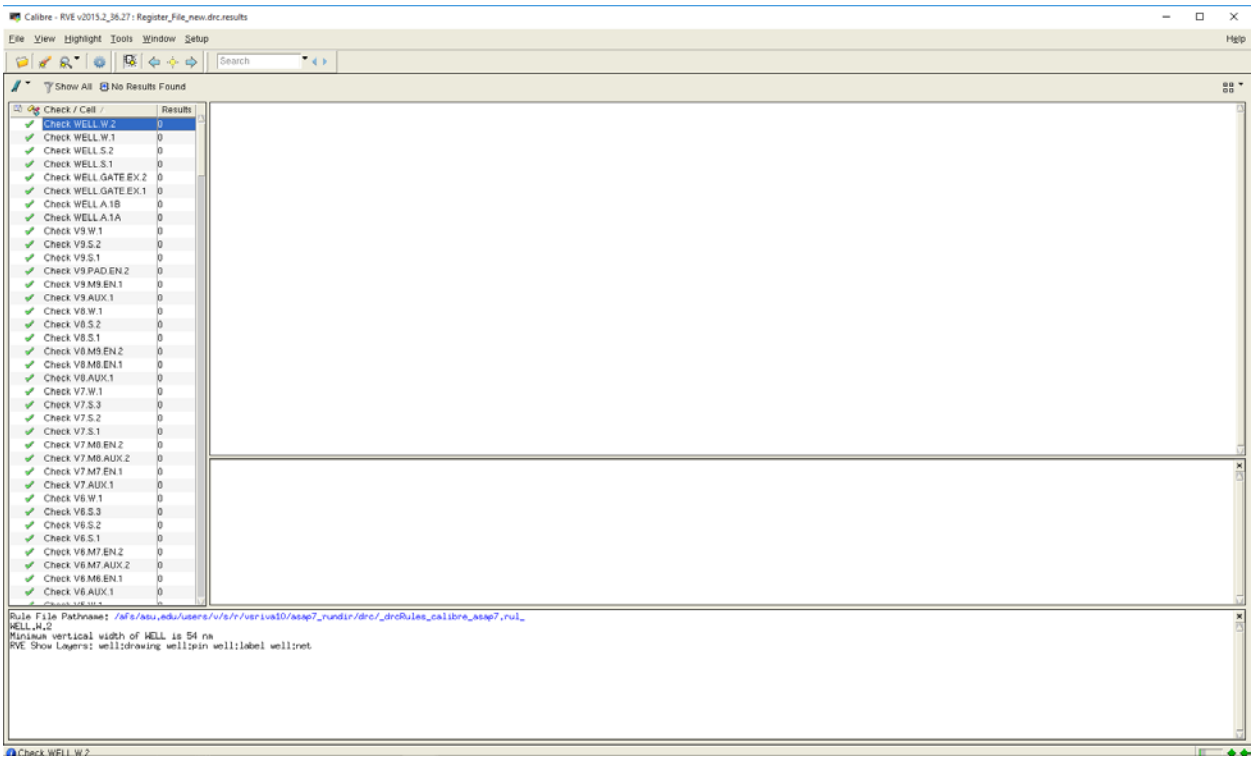



LVS:

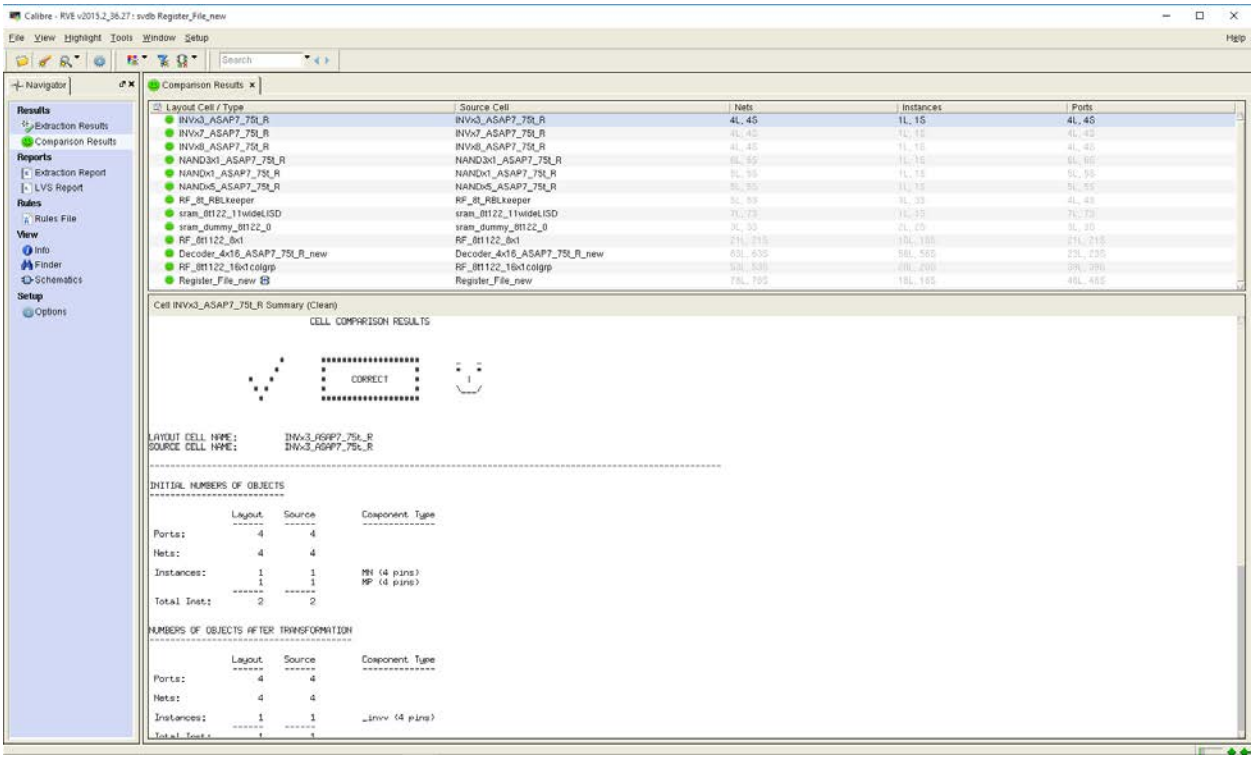



9. DRC and LVS clean snapshots for your final layout (16×16 RF cell with decoder).

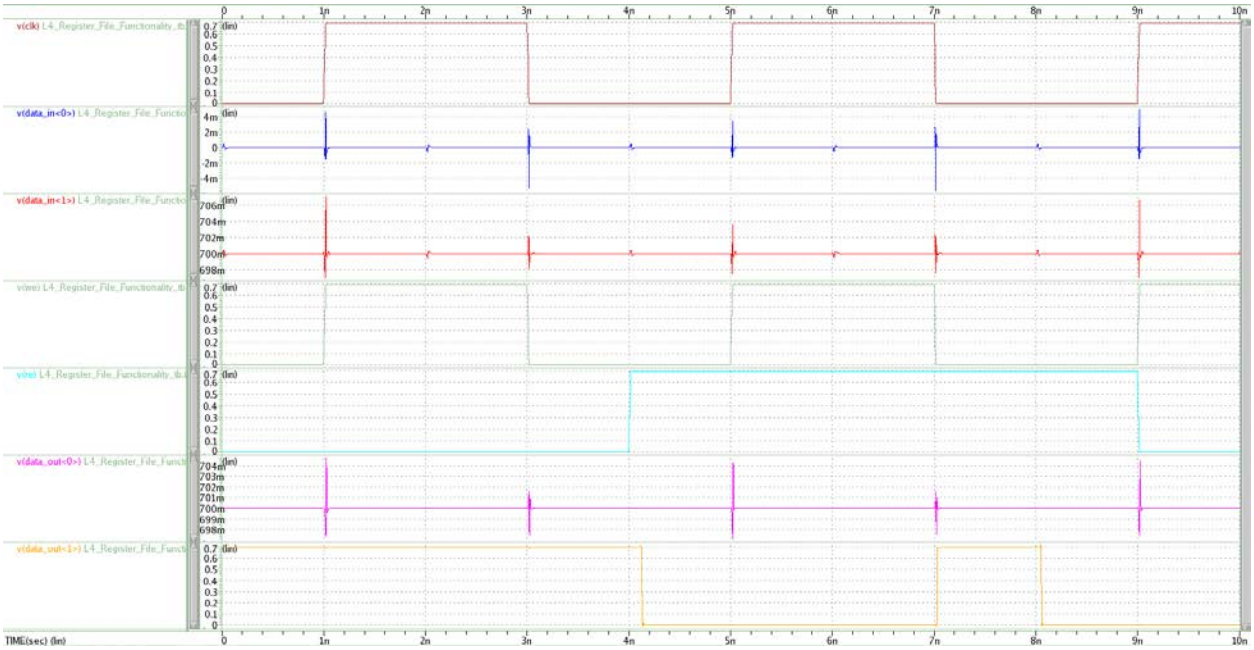
DRC:


Calibre - RVE v2015.2_36.27 : Register_File_new.drc.results
File View Highlight Tools Window Setup
Help
Search
Show All
No Results Found
Check / Cell
Results
Check WELL.W.2 0
Check WELL.W.1 0
Check WELL.S.2 0
Check WELL.S.1 0
Check WELL.GATE.EX.2 0
Check WELL.GATE.EX.1 0
Check WELL.A.1B 0
Check WELL.A.1A 0
Check V9.W.1 0
Check V9.S.2 0
Check V9.S.1 0
Check V9.PAD.EN.2 0
Check V9.M9.EN.1 0
Check V9.AUX.1 0
Check V8.W.1 0
Check V8.S.2 0
Check V8.S.1 0
Check V8.M9.EN.2 0
Check V8.M8.EN.1 0
Check V8.AUX.1 0
Check V7.W.1 0
Check V7.S.3 0
Check V7.S.2 0
Check V7.S.1 0
Check V7.M8.EN.2 0
Check V7.M8.AUX.2 0
Check V7.M7.EN.1 0
Check V7.AUX.1 0
Check V6.W.1 0
Check V6.S.3 0
Check V6.S.2 0
Check V6.S.1 0
Check V6.M7.EN.2 0
Check V6.M7.AUX.2 0
Check V6.M6.EN.1 0
Check V6.AUX.1 0
Rule File Pathname: /afs/asu.edu/users/v/s/r/vsriva10/asap7_rundir/drc/_drcRules_calibre_asap7.rul_
WELL.W.2
Minimum vertical width of WELL is 54 nm
RVE Show Layers: well:drawing well:pin well:label well:net
Check WELL.W.2

LVS:


Calibre - RVE v2015.2_36.27 : svdb Register_File_new
File View Highlight Tools Window Setup
Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
INVx3_ASAP7_75t_R
INVx7_ASAP7_75t_R
INVx8_ASAP7_75t_R
NAND3x1_ASAP7_75t_R
NANDx1_ASAP7_75t_R
NANDx5_ASAP7_75t_R
RF_8t_RBLkeeper
sram_8t122_11wideLISD
sram_dummy_8t122_0
RF_8t1122_8x1
Decoder_4x16_ASAP7_75t_R_new
RF_8t1122_16x1colgrp
Register_File_new
4L, 4S
1L, 1S
Cell INVx3_ASAP7_75t_R Summary (Clean)
CELL COMPARISON RESULTS
CORRECT
LAYOUT CELL NAME: INVx3_ASAP7_75t_R
SOURCE CELL NAME: INVx3_ASAP7_75t_R
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 4 4
Nets: 4 4
Instances: 1 1 MN (4 pins)
1 1 MP (4 pins)
Total Inst: 2 2
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 4 4
Nets: 4 4
Instances: 1 1 _invv (4 pins)

10. Waveforms proving the functionality (simultaneous read and write in single cycle). It is your responsibility to prove the functionality, so ensure that you capture all the required conditions to prove that your design is working.



11. Describe and report the fastest corner cases (one or multiple) and the slowest corner cases (one or multiple) that should be considered for the RF array design.

As the reads will be the slower ones so,

Timing Table

| Worst Case | | Best Case | |
|---|---|---|---|
| $T_{re->dataout15}$ at rwl<7> | 117.301ps | $T_{re->dataout0}$ at rwl<0> | 115.0449ps |
| $T_{re->dataout15}$ at rwl<15> | 117.4558ps | $T_{re->dataout0}$ at rwl<8> | 115.9834ps |
| $T_{re->dataout7}$ at rwl<7> | 117.0567ps | $T_{re->dataout8}$ at rwl<0> | 115.0260ps |
| $T_{re->dataout7}$ at rwl<15> | 117.1193ps | $T_{re->dataout7}$ at rwl<8> | 115.9678ps |

So, the worst case: 117.4558ps at $T_{re->dataout15}$ at rwl<7> and the Best case: 115.0260ps at $T_{re->dataout8}$ at rwl<0>

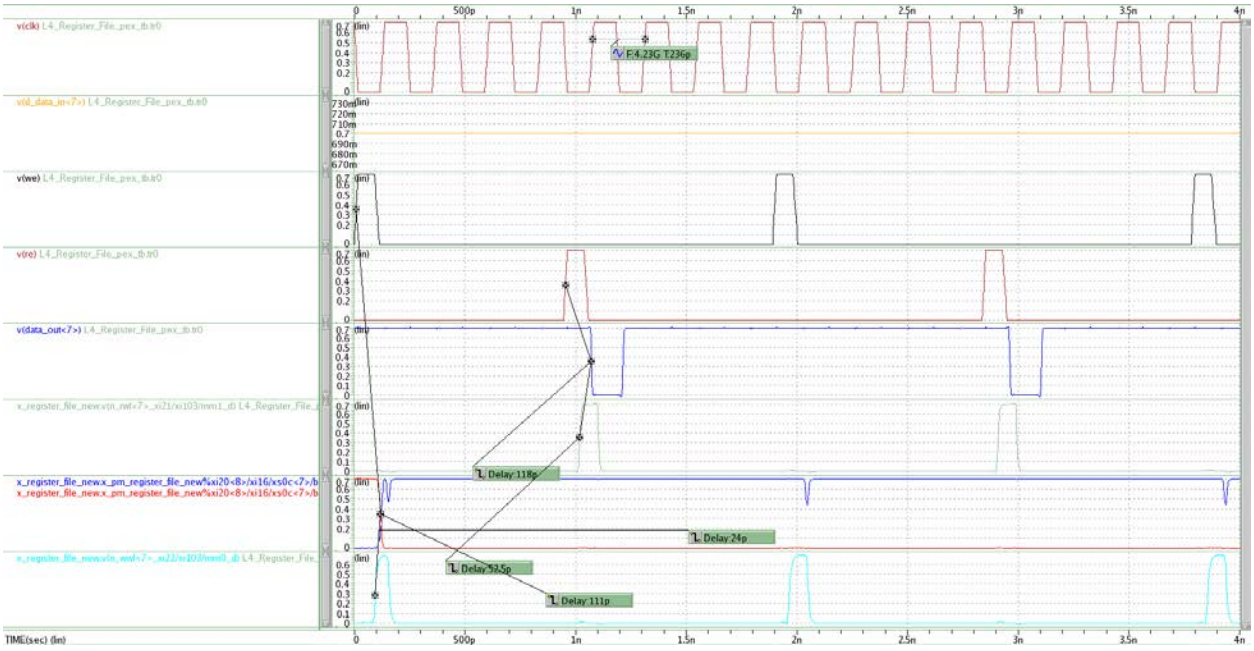
The worst cases are due to cells placed at extreme corners of the Register File whereas the best cases are due to cells placed at interior where the decoder is placed. The delay is due to RC delay introduced due to interconnect wire. So, the delay in direct proportional to the distance from the decoder.

12. Waveforms showing RE to output and WE to bit cell change delays for all corner cases.

13. Waveforms showing RWL (read word line) to output and WWL (write word line) to bit cell change delay for all corner cases.

Common Answer for Q12-Q13

Worst Case: $T_{re->dataout15}$ at rwl<7>




14. Report the area and maximum operating frequency for your design, based on post-layout extracted simulation.

Area: 5.5065 x 8.491 = 46.75nm$^2$

Max Operating Frequency: 4.23GHz

15. Directory path to your final design library (do not modify the files here after the deadline, the timestamps could be checked during the demo).

Path: afs/asu.edu/users/v/s/r/vsriva10/asap7_rundir/RF_Lab4/Register_File_new