APR Report

1. CTSRPT

##
Complete Clock Tree Timing Report
#
CLOCK: clk
#
Mode: postRoute
#
Delay Corner information
Analysis View   : default_setup_view
Delay Corner Name : delayCorner_slow
RC Corner Name   : RC_corner_25
Analysis View   : default_hold_view
Delay Corner Name : delayCorner_fast
RC Corner Name   : RC_corner_25
##

Nr. of Subtrees   : 1
Nr. of Sinks   : 3041
Nr. of Buffer   : 93
Nr. of Level (including gates) : 6
Root Rise Input Tran   : 0.1(ps)
Root Fall Input Tran   : 0.1(ps)
No Driving Cell Specified!
Max trig. edge delay at sink(R): k0_reg[13][1]/CLK 151.2(ps)
Min trig. edge delay at sink(R): k2_reg[6][7]/CLK 110.1(ps)

                         (Actual)   (Required)
Rise Phase Delay   : 110.1~151.2(ps)   0~10(ps)
Fall Phase Delay   : 121.7~165.9(ps)   0~10(ps)
Trig. Edge Skew   : 41.1(ps)   16(ps)
Rise Skew   : 41.1(ps)
Fall Skew   : 44.2(ps)
Max. Rise Buffer Tran   : 55.4(ps)   200(ps)
Max. Fall Buffer Tran   : 44(ps)   200(ps)
Max. Rise Sink Tran   : 67.9(ps)   200(ps)
Max. Fall Sink Tran   : 54.3(ps)   200(ps)
Min. Rise Buffer Tran   : 9.7(ps)   0(ps)

Min. Fall Buffer Tran   : 9.7(ps)   0(ps)
Min. Rise Sink Tran   : 4.9(ps)   0(ps)
Min. Fall Sink Tran   : 4.1(ps)   0(ps)

view default_setup_view : skew = 41.1ps (required = 16ps)
view default_hold_view : skew = 41.1ps (required = 16ps)

***** NO Max Transition Time Violation *****

***** NO Min Transition Time Violation *****

***** NO Max_Fanout Violation *****

***** NO AC Irms Limit Violation *****

**** Sub Tree Report ****
OUTPUT_TERM: clk [0(ps) 0(ps)]

Main Tree:
    nrSink   : 3041
    Rise Delay   : [110.1(ps) 151.2(ps)]
    Rise Skew   : 41.1(ps)
    Fall Delay   : [121.7(ps) 165.9(ps)]
    Fall Skew   : 44.2(ps)

  Main Tree from clk w/o tracing through gates:
    nrSink : 3041
    nrGate : 0
    Rise Delay [110.1(ps) 151.2(ps)] Skew [41.1(ps)]
    Fall Delay [121.7(ps) 165.9(ps)] Skew=[44.2(ps)]

2. Geom.rpt
##
Generated by: Cadence Encounter 14.27-s035_1
OS: Linux x86_64(Host ID eecad32.eas.asu.edu)
Generated on: Wed Nov 30 20:45:10 2016
Design: simon32_64
Command: verifyGeometry
##

Begin Summary ...
  Cells   : 0
  SameNet   : 0

```
 Wiring     : 0
 Antenna    : 0
 Short      : 0
 Overlap    : 0
End Summary
```

No DRC violations were found

3. Conn.rpt

```
####################################################################
#  Generated by:     Cadence Encounter 14.27-s035_1
#  OS:               Linux x86_64(Host ID eecad32.eas.asu.edu)
#  Generated on:     Wed Nov 30 21:46:35 2016
#  Design:           simon32_64
#  Command:          verifyConnectivity -type all -error 1000 -warning 50
####################################################################
Verify Connectivity Report is created on Wed Nov 30 21:46:35 2016
```

```
Begin Summary
    Found no problems or warnings.
End Summary
```

4. Gate and Area

simon32_64 Gates=142221 Cells=35834 Area=99532.2 um^2