Lab5

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Architecture and high level-block Diagram

The architecture consists of two big block, key generation and cipher generation block
The key generation block consists of the whole 32 pipelined staged block which outputs key at each block from k_out(ko) to k_31 which are mapped to each corresponding stage of cipher generation block from stages x0 to x31 respectively.
Note: All Key blocks are 3 stage flopped so as to retain the old Key values to generate respective next keys.

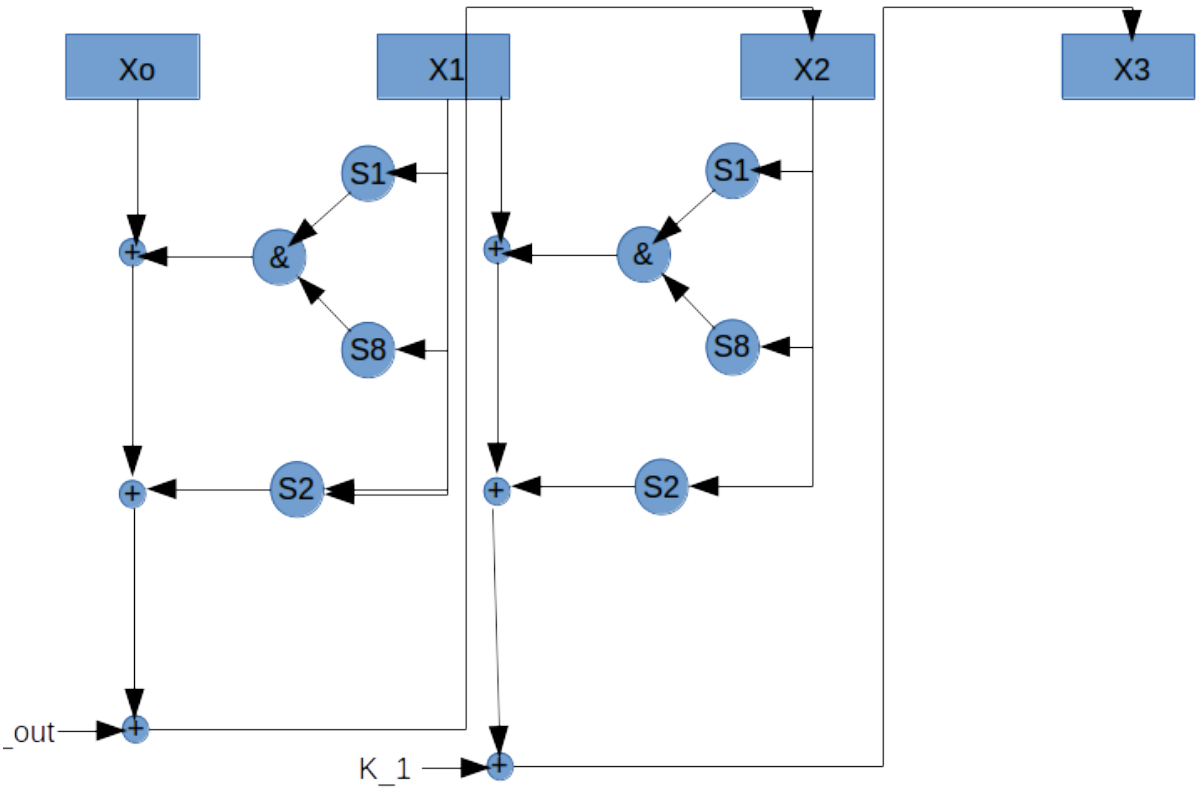


Illustration 1: Cipher Generation Block (Generation of few values presented as its the same for rest)

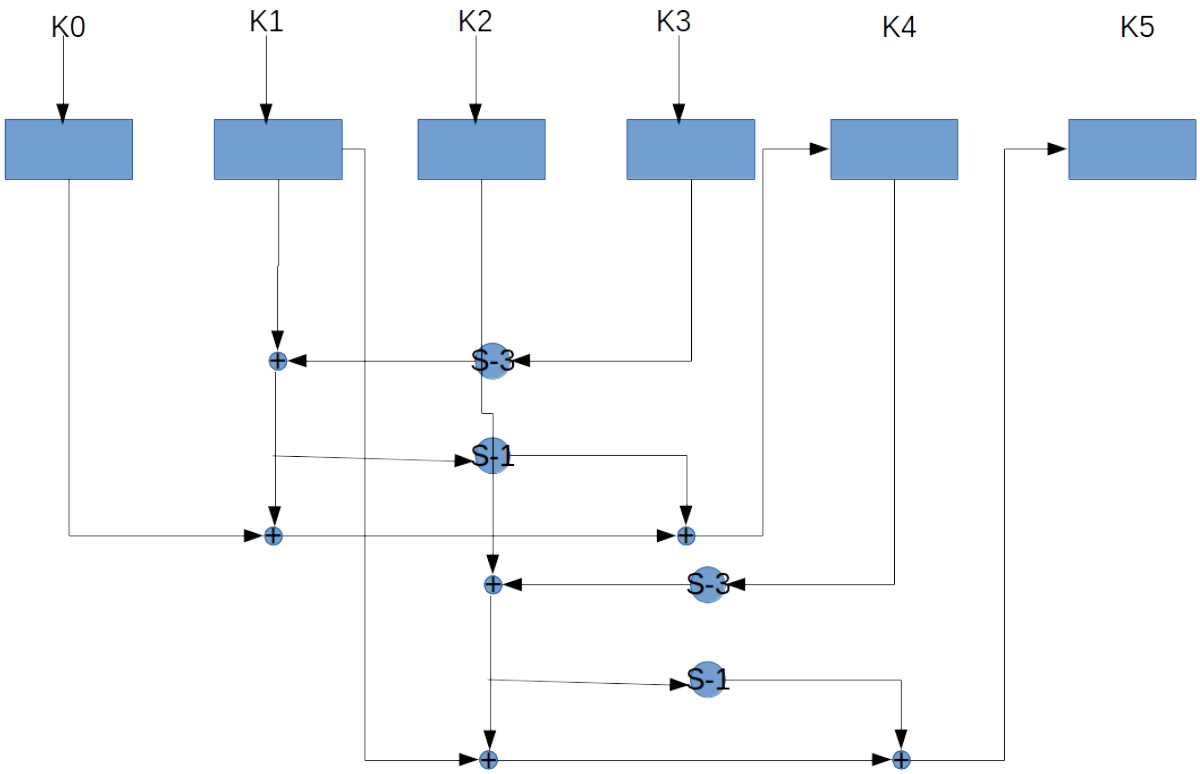


Illustration 2: Key_generation_block.(Generation few values shown as its same for all 32 stages)

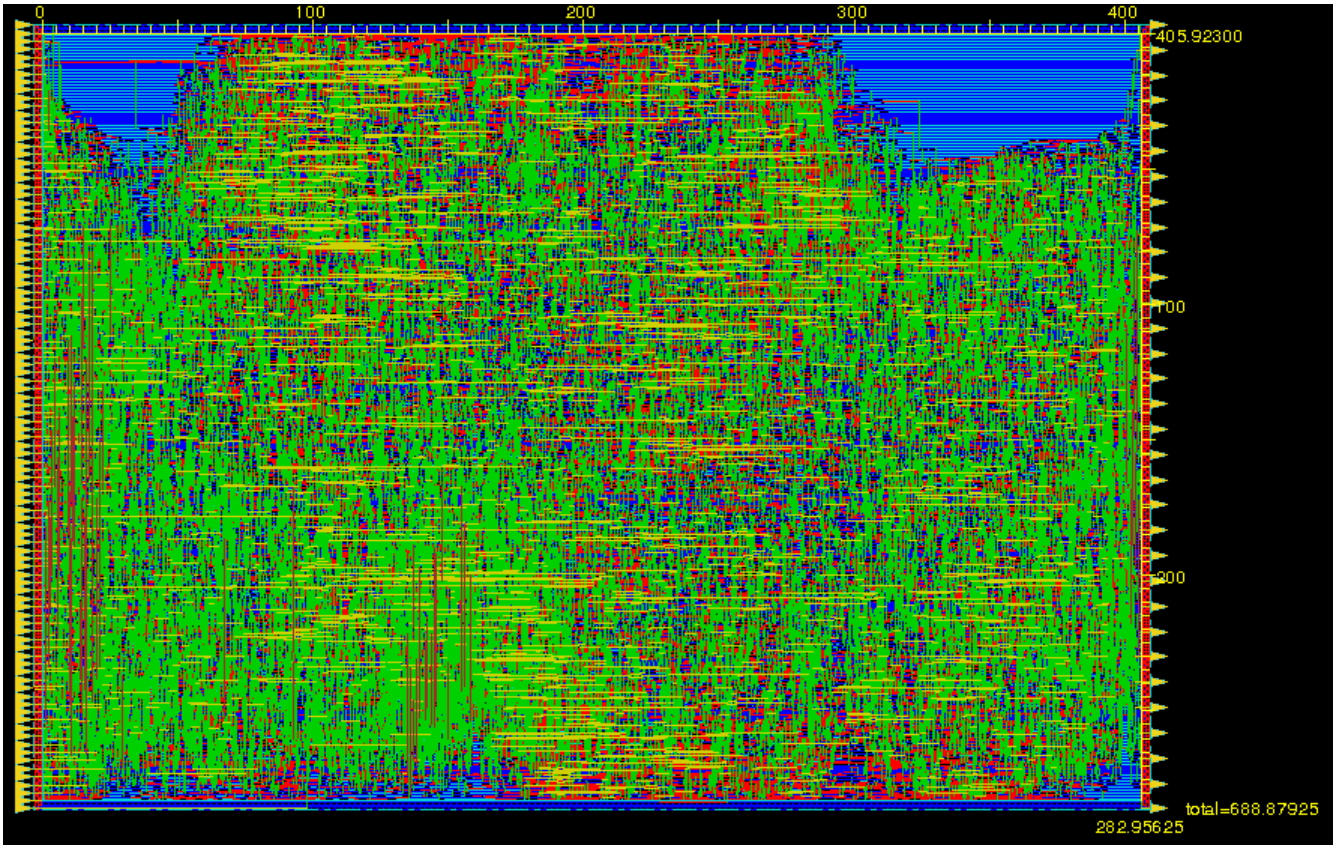
• Design Decision
Design was made pipelined in order to meet the requirement of every clk stage input and output. So after 32 cycles the clock starts to output the value consecutively.

• Total latency (= total testbench simulation time from ModelSim) =477139 ps= 0.000477139 ms

• Power (from PrimeTime) :10.1 mW

• Number of total standard cell gates =10404 cells

• Area (exclude power/ground rings, only the entire standard cells + filler cells area – show x and y dimension from screenshot) =405.923 * 282.956 = 114858.348 um^2 = 0.114858 mm^2



• Encounter density (before filler cell insertion) =0.8745