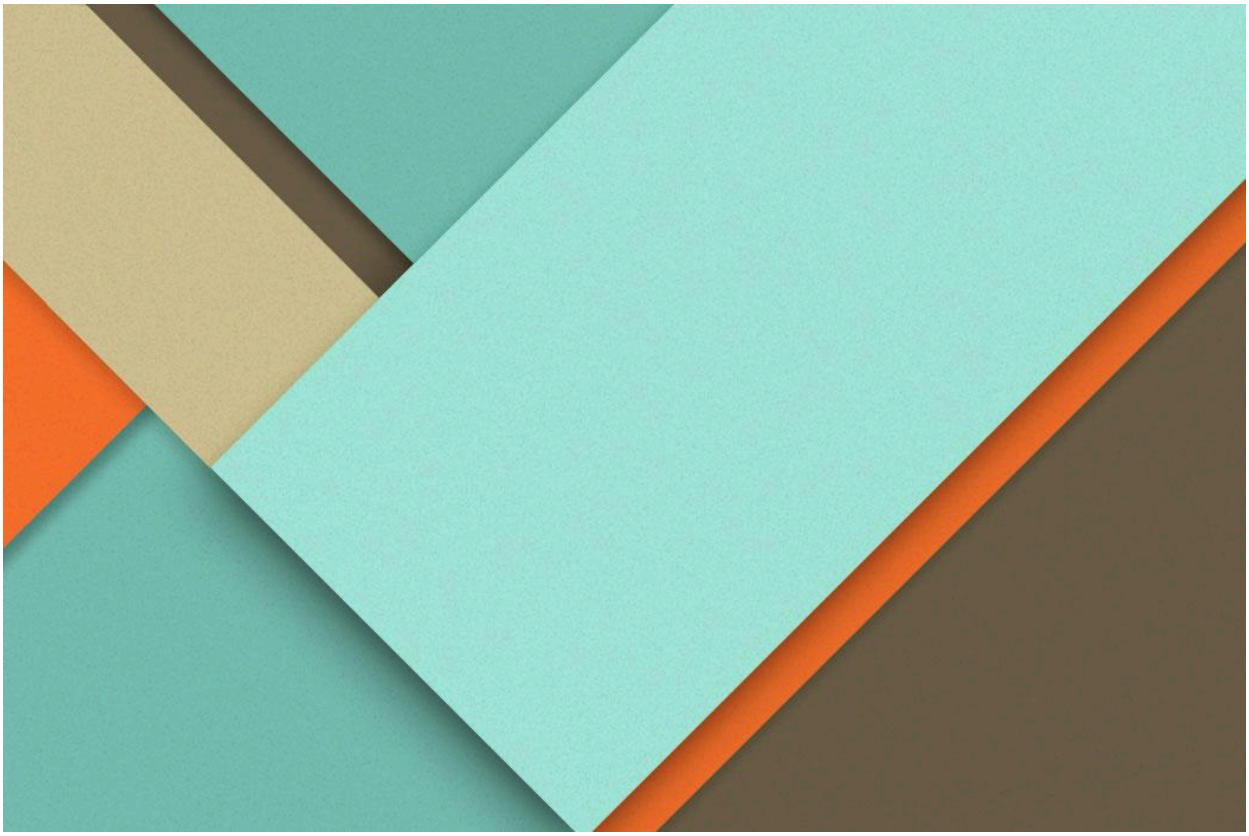

Discrete Audio Amplifier with Smart Power Protection

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1. Problem Statement

In many low-voltage electronics projects—especially those involving microcontrollers or analog audio circuits—power supply safety is often overlooked. A slight wiring mistake, such as connecting the supply in reverse or applying a voltage spike, can damage sensitive components. Similarly, short circuits and current surges pose a constant risk in experimental setups.

Another challenge lies in building audio amplifier circuits from scratch without using prebuilt ICs. While integrated amplifiers are convenient, they hide the working principles from learners. To fully understand signal amplification, it's valuable to construct a multi-stage amplifier using only discrete components like BJTs. However, achieving high gain and low distortion with BJTs alone requires careful design, especially in biasing and coupling.

This project addresses both of these challenges: creating a power input protection system and developing a discrete three-stage Class A audio amplifier. Together, they form a complete analog front-end that is both educational and practically useful.

2. Objectives

The primary goals of this project are twofold:

1. **Develop a robust power protection circuit** capable of:
    - Operating across a voltage range of **9 V to 18 V**
    - Blocking **reverse polarity (reverse current protection)**
    - Responding to **overvoltage conditions** (above 18 V) (changable according to value of used zenor diode) (similar to **Crowbar Circuit)**
    - Limiting **overcurrent** and responding to **short circuits**

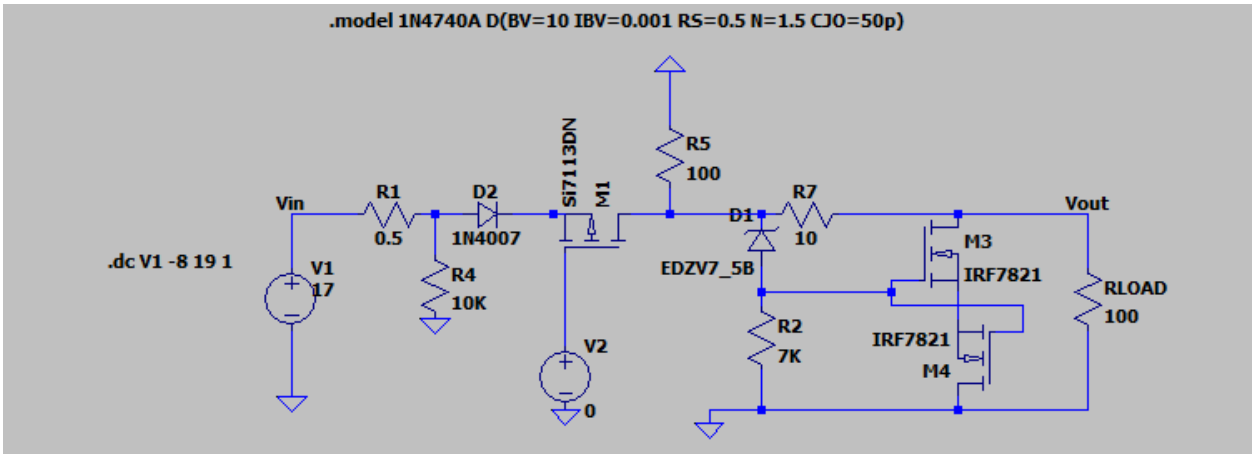
2. **Design and simulate a three-stage audio amplifier** using **only BJT transistors**, with the following goals:
    - Achieve high voltage gain from a low-amplitude input
    - Maintain clean, undistorted output
    - Bias each stage correctly for Class A operation
    - Simulated in LTSPICE with

3. Circuit Description

A. Protection Circuit

The power protection circuit serves as the first line of defence for any downstream electronics connected to it. Its key features and components include:

- A P-Channel MOSFET is placed in reverse-polarity protection mode. When the supply is connected correctly, the MOSFET conducts normally. If the supply is reversed, the MOSFET blocks the path, preventing current from reaching the board.



CIRCUIT: Protection Circuit

CIRCUIT EXPLANATION :

Component used: 1. MF-R200 (2A Resettable fuse)

2. Resistor (10k,100, 1o,7k,100 ohm)
3. Pmos (SI7113DN)
4. NMOS (IRF7821)
5. ZENER DIODE (EDZV7_58,V_bk=16v)
6. DIODE (IN4007)

CIRCUIT DISCUSSION

This circuit is divided into two parts:

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1. Diode-PMOS for Reverse Current Protection

For PMOS, **V_{gate} = 0V**. The source of the PMOS is connected to the cathode of the diode. This setup helps cancel the effect of the PMOS acting like a diode when the supply is connected in reverse.

When **V_{GS} > 0**, the PMOS should be **OFF**, but due to the diode behavior, current can still flow from drain to source. To eliminate this unwanted diode effect, I used a **series diode (D2)**. This diode will be in reverse bias during **V_{GS} > 0**, so it blocks the current.

In LTSpice, I used a **resistor as a fuse** and a **10kΩ pull-down resistor** at the anode of the diode to maintain circuit integrity.

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2. Crowbar Circuit (Overvoltage Protection)

The second part of the circuit is the **overvoltage protection** section. Generally, crowbar circuits use a **thyristor**, but here we use **NMOS transistors** in series to avoid the diode effect when the MOSFET is OFF.

Why can't we use a diode here?

If we use a diode in place of the MOSFET, it would go against the main purpose of the circuit. The goal is:

- When the **overvoltage threshold** is crossed, the gate of the NMOS gets activated.
- This turns ON the NMOS, which **shorts the load**, connecting the supply directly to ground.
- As a result, **high current** flows and the **fuse burns**, protecting other components in the circuit.

This design assumes:

- The **current spike** is brief (lasting microseconds to milliseconds).
- The spike flows through the **low-impedance crowbar**, not through sensitive components.
- The **PTC (fuse)** opens fast enough to break the circuit.

How the Crowbar Circuit Works

Because of the fuse resistor, there will be a small voltage drop at the **drain of the PMOS**. For example, I used a **16V breakdown zener diode**.

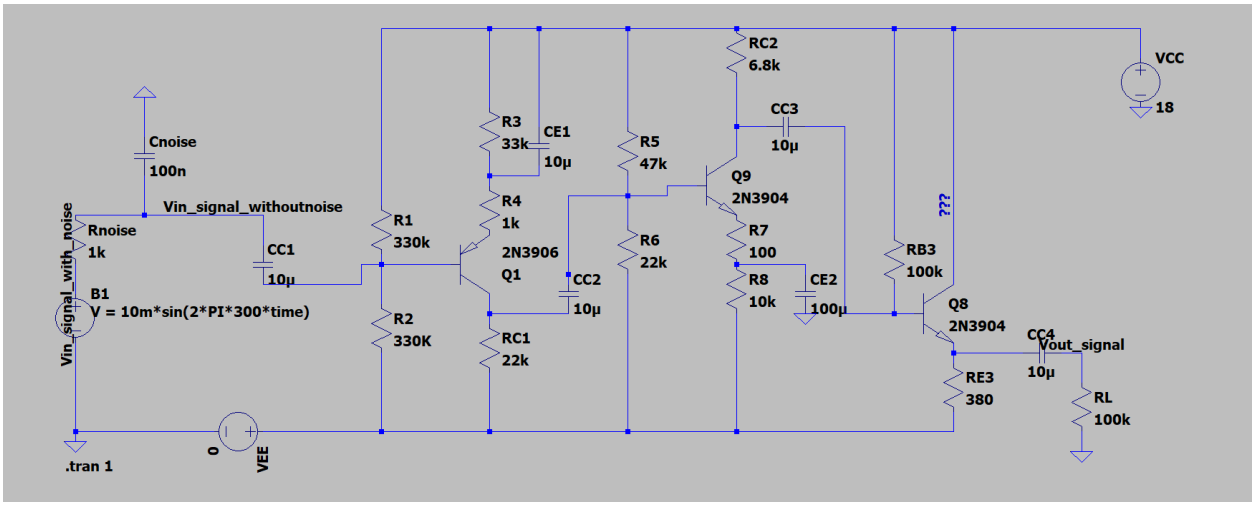
- When the drain voltage of the PMOS **exceeds 16V**, the zener diode starts conducting.
- Initially, the drain voltage stays constant, but once the **gate voltage of the NMOS crosses the threshold**, the NMOS **turns ON**.
- This **shorts the circuit**, causing a **high current** to flow.
- The high current **burns the fuse**, disconnecting the circuit and **protecting the load**.
- A **PTC (Positive Temperature Coefficient) resettable fuse** increases its resistance in response to excessive current, thereby limiting fault currents. Once the fault is cleared, the fuse automatically resets to allow normal operation.
- A **Zener diode** combined with a **crowbar protection mechanism** (implemented using a MOSFET) ensures that voltages above **18 V** are safely shorted to ground, effectively disconnecting the rest of the system from the overvoltage condition.
- Overall, this protection setup ensures that the downstream circuit receives safe power within the **9 V to 18 V range**. The mechanism is designed to **trigger instantly** when an overvoltage is detected, preventing damage to sensitive components and maintaining system integrity.

B. Audio Amplifier Circuit

The amplifier circuit is a fully discrete **Class A amplifier** designed in three stages:

1. **Q1 – PNP Transistor (Preamp Stage):**
   This stage amplifies small input signals (~10 mV) and sets the initial gain. It's biased using a voltage divider (Thevenin configuration) and includes a coupling capacitor to remove any DC offset from the source.
2. **Q2 – NPN Transistor (Voltage Gain Stage):**
   Acting as the main gain stage, this transistor operates in active mode. Proper collector-emitter biasing and bypassed emitter resistance help maximize voltage gain.
3. **Q3 – NPN Transistor (Emitter Follower Stage):**
   This stage serves as a buffer with a low output impedance. It prevents loading the previous stage and allows the circuit to drive moderate loads.

Each stage is separated using **coupling capacitors** to isolate DC biasing and pass AC signals. The amplifier is powered by a **single 18 V supply**.



Circuit : Audio Amplifier Circuit

This circuit includes a **low-pass filter at the input** to reduce noise from the incoming signal. A **coupling capacitor** is also used to block any DC voltage from entering the amplifier.

The circuit features a **three-stage multilevel amplification**, which operates similarly to a **Class-A amplifier**.

4. Simulation & Analysis

a. I analysed this circuit for two operation voltages 9v and 18v .

For 9v:

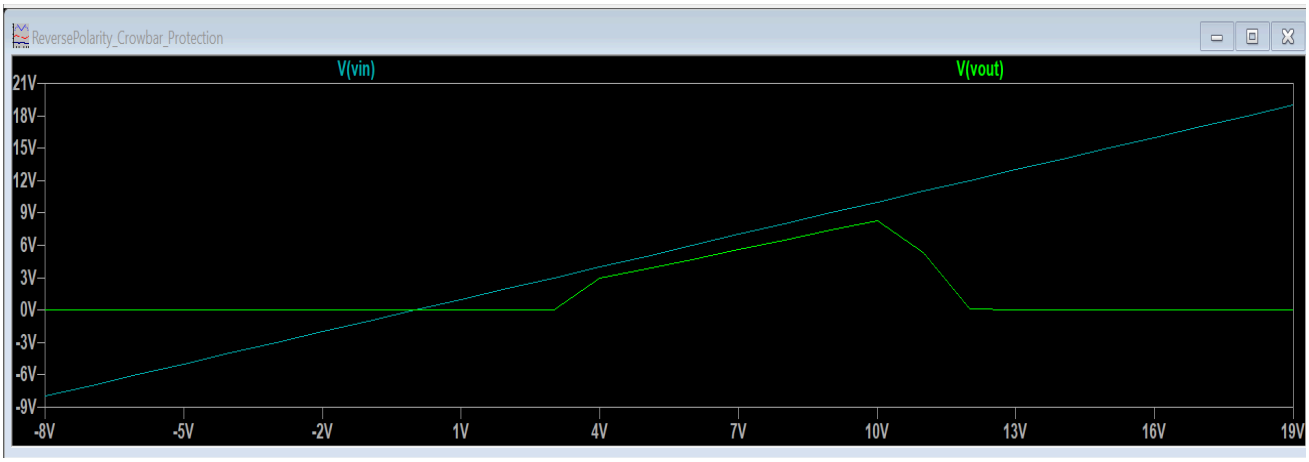
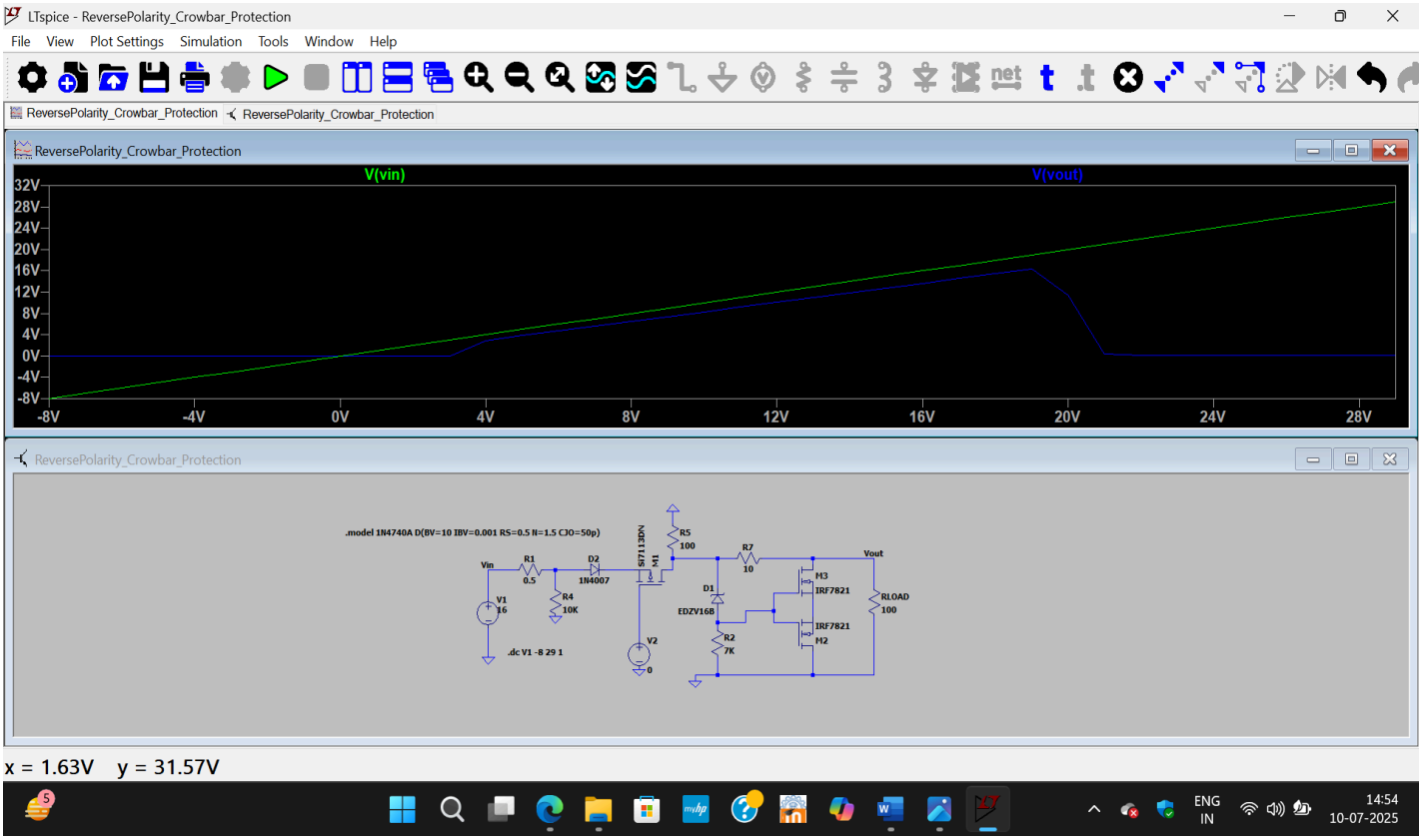


Image: simulation

I varied **V_in** between **-8 V and 19 V**, and the output behaved exactly as expected. When the input voltage reached between **12 V and 13 V**, the **output dropped to 0 V**.

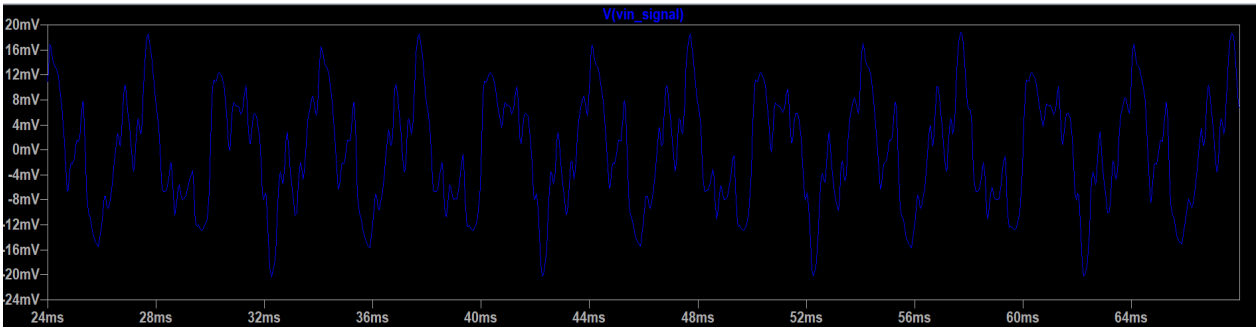
Here, the output refers to the **voltage across the load**.

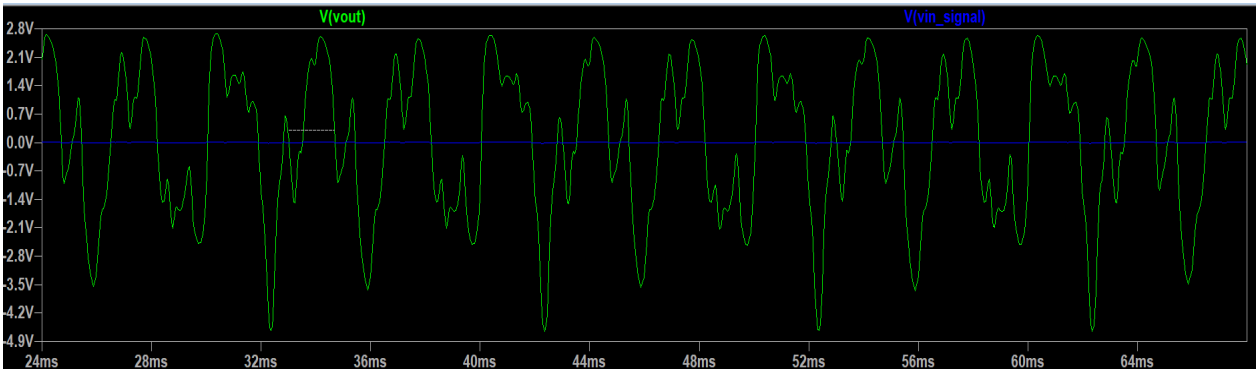
For 18v :



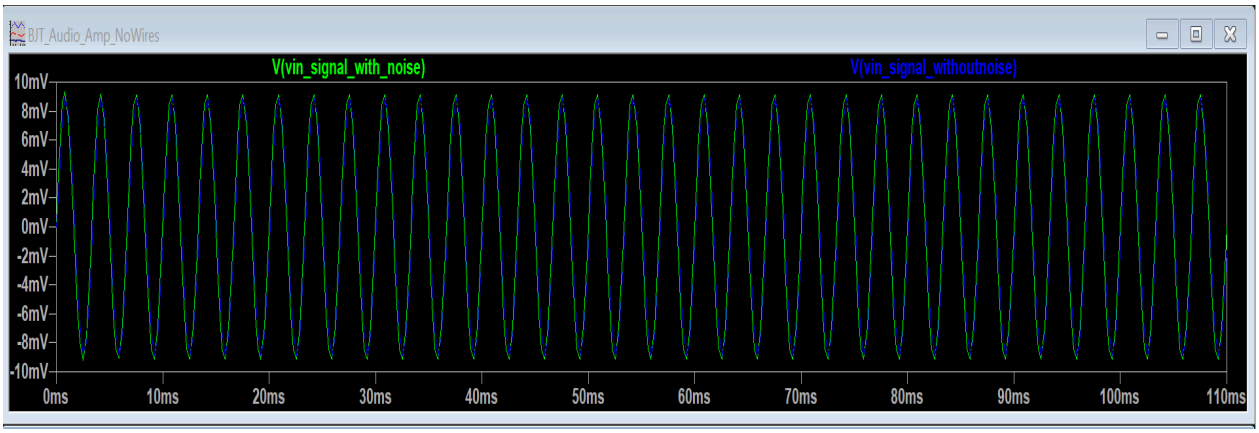
Similar for this circuit we get output 0v at 20-22v that is for when supply is 18v . so here if supply crossed 22v output will drop to 0v .

b. I apply a noised low voltage signal that not same as sine wave in first case and same as low voltage sine wave in second wave .

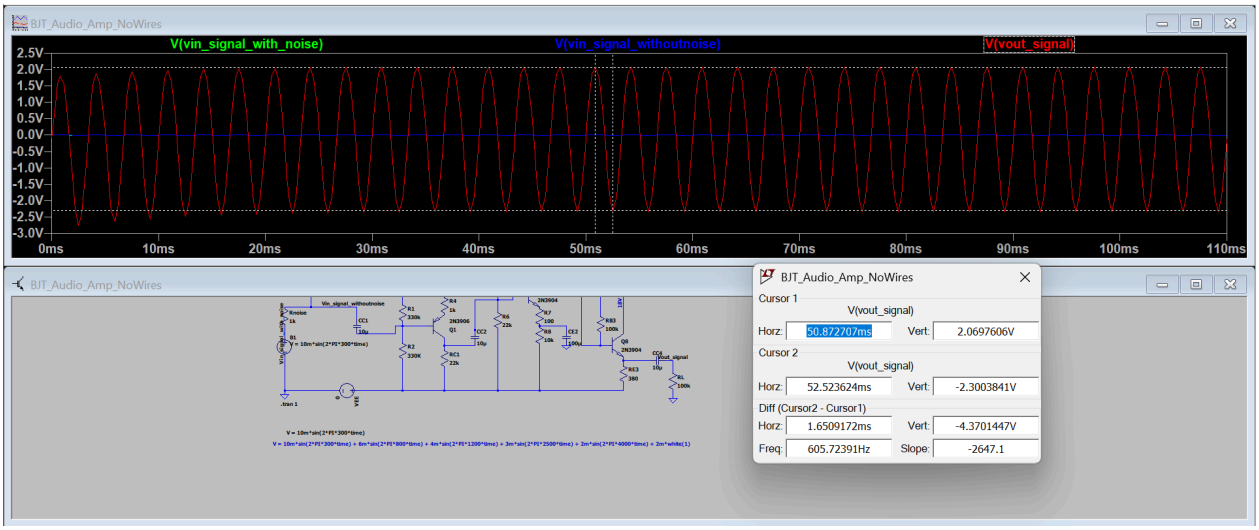




I got a amplified output signal .



Output:



Delta Vout=4.37v , delta Vin=18mv

gain=(4.37/18)*1000=242.27

gain=47.68 dB (simulated)

For circuit calculation of this circuit i attached a pdf named “calculations_of_project”

DC Analysis :

• All capacitors are open circuits.

• The input signal (Vin) is ignored in DC analysis because it is blocked from entering the circuit by the coupling capacitor, which acts as an open circuit for DC.

First Stage DC Analysis

- Applying Thevenin representation to the following circuit:

$$R_{B1} = R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{330 \times 10^3}{2} = 165\,\text{k}\Omega$$

$$V_{B1} = V_{Th} = V_{CC} \times \frac{R_2}{R_1 + R_2} - V_{EE} \times \frac{R_1}{R_1 + R_2}$$

$$= 9 \times \frac{330 \times 10^3}{2(330 \times 10^3)} - 9 \times \frac{330 \times 10^3}{2(330 \times 10^3)} = 0\,\text{Volt}$$

- Apply Kirchhoff’s Voltage Law (KVL) to the input loop, which includes the Thevenin resistance R_{B1}, the base-emitter junction, and the emitter resistor:

$$V_{B1} - I_{B1}R_{B1} - V_{BE} - I_{E1}(R_3 + R_4) + V_{CC} = 0$$

$$V_{B1} - I_{B1}R_{B1} - V_{BE} - I_{B1}(1 + \beta_1)(R_3 + R_4) + V_{CC} = 0$$

$$0 - I_{B1} \cdot 165k - 0.7 - I_{B1}(1 + 205)(33k + 1k) + 9 = 0$$

$$I_{B1} = \frac{9 - 0.7}{165000 + 206 \times 34000} = 1.15\,\mu\text{A}$$

$$I_{C1} = \beta_1 I_{B1} = 205 \times 1.15 \times 10^{-6} = 0.235\,\text{mA} \approx 0.24\,\text{mA}$$

$$I_{E1} = (\beta_1 + 1) I_{B1} = 206 \times 1.15 \times 10^{-6} = 0.24\,\text{mA}$$

$$g_{m1} = \frac{I_{C1}}{V_T} = \frac{0.24 \times 10^{-3}}{0.026} = 9.23\,\text{mA/V}$$

$$r_{\pi 1} = \frac{\beta_1}{g_{m1}} = \frac{205}{9.23 \times 10^{-3}} = 22.21\,\text{k}\Omega$$

Second Stage DC Analysis

- Applying Thevenin representation:

$$R_{B2} = R_{Th2} = \frac{R_5 R_6}{R_5 + R_6} = \frac{47 \times 22}{47 + 22} = 15\,\text{k}\Omega$$

$$V_{B2} = V_{Th2} = V_{CC} \times \frac{R_6}{R_5 + R_6} + (-V_{EE}) \times \frac{R_5}{R_5 + R_6}$$
$$= 9 \times \frac{22}{47 + 22} - 9 \times \frac{47}{47 + 22} = -3.26\,\text{V}$$

- Apply KVL:

$$V_{B2} - I_{B2}R_{B2} - V_{BE} - I_{E2}(R_7 + R_8) + (-V_{EE}) = 0$$
$$V_{B2} - I_{B2}R_{B2} - V_{BE} - I_{B2}(1 + \beta_2)(R_3 + R_4) - V_{EE} = 0$$
$$3.26 - I_{B2} \cdot 15k - 0.7 - I_{B2}(1 + 287)(100 + 10000) - 9 = 0$$
$$I_{B2} = \frac{9 - 3.26 - 0.7}{15000 + 288 \times 10100} = 1.72\,\mu\text{A}$$
$$I_{C2} = \beta_2 I_{B2} = 287 \times 1.72 \times 10^{-6} = 0.49\,\text{mA} \approx 0.5\,\text{mA}$$
$$I_{E2} = (\beta_2 + 1) I_{B2} = 288 \times 1.72 \times 10^{-6} = 0.5\,\text{mA}$$
$$g_{m2} = \frac{I_{C2}}{V_T} = \frac{0.5 \times 10^{-3}}{0.026} = 19.23\,\text{mA/V}$$
$$r_{\pi 2} = \frac{\beta_2}{g_{m2}} = \frac{287}{19.23 \times 10^{-3}} = 14.924\,\text{k}\Omega$$

Third Stage DC Analysis

- Apply KVL:

$$V_{CC} - I_{B3}R_{B3} - V_{BE} - I_{E3}R_{E3} = -V_{EE}$$

$$V_{CC} - I_{B3}R_{B3} - V_{BE} = I_{B3}(1+\beta_3)R_{E3}$$

$$9 - I_{B3} \cdot 100k - 0.7 = I_{B3}(1+214) \cdot 390$$

$$I_{B3} = \frac{9+9-0.7}{100000 + 215 \times 390} = 94.1\,\mu\text{A}$$

$$I_{C3} = \beta_3 I_{B3} = 214 \times 94.1 \times 10^{-6} = 20.1\,\text{mA}$$

$$I_{E3} = (\beta_3 + 1) I_{B3} = 215 \times 94.1 \times 10^{-6} = 20.2\,\text{mA}$$

$$g_{m3} = \frac{I_{C3}}{V_T} = \frac{20.1 \times 10^{-3}}{0.026} = 773\,\text{mA/V}$$

$$r_{\pi 3} = \frac{\beta_3}{g_{m3}} = \frac{214}{773 \times 10^{-3}} = 276.84\,\Omega$$

AC Analysis

$$R_{in} = R_{B1} \parallel (r_{\pi 1} + (1+\beta_1)R_{E1}) = 165 \parallel (22.21 + (1+205)\times 1) = 165 \parallel 228.21 = 95.76\,\text{k}\Omega$$

$$R_{out} = R_{E3} \parallel R_L \parallel \left(\frac{R_{C1} \parallel R_{B2} + r_{\pi 3}}{\beta_3 + 1}\right) = 390 \parallel 10000 \parallel \left(\frac{100000 \parallel 6800 + 276.84}{215}\right) = 1.312\,594\,\Omega$$

$$v_{\pi 1} = v_{in} \times \frac{r_{\pi 1}}{r_{\pi 1} + (1+\beta_1)R_{E1}}$$

$$v_{\pi 2} = -g_{m1} v_{\pi 1} \times \left(\frac{R_{C1} \parallel R_{B2}}{(R_{C1} \parallel R_{B2}) + r_{\pi 2} + (1+\beta_2)R_{E2}}\right) \times r_{\pi 2}$$

$$v_{\pi 3} = -g_{m2} v_{\pi 2} \times \left(\frac{R_{C2} \parallel R_{B3}}{(R_{C2} \parallel R_{B3}) + r_{\pi 3} + (1+\beta_3)(R_{E3} \parallel R_L)}\right) \times r_{\pi 3}$$

$$v_o = (R_{E3} \parallel R_L) \times \left(\frac{v_{\pi 3}}{r_{\pi 3}} + g_{m3} v_{\pi 3}\right) = (R_{E3} \parallel R_L) \times v_{\pi 3}\left(\frac{1}{r_{\pi 3}} + g_{m3}\right)$$

$$A_v = \frac{v_o}{v_{in}} = -g_{m3} g_{m2} v_{in} \times \frac{r_{\pi 1}}{r_{\pi 1} + (1+\beta_1)R_{E1}} \times \frac{R_{C1} \parallel R_{B2}}{(R_{C1} \parallel R_{B2}) + r_{\pi 2} + (1+\beta_2)R_{E2}} \times r_{\pi 2}$$

$$\times \frac{R_{C2} \parallel R_{B3}}{(R_{C2} \parallel R_{B3}) + r_{\pi 3} + (1+\beta_3)(R_{E3} \parallel R_L)} \times r_{\pi 3} \times (R_{E3} \parallel R_L) \times \left(\frac{1+\beta_3}{r_{\pi 3}}\right)$$

$$= \beta_1\beta_2(1+\beta_3) \times \left(\frac{(R_{C1} \parallel R_{B2})(R_{E3} \parallel R_L)(R_{C2} \parallel R_{B3})}{(r_{\pi 1} + (1+\beta_1)R_{E1})((R_{C1} \parallel R_{B2}) + r_{\pi 2} + (1+\beta_2)R_{E2})(R_{C2} \parallel R_{B3}) + r_{\pi 3} + (1+\beta_3)(R_{E3}}\right.$$

$$= 371.98\,\text{V/V} = 51.41\,\text{dB}$$

$$\frac{A_v}{\sqrt{2}} = 263.02\,\text{V/V} = 48.4\,\text{dB}$$

So **calculated gain=51.41 dB**

5. Conclusion

This project successfully integrates two critical aspects of analog design: **safe power delivery** and **clean signal amplification**. The protection circuit proved reliable in blocking reverse polarity and overvoltage events without false triggering. Meanwhile, the discrete amplifier design achieved high voltage gain, minimal distortion, and adequate bandwidth for real audio applications.

While Class A amplifiers are inherently inefficient in power usage, they are valued for their **linearity** and **faithful signal reproduction**, both of which were observed during testing. Additionally, working with discrete components provided deep insights into biasing, signal coupling, and transistor behaviour, making the learning experience technically enriching.

6. Key Learnings

1. ***Understanding BJT Biasing:*** *Learned how to bias PNP and NPN transistors using resistor networks correctly and verified the operation using both DC and AC analysis.*

2. ***Multi-Stage Amplifier Design:*** *Understood how to cascade transistor stages for greater gain and how to isolate them using capacitive coupling.*

3. ***Protection Circuit Techniques:*** *Applied real-world techniques like crowbar protection, MOSFET polarity protection, and current limiting using PTC fuses.*

4. ***Simulation Workflow:*** *Strengthened skills in using LTspice for both schematic design and time-domain analysis.*

Reference:

1. *Sedra, A. S., & Smith, K. C. (2020). Microelectronic Circuits,*
2. *Analog circuits , prof: Mb*