



## Assuming there is block design project opened in vivado gui. How to generate TCL script for recreation this project in future?

To generate a Tcl script in Vivado GUI so you can re-create your current block design project in the future, follow these steps:

### 1. Open your block design

- Make sure your block design is active/open in Vivado.

### 2. Export the block design to Tcl

- In Vivado GUI, go to **File** → **Export** → **Export Block Design**.
- In the Export Block Design dialog, specify the desired name and location for your Tcl script.
- Click **OK**. This will generate a Tcl file with commands sufficient to recreate your block design.<sup>[1]</sup>
- Alternatively, you can type the following in the Vivado Tcl Console:

```
write_bd_tcl <path_to_file>/<filename>.tcl
```

- If you want to include block layout information, use:

```
write_bd_tcl -include_layout <path_to_file>/<filename>.tcl
```

- For hierarchical blocks only:

```
write_bd_tcl -hier_blks [get_bd_cells /hier_block_name] <path_to_file>/<hier_file>.tcl
```

*Note:* The generated script only records parameters that you explicitly changed. Default IP parameters and tool-modified parameters may not be captured. Block layout info is omitted unless you use the `-include_layout` option.<sup>[1]</sup>

### 3. Export overall project information to Tcl (optional)

- To export the entire Vivado project (settings, sources, block design recreation scripts, etc.), go to **File** → **Project** → **Write Tcl**.
- In the dialog, select options such as **Copy sources to new project** and **Recreate Block Design using Tcl** as needed.
- Save the file.

- Or use the Tcl Console:

```
write_project_tcl <path_to_file>/<filename>.tcl
```

- Add options for how sources and block designs are included:

```
- `write_project_tcl -use_bd_files <path>/<filename>.tcl` (imports BD from de
```

```
- `write_project_tcl -no_copy_sources -use_bd_files <path>/<filename>.tcl` (u
```

#### 4. Re-create the project in the future

- In a new Vivado session, source the Tcl file you created:

```
source <path_to_file>/<filename>.tcl
```

- This will regenerate the project and block design per your saved state.

#### Best Practice:

For version control, store your Tcl recreation scripts (and HDL/IP sources) in your repository. Do not version control generated files like .xpr (Vivado project file).<sup>[2]</sup>

By following these steps, you can reliably recreate your Vivado block design project in future sessions or on different machines. Ensure all required sources are available and that you use the Tcl file and Vivado version with which it was generated for best consistency.

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1. <https://docs.amd.com/r/en-US/ug994-vivado-ip-subsystems/Exporting-a-Block-Design-to-a-Tcl-Script-in-the-IDE>
2. <https://www.fpgadeveloper.com/2014/08/version-control-for-vivado-projects.html/>
3. <https://forum.digilent.com/topic/25590-vivado-tcl-build-scripts/>
4. <https://stackoverflow.com/questions/46702015/is-it-possible-to-open-a-vivado-project-via-tcl-and-export-it-via-write-project>
5. <https://community.element14.com/technologies/fpga-group/f/forum/51343/sharing-vivado-projects>
6. <https://www.koheron.com/software-development-kit/documentation/fpga/block-design/>
7. [https://www.xilinx.com/support/documents/sw\\_manuals/xilinx2022\\_2/ug894-vivado-tcl-scripting.pdf](https://www.xilinx.com/support/documents/sw_manuals/xilinx2022_2/ug894-vivado-tcl-scripting.pdf)
8. [https://xilinx.github.io/Alveo-Cards/cards/ul3524/build/html/docs/Docs/loading\\_ref\\_proj.html](https://xilinx.github.io/Alveo-Cards/cards/ul3524/build/html/docs/Docs/loading_ref_proj.html)
9. <https://stackoverflow.com/questions/57291317/recreating-a-vivado-project-from-a-tcl-file-without-copying-the-sources-over>
10. <https://www.edaboard.com/threads/creating-a-tcl-script-for-specific-hardware-design-in-ip-integrator.401726/>
11. [https://www.reddit.com/r/FPGA/comments/1dctfcb/amd\\_vivado\\_tcl\\_based\\_project\\_no\\_block\\_design/](https://www.reddit.com/r/FPGA/comments/1dctfcb/amd_vivado_tcl_based_project_no_block_design/)
12. <https://www.youtube.com/watch?v=BXhLFecEPc8>
13. <https://gist.github.com/imrickysu/66b6321c64713429b97fa96db20ebd0b>
14. <https://www.fpgarelated.com/thread/14179/vivado-tcl>

15. <https://adaptivesupport.amd.com/s/article/56421>
16. <https://docs.amd.com/r/2021.2-English/ug994-vivado-ip-subsystems/Using-Tcl-Scripts-to-Create-Projects-and-Block-Designs>
17. <https://docs.amd.com/r/en-US/ug895-vivado-system-level-design-entry/Tcl-Command-for-Saving-a-Project>
18. [https://www.xilinx.com/support/documents/sw\\_manuals/xilinx2022\\_1/ug994-vivado-ip-subsystems.pdf](https://www.xilinx.com/support/documents/sw_manuals/xilinx2022_1/ug994-vivado-ip-subsystems.pdf)