Major Team Project

Audio Amplifier Report

ELEC3404 Electronic Circuit Design

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Assignment Title: ELEC3404 Audio Amplifier Team Project Report			
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Design

The objective of this project is to understand the principles of a Darlington push-pull power amplifier and its application, design and construct an audio power amplifier on a vero board and heatsink and trouble shoot the circuit as well as testing the performances of the amplifier.

The components must be defined and selected from calculated and assumed design parameters and then solder onto the PCB board. The selection of the components will be tested prior to soldering using a prototype circuit constructed on a bread board. Testing will involve measuring properties of the circuit performance under laboratory conditions.

The audio amplifier uses a DC voltage power supply and outputs power up to a wattage of three. The aim is to acquire a power efficiency greater that 45% (when tested with an 8Ω or 8.2Ω dummy load) The circuit consists of two stages:

- The **input stage** where the input signal is received for voltage amplification.
- The **output stage** where the current is amplified to run high power to the speaker.

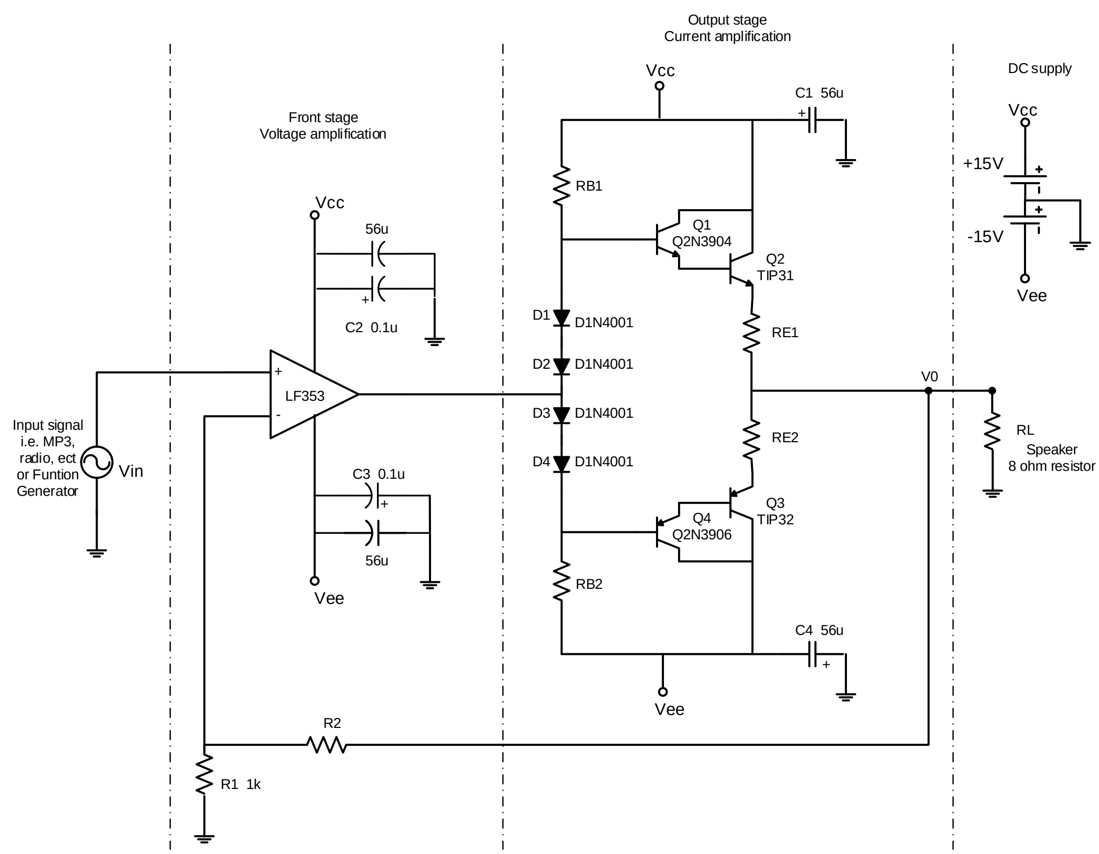

Figure 1: Circuit Diagram of Audio Amplifier

Design Parameters

<u>Note:</u> since the current is amplified by a Darlington push-pull configuration, the R_E values are set to 1kΩ due to the thermal buffer of the BJT's. The non-inverting op-amp pre-amplifies the audio signal with a grain of $\frac{10V}{V}, where\ A_v = \frac{V_{out}}{V_{in}} = 10.$

Given $R_1 = 1k\Omega\ and\ A_v = \frac{R_1+R_2}{R_1} \rightarrow 10 = \frac{1000+R_2}{1000} \rightarrow R_2 = 9k\Omega$. Using KVL to the circuit.

$P_{out} = I^2{}_{rms}R_L = 5W, where\ R_L = 8\Omega\ \&\ I_{rms} = \sqrt{\frac{P_{out}}{R_L}} = \sqrt{\frac{5}{8}} = 0.79A$ Set desired output power.

$\therefore I_{peak} = \sqrt{2}I_{rms} = 1.12A$

The V_{BE} is given to be $0.6V, \therefore V_{RB1} = V_{cc} - (0.6 + 0.6 + I_P \cdot 1\Omega + I_P \cdot 8\Omega = 3.738V$

$\therefore R_{B1} = \frac{V_{RB1}}{I_{RB1}} = 4.51k\Omega = R_{B2}, where\ I_{BQ1} = \frac{I_p}{(B)(B_2)} = \frac{\sqrt{1.25}}{(60)(25)} = 0.745kA$ and this is used to derive $I_{RB1} \times 0.9 = I_{BQ1} \rightarrow I_{RB1} = 0.828kA$

$R_{E1} = 1k\Omega = R_{E2}$

Spice Simulation

Transient Analysis

The following table of values shows the maximum voltage input that can be delivered to the simulated circuit, with an unchanged frequency on the function generator and the maximum input was found to be approximately **1.12V**. This was measured using methods of transient analysis. Furthermore, R_{B1} and R_{B2} was adjusted to maximize the swing of the output voltage and the above values in the design parameters section are the final values used in this project.

Table 1: Finding Maximum Output (Clipping)

Input (V)	Frequency (kHz)	Clipping (Y/N)
1	1	N
1.12	1	N
1.5	1	Y
2	1	Y

Power Calculations

The power supplied by V_{cc} is equal to the following equation:

$$P_{V_{CC}} \cong \frac{1}{\pi} \cdot V_{CC} \cdot I_{Lpeak} = 5.35W\ (margin\ of\ error - simulated\ power\ vs\ specifications)$$

Therefore, this simulated model is measuring power at a margin of error of approximately **7%**.

The maximum power output was calculated using the peak voltage output which was measured to be **11.45V** by getting the corresponding output voltage V_{pp} when the output starts to clip.

$$Max\ Power = \frac{(\frac{V_p}{\sqrt{2}})^2}{R_L} = \frac{(\frac{11.45}{\sqrt{2}})^2}{8} = 8.19W$$

$$Power\ Efficiency\ (\eta) = \frac{Useful\ Power\ Output}{Total\ Power\ Input} = \frac{8.19}{0.45649 \times 15 \times 2} \cong \frac{8.19}{13.69} \cong 0.598 = 59.8\%$$

$$A_v = 20\log\left|\frac{V_{out}}{V_{in}}\right| = 20\log(10) = 20dB$$

DC Biasing Measurements

The table below denotes the DC bias measurements from the circuit (to three significant figures):

Table 2: DC Bias Measurements

BJT	Nodes	Voltage (V)
Q1(Q2N3904)	Base	1.22
	Emitter	0.629
	Collector	15.0
Q2(TIP31)	Base	0.629
	Emitter	0.086
	Collector	15.0
Q3(TIP32)	Base	-0.531
	Emitter	-15.0
	Collector	0.019
Q4(Q2N3906)	Base	-1.12
	Emitter	-15.0
	Collector	-0.531

AC Analysis

The voltage gain of the circuit was calculated using the following calculation:

$$A_V = \frac{11.45}{1.12} = 10.2 \rightarrow 20\log(10.2) = 20dB$$

Adjusting the frequency until the gain of the circuit is 3dB while maintaining a constant voltage. The upper 3dB was calculated to be **155 kHz**. The lower 3dB cannot be found since the circuit resembles a low-pass filter.

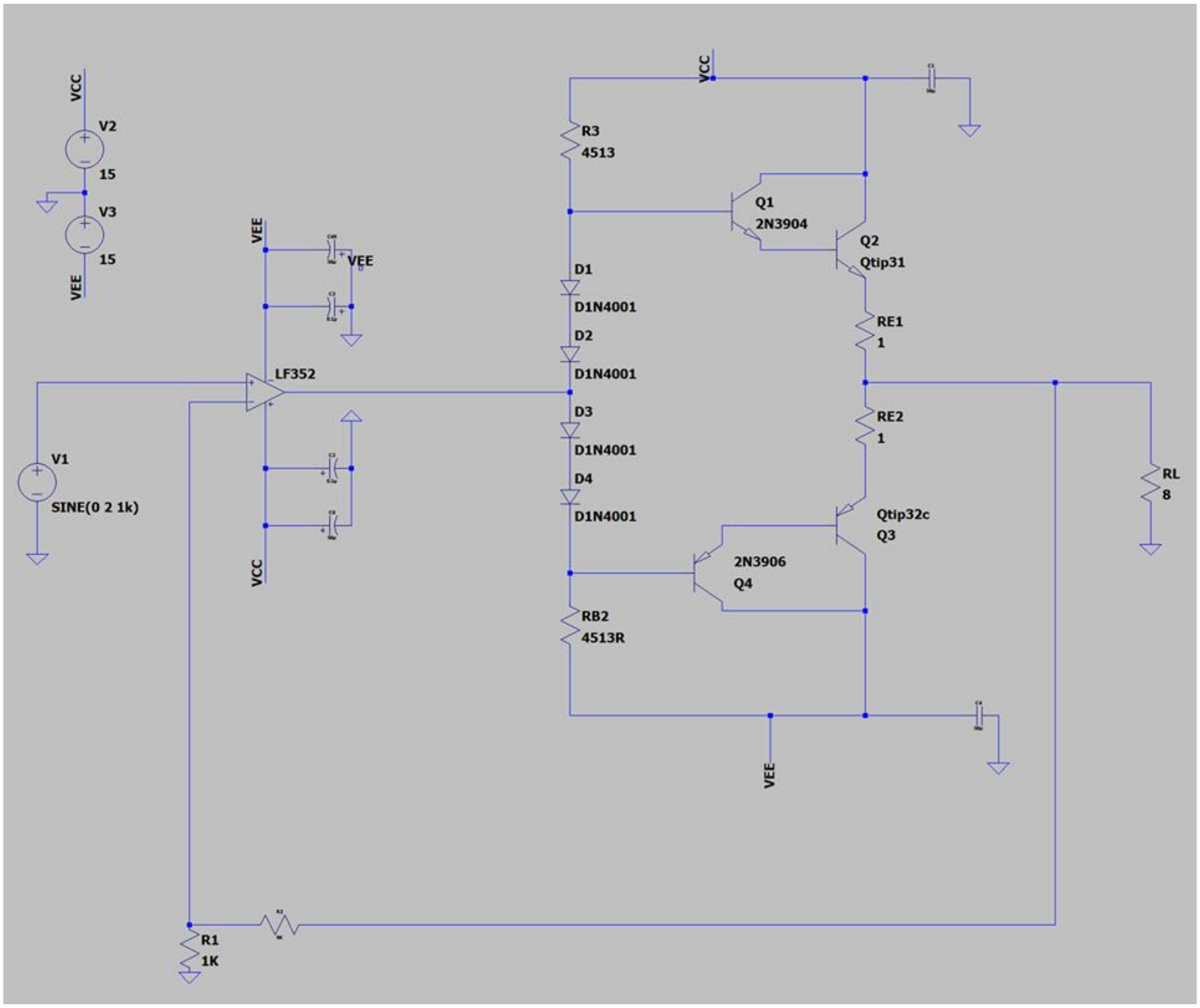

Figure 2: LTSpice Simulation Circuit

<u>Note:</u> the LF352 was changed to an LF353 for the investigation. This is displayed incorrectly in the above image due to errors with being able to load the correct Op-Amp on the project file.

Prototype Circuit

A prototype circuit based on the simulated circuit is to be implemented on a breadboard and the following section displays measurements and calculations from this circuit.

DC Biasing Measurements

The table below denotes the DC bias measurements from the circuit (to three significant figures):

Table 3: Prototype DC Bias Measurements

BJT	Nodes	Voltage (V)
Q1(Q2N3904)	Base	1.15
	Emitter	0.67
	Collector	15.1
Q2(TIP31)	Base	0.653
	Emitter	0.090
	Collector	15.0
Q3(TIP32)	Base	-0.499
	Emitter	-15.1
	Collector	0.021
Q4(Q2N3906)	Base	-1.11
	Emitter	-15.0
	Collector	-0.533

Power Calculations

Note: For this calculation the resistor that was available was an **8.2Ω** resistor, hence, power output is not accurate as the project had specified an 8Ω resistor needed to be used.

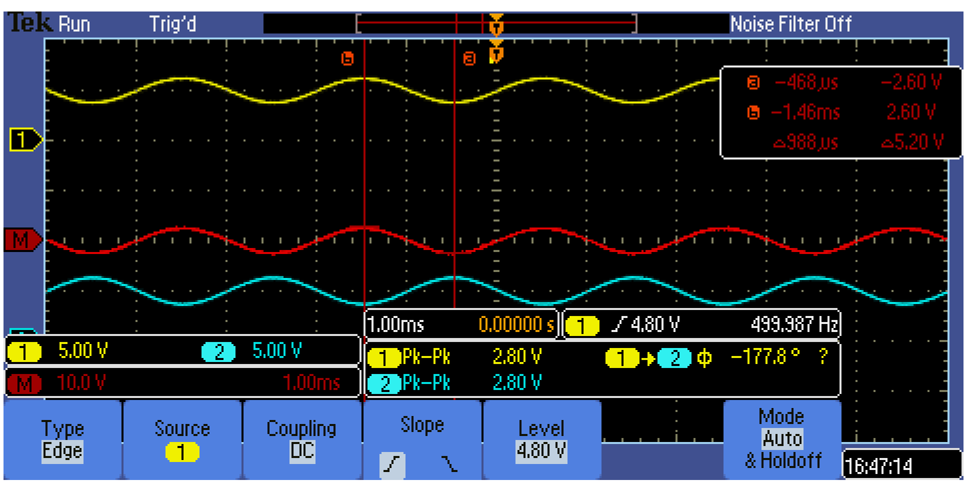

Figure 3: Voltage Gain of Prototype Circuit

The prototype circuit clips at **2.6V$_{pp}$**, with a voltage gain of $10V/V$.

$$A_v = 20\log\left|\frac{5.2}{2.6}\right| = 20\log(10) = 10V/V$$

$$P_{out} = \frac{\left(\frac{V_{peak}}{\sqrt{2}}\right)^2}{R_L} = \frac{\left(\frac{10.2}{\sqrt{2}}\right)^2}{8.2} = 6.34W$$

$$P_{out} = |(V_{CC})(I_{in})| + |(V_{ee})(I_{in})| = 15(0.398 + 0.401) = 11.99W$$

$$Power\ Efficiency\ (\eta) = \frac{Useful\ Power\ Output}{Total\ Power\ Input} = \frac{6.34}{11.99} \cong 0.529 = 52.9\%$$

Therefore, the prototype circuit satisfies the objective of output a power efficiency rating greater than 45%.

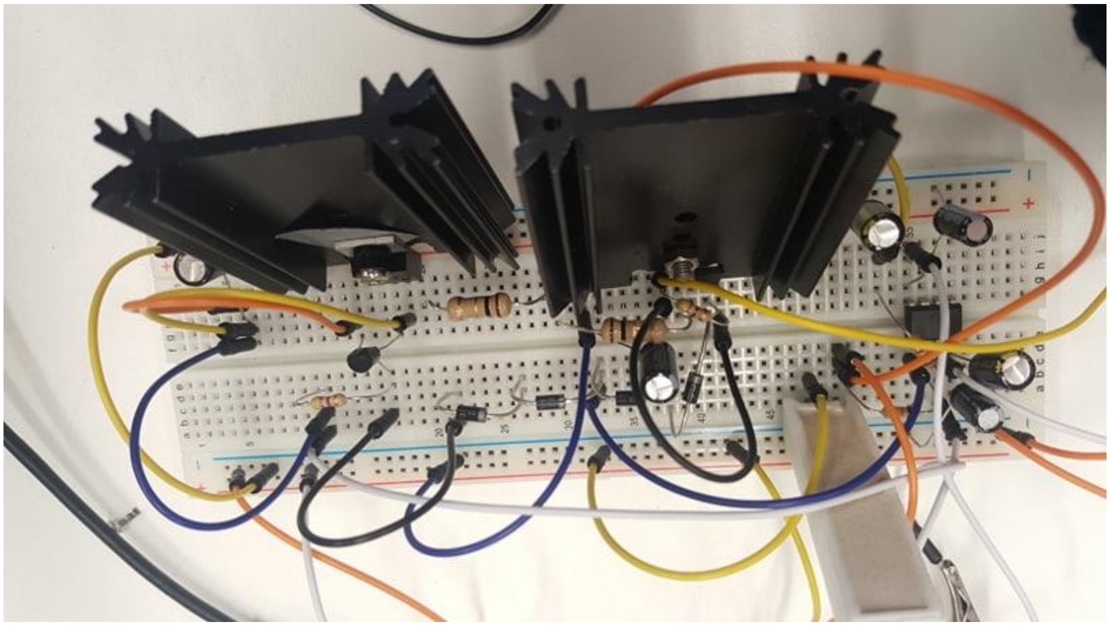

Figure 4: Prototype Circuit Model

Testing

- It was found that as V_{input} swings positive, Q_3 turns off and Q_1 supplies current to the load (standard push-pull).
- As V_{input} swings negative, Q_3 supplies the base current for Q_2 into V_{input}.
- The resistors are required to add maintain the required amperes.

Op-Amp

Node	**Voltage (V_{pp})**
Input	0.58
Output	5.20

Darlington-Pair

Component (V_{BE})	**Voltage (V)**
Q1	1.41
Q4	-1.54

PCB Tests and Measurements

Table 4: Finding the Maximum Voltage Input

Voltage (V_{pp})	Current (A)	Clipping (Y/N)
1	0.38	N
1.35	0.48	N
1.7	0.57	Y

$\therefore 14.6 \times 0.7 = 10.22V/V$

Power Rating

The maximum output power occurs at the signal clipping of **1.7V_{pp}**. Therefore, the input and output power calculation and power efficiency percentage are as follows:

Note: For this calculation the resistor that was available was an **8.2Ω** resistor, hence, power output is not accurate as the project had specified an 8Ω resistor needed to be used.

$$P_{output} = I^2R = (0.945)^2(8.2) = 7.40W\ (Power\ Output)$$

$$P_{input} = VI = (14.98)(0.44) + (14.53)(0.46) = 13.28W$$

$$\therefore Power\ Efficiency\ (\eta) = \frac{P_{output}}{P_{input}} \cong \frac{7.4005}{13.275} \times 100 \cong 55.75\%$$

In summation, the desired power efficiency that the projected aimed towards has been achieved (>45%). The design specifications have been satisfied with the construction of the audio amplifier.

At mid-band frequency, the circuit has a voltage gain of approximately **20dB**, hence, keeping a constant voltage while trying to get the upper frequency with a gain drop of 3dB the frequency is approximately **148 kHz**, and the lower 3dB cut-off frequency was measured to be approximately 32Hz.

Therefore, the frequency response results are lower than the values plotted by the LTSpice simulation. Furthermore, the PCB plot of the frequency response displays a lower cut-off compared to the low-pass represented in LTSpice.

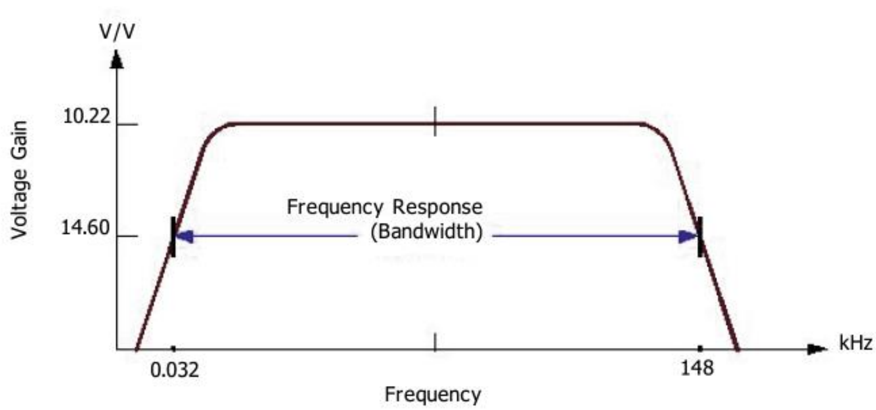

Figure 5: Frequency Response Plot

Figure 6: PCB Circuit Model

Audio Output Testing

The function generator and the PCB output (or 8.2Ω dummy load) was replaced with a male audio three millimeter jack and a speaker respectively. With the audio jack connected to the computer's female audio jack input, audio could now be played and the on potentiometer on the PCB can be used to vary the volume of the audio outputted.

Rotating the potentiometer clockwise decreases the output volume and rotating it anticlockwise increases the output volume.

Project Questions

1. **How much is the voice from the audio source amplified?**
   The audio amplifier has a measured gain of approximately **10.2V/V**, hence the audio source can be amplified by **20dB.** Using the gain, it can be concluded that the amplification is ten times as loud as the default output.
2. **How much current is drawn from the DC power supply with different volume?**
   Current drawn from the DC power supply was measured to be **0.945A** at full volume or rotation (anticlockwise) on the potentiometer. However, at low volume approximately **0.44A** current is drawn from the power supply.

Conclusion

The objective of the investigation is to record all findings between the simulation circuit, prototype circuit and PCB model of the audio amplifier and draw similarities and differences in properties between these models of the circuit (theoretical and practical comparison of findings). The specific properties that were desired include the power efficiency, DC bias analysis and output power performance.

The simulation and PCB model display a drop in power efficiency most likely due to heat accumulation. The prototype displays a larger drop in power in comparison to the simulation most likely due to power loss from heat in BJT’s Q2 and Q3. There are also, as expected, no significant difference between Q1, Q2, Q3 and Q4 voltage values across each node using DC bias analysis between the simulation and prototype model.

When testing the prototype board and PCB model, the DC power supply displayed an overload warning for V_{cc} and V_{ee}. This was due to the restriction of current (0.5A) on the power supply itself. It is recommended for future experiments that at least a one amp DC power supply is utilized. The simulation displayed the frequency response to display only a higher cut-off frequency however, the prototype circuit or PCB displays a lower cut-off frequency and an upper cut-off frequency.

References

Motorola. (1995). *Semiconductor Technical Data.* Motorola, Inc. .

Technologies, D. P. (n.d.). *NPN General Purpose Amplifier.* National Semiconductor.

Appendix

Prototype & PCB Circuit Components

The following table displays the values of the resistors used in the PCB model circuit:

Table 5: Resistor Values for PCB & Prototype

Resistor	Ohms ($k\Omega$)
R_1	1.0
R_2	8.2
R_{B1}	4.7
R_{B2}	4.7
R_{E1}	1.0
R_{E2}	1.0
R_L	8.2

Simulation Model Components

The following table displays the values of the resistors used in the simulation model:

Table 6: Resistor Values for Simulation Circuit

Resistor	Ohms ($k\Omega$)
R_1	1.0
R_2	9.0
R_{B1}	4.5
R_{B2}	4.5
R_{E1}	1.0
R_{E2}	1.0
R_L	8.0