UEM

University of Engineering & Management, Kolkata

1st Term Examination, March, 2019

Course: B.Tech (CSE) Semester: 4th

Paper Name: Computer Organization & Architecture

Paper Code: CS403

Full Marks: 50 Time: 1 hour 30 minutes

Group-A (10 marks)

Answer any 5. Each question is of 2 marks.

1. **A)** Evaluate the RPN for the following : **(A-B)*[C/(D+E)+F]**
   B) How many RAM chips each of size 256 X 2 is required to built a memory of 1K X 2?
   C) Show the addressing for the program assuming von Neumann architecture for storing the following:
   i. Assume that the program (instruction) has a length of 2048 bytes and the program starts from the address 1000.
   ii. The input data size is 512 bytes and stores from 4050.
   iii. The results of 50 bytes generated after program execution are stored at address 5000.
   D) What is OS? What are the tasks of OS?
   E) State the difference between register direct and register indirect mode using suitable example.
   F) State the difference between a multiprogramming and multitasking OS.
   G) State the advantages and disadvantages of using GPR based CPU Organization over single Accumulator based CPU Organization.

Group-B (10 marks)

Answer any 2. Each question is of 5 marks.

2. **A)** What value remains on the stack after the following sequence of instructions?

```
PUSH #3
PUSH #5
PUSH #4
ADD
PUSH #7
SUB
MULT
```

   B) What are the advantages of using general purpose register based CPU Organization over Single accumulator based organization? **[3+2=5]**

2. Design a structure of an ISA computer. How does Von-Neumann Bottleneck can be solved using cache memory? **[3+2=5]**

3. What is an instruction cycle? What are the five major phases of an instruction cycle? Draw the flow diagram for an instruction cycle. [1+1+3=5]

4. A) Assuming all registers initially containing 0, what is the value of R1 and R0 after the following instruction sequence is executed?

```
MOV R1, #6
MOV R2, #5
ADD R0, R1, R1
SUB R1, R0, R2
MULT R0, R1, R1
```

B) Briefly explain the PC-Relative addressing mode under CLASS – IV addressing. [3+2=5]

Group-C (30 marks)

Answer any 2. Each question is of 15 marks.

5. A) Use sequential method of multiplication to multiply M = 6 (multiplicand) and Q = 14 (multiplier). Show the intermediate steps used to determine the answer.
B) Assume that an LSI IC at semiconductor memory stores 2048 bits. Assume a main memory unit of 2048 ICs. How many bytes do these ICs stores?
C) Suppose a 300 MHz machine does the number of context switching 30 times per second. How many cycles are there in each time-slice?
D) To achieve a speed up of 8 on a program that originally took 160ns to execute, what must be the execution time of the program be reduced to? [7 + 2 + 3 + 3 = 15]

6. A) A hardwired control unit contains an IR of 16 bits. Decode the opcode stored in the IR. Use a n bit sequential counter to generate the T states.
B) Let us assume the opcode of the instruction ADD A, B is $1F_H$. What is the contain of CAR? How does control memory decode this opcode?
C) State the differences between Polled IO, interrupt Initiated IO and DMA?
D) Why CISC Architecture does uses complex and large number of instructions? What are the advantages and disadvantages of Variable Length Instruction Format?
E) State the differences between Strobe control technique and Handshaking technique?
[3 + 3 + 3 + 3 + 3 = 15]

7. A) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts:

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	50000	1
Data transfer	35000	2
Floating point arithmetic	20000	2
Branch	6000	3

Calculate the effective CPI, MIPS rate and execution time for this program
B) State and derived the equation of Amdahl's Law.
C) Assume that 25% of our program is floating-point operations and that the rest of the program is integer operations. A design team proposes to speed up the floating-point operations by five times using a dedicated floating-point hardware unit. Another team proposes to speed up just the integer operations by two times. Given that we have the budget to spend on only one design, which design would we fund, and why?
D) Suppose that we are considering an enhancement to the processor used for scientific computation. Floating point instructions are improved to run twice as fast, but only 10% of the time was spent on these instructions originally. How much faster is the new

machine? How much faster would the new machine be if floating point instructions become 100 times faster?

E) An instruction pipeline consists of 4 stages – Fetch (F), Decode field (D). Execute (E) and Result Write (W). The 5 instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below. Find the number of clock cycles needed to perform the 5 instructions.

	No. of clock cycles needed for			
Instruction	**F**	**D**	**E**	**W**
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

[3 + 3 + 3 + 3 + 3 = 15]

8. **A)** Evaluate the following expression using 0, 1, 2 and 3 – addressing instruction length and state each one's advantage: **X = (A-B) / (C+D),** using suitable assumptions.
B) With proper example, state the difference of the instructions: LOAD and STORE.
C) Convert the given arithmetic expression to RPN :

(A+B^D) / (E-F) + G

[(2.5*4)+2+3=15]

9. **A)** Draw the flow chart to illustrate the non-restoring division algorithm. Use this to evaluate an example where DIVIDEND Q = 7 = 0111 and DIVISOR M = 3 = 0011.
B) Draw the basic block diagram and explain with an example, the working of a binary Adder-Subtractor composite unit.

[10+5=15]

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