International Institute of Information Technology, Hyderabad

(Deemed to be University)

EC2.101 – Digital Systems and Microcontrollers

Mid Semester Examination

Max. Time: 1.5 Hr **Max. Marks: 40**

CALCULATORS ARE NOT ALLOWED

Numbers in square brackets [x] after a statement show the marks for that question.
Numbers in {} brackets are for administrative use. Please ignore.

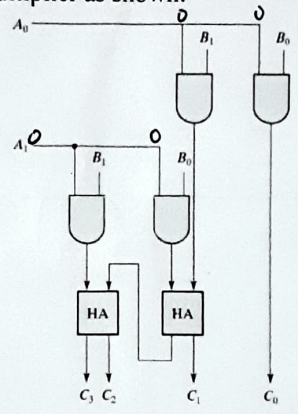
Q1. Imagine there is a terrible crime, and the police catch hold of four suspects: Abdul, Bishnoi, Carren and David. The police questions them and after a lot of investigation, finds out that they are deceiving the police in a set pattern:

i. Abdul is lying only when either Bishoi is telling the truth, or Carren is lying.
ii. Bishnoi is lying only when either Abdul is lying, or David is telling the truth.
iii. Carren is lying only when Abdul is lying.
iv. David is telling the truth only when either Abdul and Bishnoi are both lying, or Carren is lying.

Find out the condition when *all the above* statements are simultaneously true. Who is telling the truth? (Hint: the "or" in the above statements is inclusive).

[10 marks]{CO-1}

Q2. Say we create a 2-bit binary multiplier as shown:



However, when we test the circuit, we find that the output is correct only for the four cases when A=10 or 11 and B=01 or 11. We investigate and find out that because of a problem with the breadboard, one of the internal wires is permanently getting connected to either ground or VDD, i.e., it is either stuck at ground or VDD level. Can you find out which wire is problematic and what value it is getting stuck at?

[10 marks]{CO-2}

Q3. In the n-bit binary adder, there is a choice between the speed and power/area of the circuit. We can make a fast circuit with the carry lookahead logic, or we can make a slow circuit with cascaded full adders. Let us quantify the circuit complexity increase in going from the simple full adder-based circuit to the carry lookahead circuit. Calculate the number of transistors in each implementation for an n-bit binary adder. (Consider a two level AND-OR implementation for carry look ahead circuit, 2-input ExOR is 16 transistors and 3-input ExOR is obtained using two two-input ExOR).

[10 marks]{CO-1}

Q4. A 4-digit decimal number of the form (*aabb*) is a perfect square. What is the value of the digits *a* and *b*? Provide detailed mathematical reasoning.

[10 marks]{CO-2}

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End Semester Examination

Max. Time: 3 Hr **Max. Marks: 70**

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Q1. Let's say we are working in the ternary system (radix = 3). However, we need to create circuits using Boolean logic for the operations. A simple operation is to add two numbers. Given two 1-digit ternary numbers, design a circuit that produces their sum. [Hint: you will require 2 wires to represent 1-digit of ternary].

[12 marks]{CO-1}

Q2. We are given a serial stream of bits. Within this bit stream, we want to see if there is a 4-bit prime number. Design a circuit that outputs '1' if there is a 4-bit prime number in a given bit stream. The output should be active for one clock cycle upon detection of the prime number. If the next combination of 4 bits is also prime, the output should remain '1'. For example, bit stream 10111 will produce output '1' for two cycles, because 0111 and 1011 are both prime.

[12 marks]{CO-3}

Q3. Most of the arithmetic happens in a computer using 2's complement notation. Suppose we are given two 4-bit numbers in signed 2's complement representation (A and B). Design a circuit to compare them and output (A>B), (A<B), and (A=B).

[12 marks]{CO-2}

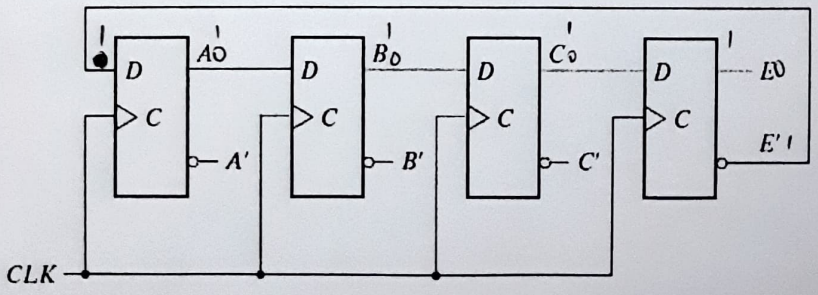
Q4. Perform the following conversions:

1) $(978)_{10} = (?)_{16}$
2) $(73)_8 + (5BC)_{16} = (57)_8 + (?)_{16}$
3) $(1011)_8 = (?)_{10}$
4) $(110)_2 \times (11011)_2 = (?)_{16}$
5) $(3.78)_{10} = (?)_2$

[2x5 = 10 marks]{CO-1}

Q5. What is the behaviour of the following circuit if clock pulses are applied from a reset state (when all FFs are at zero) [4]? Draw the complete state diagram for the 16 distinct states (including starting in any other state) [4]. In general, if there are *k* flip-flops in this chain and any arbitrary starting state is chosen, how many clock cycles does it take to make sure we return to the original state [4]?

[4+4+4 = 12 marks]{CO-3}



Q6. We are required to find the sum of a set of N numbers located in a block of memory starting from location "0x200". The number N itself is stored in location "0x220" (assume N<0x20). Write an assembly level program that computes this sum using our simple 8-bit microcontroller. (Concise instruction set is provided below). Assume your own code starts at memory location "0x000". Provide reasoning for your code.

[12 marks]{CO-4}

Instruction	Opcode	Clk	Control Signals	Select Signals
adi xx	01	3	E_{PC}, L_{MR}, I_{PC}	-
		4	RD, L_{OR}	-
		5	E_{AR}, L_{AR}, End	$S_{ALU} \leftarrow$ ADD
sbi xx	02	3	E_{PC}, L_{MR}, I_{PC}	-
		4	RD, L_{OR}	-
		5	E_{AR}, L_{AR}, End	$S_{ALU} \leftarrow$ SUB
xri xx	03	3	E_{PC}, L_{MR}, I_{PC}	-
		4	RD, L_{OR}	-
		5	E_{AR}, L_{AR}, End	$S_{ALU} \leftarrow$ XOR
ani xx	04	3	E_{PC}, L_{MR}, I_{PC}	-
		4	RD, L_{OR}	-
		5	E_{AR}, L_{AR}, End	$S_{ALU} \leftarrow$ AND
movs <R>	70-7F	3	E_{RG}, L_{AR}, End	$S_{RG} \leftarrow$ <R>, $S_{ALU} \leftarrow$ PASS0
movd <R>	80-8F	3	E_{AR}, L_{RG}, End	$S_{RG} \leftarrow$ <R>
movi <R> xx	90-9F	3	E_{PC}, L_{MR}, I_{PC}	-
		4	RD, L_{RG}, End	$S_{RG} \leftarrow$ <R>
stor <R>	A0-AF	3	E_{AR}, L_{MR}	-
		4	E_{RG}, WR, End	$S_{RG} \leftarrow$ <R>
load <R>	B0-BF	3	E_{AR}, L_{MR}	-
		4	RD, L_{RG}, End	$S_{RG} \leftarrow$ <R>
jumpd<FL> xx	E0-E7	3	E_{PC}, L_{MR}, I_{PC}, E_{FL}, End if <FL>'	$S_{FL} \leftarrow$ <FL>
		4	RD, L_{PC}, End	-
jmpr<FL>	E8-EF	3	E_{FL}, End if <FL>'	$S_{FL} \leftarrow$ <FL>
		4	E_{AR}, L_{PC}, End	-