VISHAK NARAYANAN

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Summary

- Embedded Computer systems architect with prior **1.8 years** of industrial experience in embedded hardware **PCB designing.**
- PhD candidate focused on developing HW-SW co-design systems to enable robust and reliable battery-free wireless sensor networks.
- Specialized in modelling and building complete, **end-to-end systems** with technical skills spanning from software through digital hardware to PCB prototypes.

Education

Iowa State University

Ph. D, Computer Engineering:

Jan 2021 – Present

SCMS School of Engineering and Technology (SSET)

Bachelor of Technology, B.Tech, Electronics and Communication Engineering (ECE)

Aug 2013 – May 2017

Honors and Awards

- Selected as lead organizer IBM Qiskit Fall 24 event, one among 50 best applicants over the world.
- Honored for service (twice) as a graduate student leader by Iowa State University.
- Multiple student travel grant awards (International Symposium on Microarchitecture (MICRO), Annual International Conference on Mobile Computing and Networking (MobiCom).

Experience

Intern – Engineer

Microchip

May 2023 – August 2023

- An intern with the Advanced Development FPGA R&D Team.
- Developed and characterized a time to delay counter system to detect voltage droop due to PDN resonance.

Computer Systems Graduate Research Assistant

Iowa State University

Jan 2021 - Present

- Proposed, developed and contributed to design and development of novel HW-SW systems, accepted by peer-reviewed premium conferences like ***RTSS, ISFPGA etc.,***
- Developed PAIL - a novel HW-SW approach to ensure robust coordination between batteryless wireless sensor networks.
- Proposed BOBBER, an **energy harvesting research platform** for low volume exploration of batteryless Intermittent accelerator architectures.
- Optimized BOBBER across different layers of the computing stack to **mitigate 10x performance overheads** to a **105x performance benefit** in continuous power.
- Investigated the idea of having a heterogenous microarchitecture to achieve **responsive, context-driven computing** for batteryless wireless sensor networks -- accepted as an NSF grant.

- Designed the hardware, proposed, and implemented a **sub 10% error**- hyper accurate voltage resilient robust clock using hierarchical multi-dimensional regression for energy harvesting timekeeping ***(RTSS 2020).***

Graduate Assistant

Iowa State University- Management Information Systems (MIS) department

Sep 2019 - Nov 2019 (3 months)

- Fostered a Python code to implement image recognition using Google Vision API to automate Airbnb property selection.

Hardware Design Engineer

iWave Systems

Sep 2017 - Jul 2019 (1 year 11 months)

- Gained a premium experience on end-to-end development of **RF**, **Digital** High-speed (Upto 16 Gbps) and **FPGA PCB hardware** designs: right from requirement analysis, power budgeting, schematic capture, interface testing of prototypes and documentation.
- Enhanced **yield by 20 %** by optimizing PCBA hardware layout, component selection and enclosure designs trading-off desired **power /performance requirements** and overall **cost** of the product.
- Experience in **PCB design** with RFFE, MIPI, ethernet, USB2/3/Type C, PCIE, SATA, I2C, UART, JTAG, SPI, HDMI 2.0, SFP+ interfaces.

Skills

- **Hardware EDA tools:** OrCAD, Allegro, EAGLE, Virtuoso, Innovus, Encounter, Libero SoC
- **Programming Language**: Python, C, VHDL, GCC assembly, RISC-V assembly,
- **Protocols**: USB 2.0, USB- C, SPI, UART, I^2C, SFP+,
- **Numerical and ML packages:** NumPy, TensorFlow, Keras, Scikit-learn.
- **Simulation and Compiler**: GNU Compiler Collection (GCC), TI C/C++ Compiler, ModelSim, gem5.
- **Equipment and other tools:** Oscilloscope, Signal generator, Network Analyzer (VNA).
- **Operating systems**: Linux, Windows.

Publications

- **Vishak Narayanan**. Back From the Dead- Towards Enabling Timely Computation and Communication. in Proceedings of the 2024 in *30th ACM/SIGDA International Conference on Mobile Computing and Networking (MobiCom'24)* – accepted as poster
- Wymore, Mathew L., Rohit Sahu, Thomas Ruminski, Vishal Deep, Morgan Ambourn, Gregory Ling, **Vishak Narayanan**, William Asiedu, Daji Qiao, and Henry Duwe. "Lure: A simulator for networks of batteryless intermittent nodes." *Performance Evaluation* (2024): 102440.
- Mahmoud Gshash, **Vishak Narayanan,** Henry Duwe, Nathan Neihart: RF Energy Harvester with Constant Off-Time Charger for Batteryless Devices in 2023 IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS 2023)
- **Vishak Narayanan**, Rohit Sahu, Jidong Sun, Henry Duwe: BOBBER: A Prototyping Platform for Batteryless Intermittent Accelerators in *Proceedings of the 2023 31st ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (ISFPGA 2023)*
- Vishal Deep, Mathew L. Wymore∗, Alexis A. Aurandt, **Vishak Narayanan**, Shen Fu, Henry Duwe, Daji Qiao: Experimental Study of Lifecycle Management Protocols for Batteryless Intermittent Communication, *In 2021 18th IEEE International Conference on Mobile AD-Hoc and Smart Systems (IEEE MASS 2021)*
- Vishal Deep, **Vishak Narayanan**, Mathew L. Wymore, Henry Duwe & Daji Qiao: HARC- A Heterogeneous and Redundant Array of Persistent Clock for Intermittent systems in *2020 IEEE 41st Real-Time Systems Symposium* (RTSS 2020)
- Mathew L. Wymore, Vishal Deep, **Vishak Narayanan**, Henry Duwe & Daji Qiao: LMP- Life-cycle Management protocol for Intermittent systems, In *2020 IEEE 37th International Performance Computing and Communications Conference (IPCCC 2020).*

Research Talks

- *Preliminary Oral Examination,* Department of Electrical and Computer Engineering, Iowa State University 2024
- *Departmental seminar,* Department of Electrical and Computer Engineering, Iowa State University 2024
  Towards Enabling Robust Communication and Computation in Batteryless Intermittently-powered Sensor Nodes
- Invited talk – *One topic Day:* Microchip Technologies Pvt Ltd, San Jose, California 2023
  Towards Enabling Robust Communication and Computation in Batteryless Intermittently-powered Sensor Nodes
- 31st ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (ISFPGA) 2023
  A Prototyping Platform for Batteryless Intermittent Accelerators

Leadership Skills

- President of Graduate Organization of Electrical and Computer Engineering (GO-ECpE).
- Awarded a student travel grant for the 2022 International Symposium on Microarchitecture (MICRO).
- Guided several senior design students, for projects ranked top 3 in the department.
- Managed and organized an inter college technical quiz WIZPRO attended by over 20 colleges.
- Junior volleyball team captain for a year-round and lead the team to runner up's in the state. Played at State and National level representing the school.