Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ECC503	Digital VLSI	03	--	--	03	--	--	03

Course Code	Course Name	Examination Scheme							
		Theory Marks				Exam Duration (Hrs.)	Term Work	Practical and Oral	Total
		Internal Assessment			End Sem. Exam.				
		Test1	Test2	Avg.					
ECC503	Digital VLSI	20	20	20	80	03	--	--	100

Course Pre-requisite:

ECC302 – Electronic Devices and Circuits
ECC303 – Digital System Design
ECC403 – Linear Integrated Circuits

Course Objectives:

1. To introduce process flow of VLSI Design.
2. To understand MOSFET operation from VLSI design perspective.
3. To learn VLSI design performance metric and various tradeoffs.
4. To design, implement and verify combinational and sequential logic circuits using various MOS design styles.
5. To provides an exposure to RTL design and programming

Course Outcomes:

After successful completion of the course student will be able to:

1. Know various tools and processes used in VLSI Design.
2. Explain working of various CMOS combinational and sequential circuits used in VLSI Design.
3. Derive expressions for performance parameters of basic building blocks like CMOS inverter.
4. Relate performance parameters with design parameters of VLSI circuits.
5. Select suitable circuit and design style for given application.
6. Design and realize various combinational and sequential circuits for given specifications.

Module No.	Unit No.	Topics	Hrs.
1.0		**Review of MOSFET operation and Fabrication**	**08**
	1.1	Overview of VLSI Design Flow, Review of MOSFET operation, MOSFET Capacitances, MOSFET scaling, Short channel effects	03
	1.2	Fabrication process flow of NMOS and CMOS, Lambda based design rules	03
	1.3	Novel MOSFET Architectures FinFET, GAA-FET, CNTFET	02
2.0		**Combinational CMOS Logic Circuits**	**06**
	2.1	CMOS inverter operation, Voltage Transfer characteristics (VTC), Noise Margins, Propagation Delay, Power Dissipation, Design of CMOS Inverter, Layout of CMOS Inverter	03
	2.2	Realization of CMOS NAND gate, NOR gate, Complex CMOS Logic Circuits, Layout of CMOS NAND, NOR and complex CMOS circuits	03
3.0		**MOS Design Logic Styles**	**09**
	3.1	Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Dynamic Logic, Domino Logic, NORA, Zipper, C^2MOS	04
	3.2	Setup time, Hold time, clocked CMOS SR Latch, CMOS JK Latch, MS –JK Flip Flop, Edge triggered D-Flip Flop and realization using design styles	03
	3.3	Realization of Shift Register, MUX, Decoder using above design styles ,1-bit full adder	02
4.0		**Semiconductor Memories**	**06**
	4.1	ROM array, 6T-SRAM (operation, design strategy, leakage currents, sense amplifier), layout of SRAM	03
	4.2	Operation of 1T and 3T DRAM Cell, NAND and NOR flash memory	03
5.0		**Data path and system design issues**	**06**
	5.1	Ripple carry adder, CLA adder, carry save adder, carry select adder, carry skip adder, Array Multiplier	04
	5.2	On chip clock generation and distribution, Interconnect delay model, interconnect scaling and crosstalk	02
6.0		**RTL Design**	**04**
	6.1	High Level state machines, RTL design process	02
	6.2	RTL design of Soda dispenser machine, FIR Filter	02
		Total	**39**

Text Books:

1. Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition, 2012.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.
3. Frank Vahid, "Digital Design with RTL design, VHDL and VERILOG", John Wiley and Sons Publisher 2011.

Reference Books:

1. Neil H. E. Weste, David Harris and Ayan Banerjee, —*CMOS VLSI Design: A Circuits and Systems Perspectivel*, Pearson Education, 3rd Edition.
2. John P. Uyemura, "*Introduction to VLSI Circuits and Systems*", Wiley, Student Edition, 2013.
3. R. Jacob Baker, "*CMOS Circuit Design, Layout and Simulation*", Wiley, 2nd Edition, 2013

NPTEL / Swayam Course:

1. https://nptel.ac.in/courses/117/101/117101058/
2. https://nptel.ac.in/courses/108/107/108107129/

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on completion of approximately 40% of the syllabus and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

Weightage to each of the modules in end-semester examination will be proportional to number of respective lecture hours mentioned in the curriculum.

1. Question paper will comprise of **total 06** questions, each carrying **20 marks**.
2. **Question No: 01** will be **compulsory** and based on entire syllabus wherein 4 to 5 sub-questions will be asked.
3. Remaining questions will be mixed in nature and randomly selected from all the modules.
4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
5. **Total 04 questions** need to be solved.