EXPERIMENT NO. 8

TITLE: VERIFY THE TRUTH TABLE OF RS, JK, T, AND D FLIP-FLOPS USING NAND AND NOR GATES.

OBJECTIVE:

To verify the truth table and timing diagram of RS, JK, T and D flip-flops by using NAND & NOR gates ICs and analyses the circuit of RS, JK, T and D flip-flops with the help of LEDs display.

APPARATUS REQUIRED:

- Switches
- Power supply
- Resistances
- LEDs
- IC 7400 NAND Gates, etc.

THEORY:

RS flip flop:

The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop actually has three inputs, SET, RESET and clock pulse.

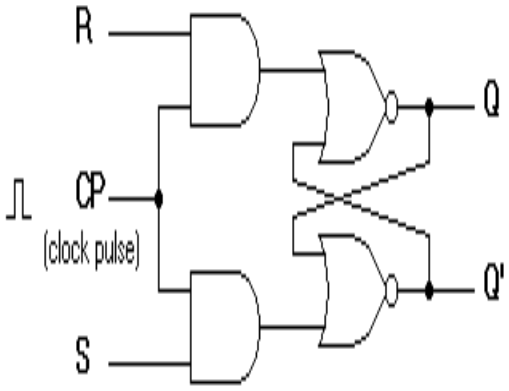


Fig: RS flip flop circuit diagram.

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

fig: Characteristics table of RS flip flop.

D flip flop :

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below.

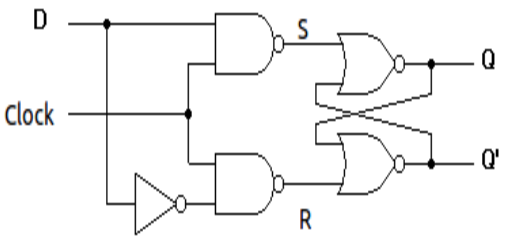


Fig: Circuit diagram D flip flop.

Input			Output	
D	reset	clock	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

Fig: Characteristics table of D flip flop.

J-K FLIP FLOP:

In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other as shown in characteristics table below.

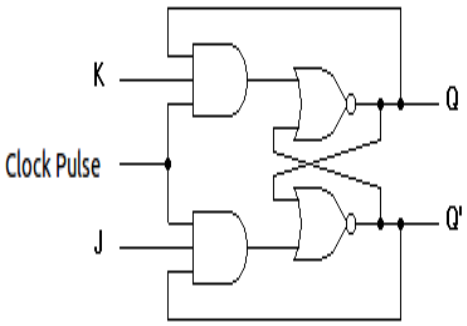


Fig: Circuit diagram J-K flip flop.

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	

Fig: Characteristics table of J-K flip flop.

T FLIP FLOP:

T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change as shown in table below.

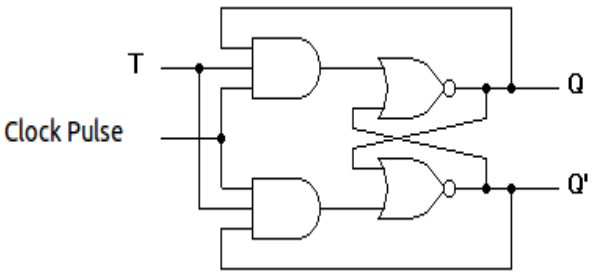


Fig: Circuit diagram T flip flop.

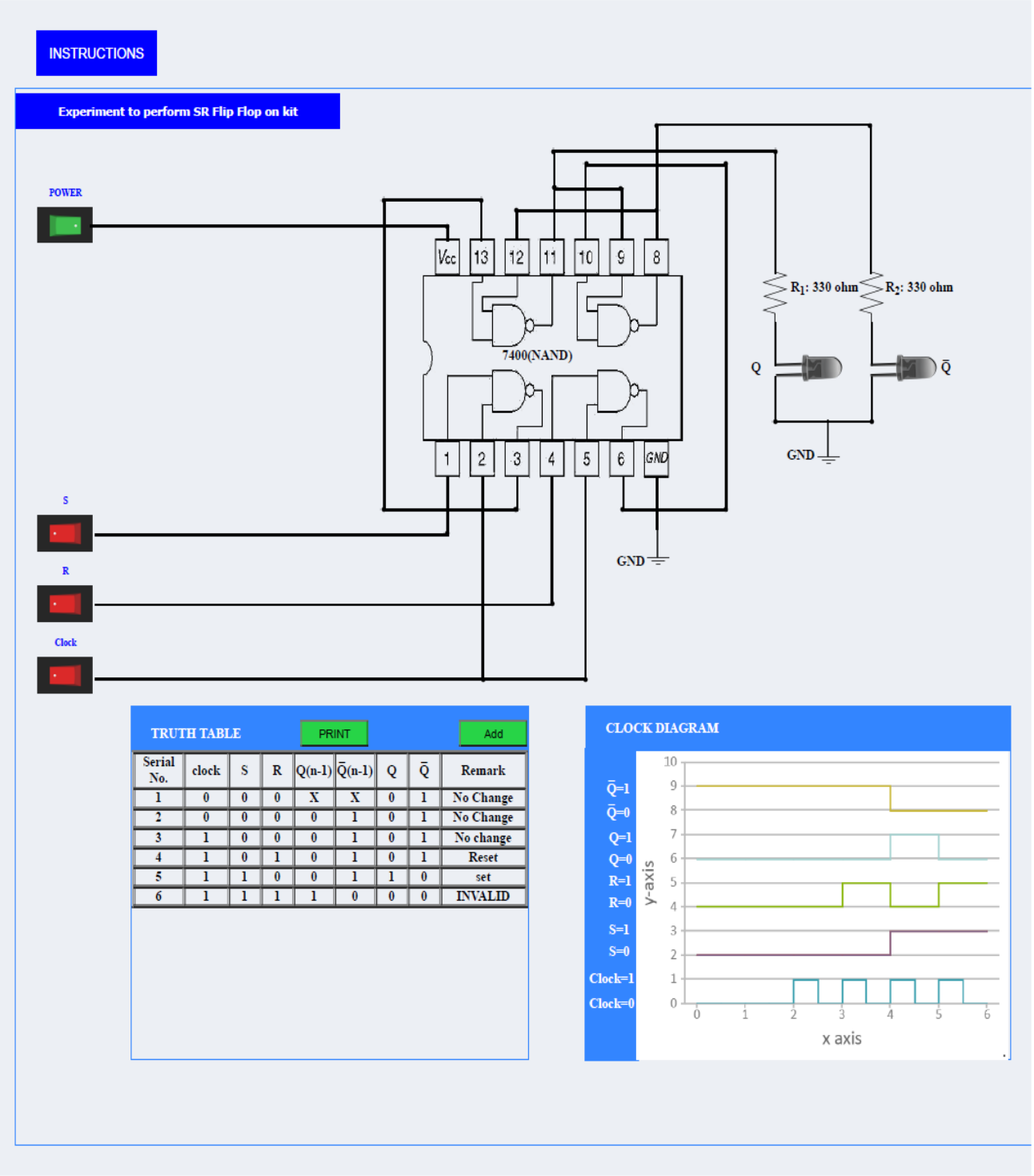
T flip-flop

T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
x	↓	Q	Q'

Fig: Characteristics table of T flip flop.

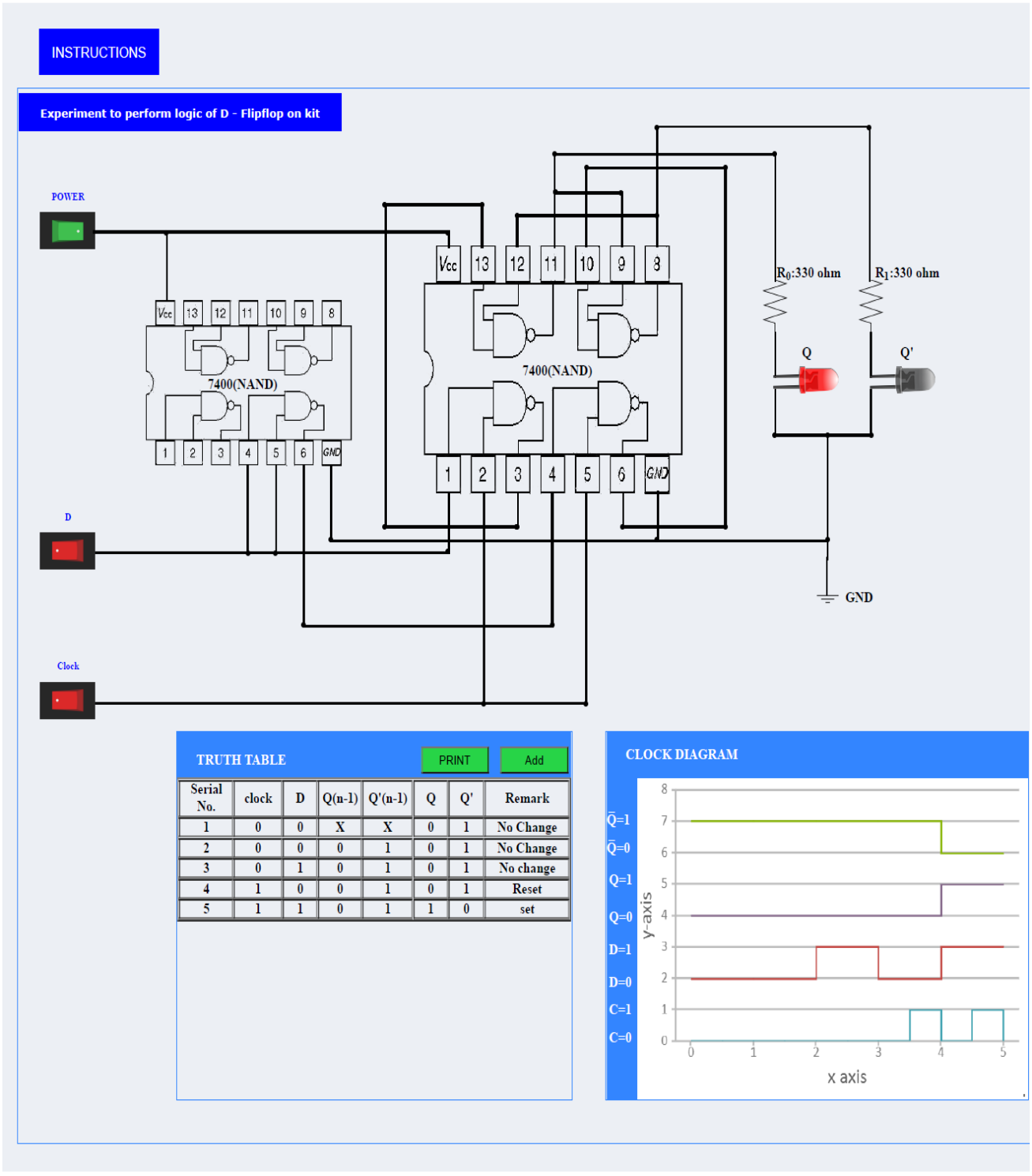
- **CIRCUIT DIAGRAM:**

SR FLIP FLOP:

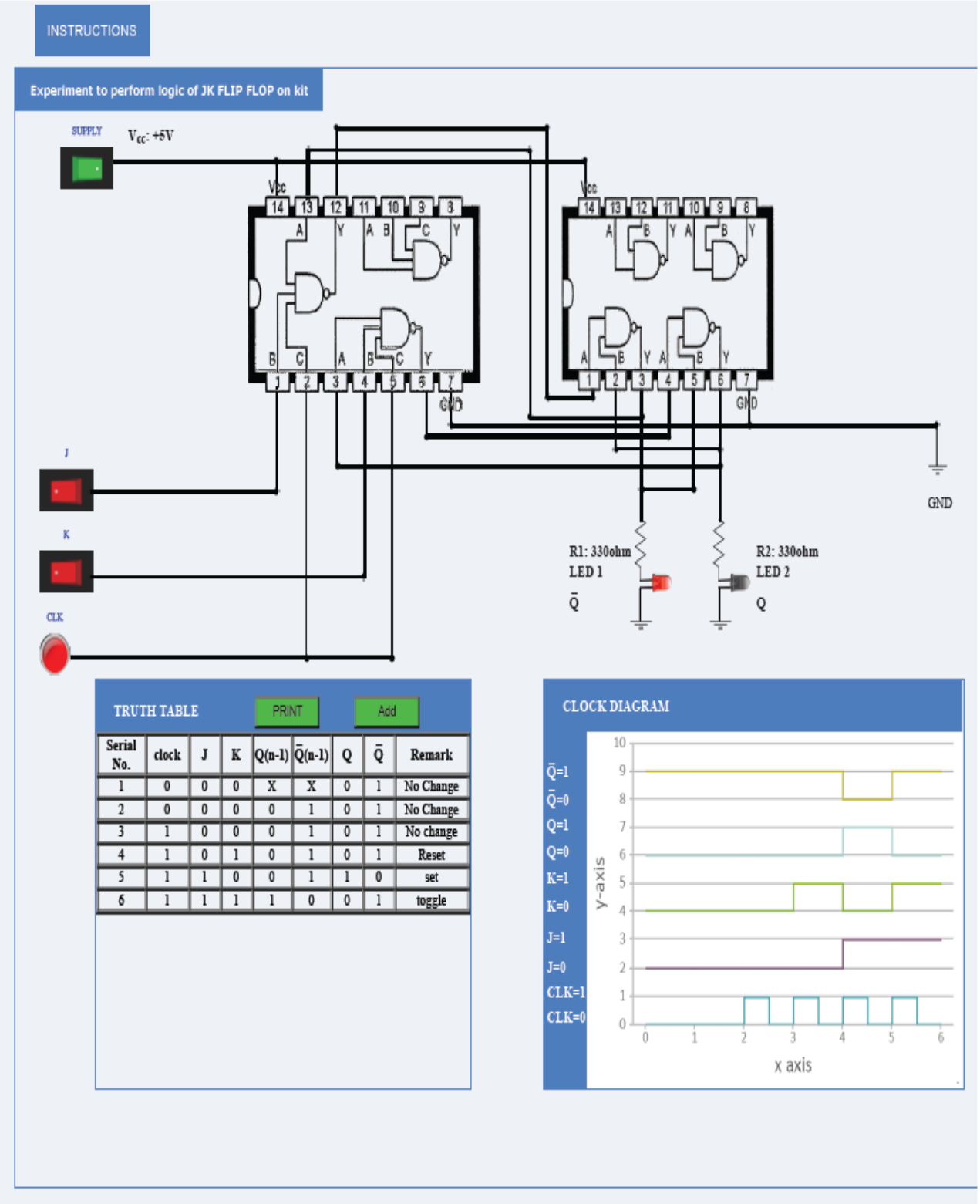


Serial No.	clock	S	R	Q(n-1)	Q̄(n-1)	Q	Q̄	Remark
1	0	0	0	X	X	0	1	No Change
2	0	0	0	0	1	0	1	No Change
3	1	0	0	0	1	0	1	No change
4	1	0	1	0	1	0	1	Reset
5	1	1	0	0	1	1	0	set
6	1	1	1	1	0	0	0	INVALID

D FLIP FLOP:


INSTRUCTIONS
Experiment to perform logic of D - Flipflop on kit
POWER
D
Clock
Vcc 13 12 11 10 9 8
7400(NAND)
1 2 3 4 5 6 GND
R0:330 ohm
R1:330 ohm
Q
Q'
GND
TRUTH TABLE
PRINT
Add
Serial No. | clock | D | Q(n-1) | Q'(n-1) | Q | Q' | Remark
1 | 0 | 0 | X | X | 0 | 1 | No Change
2 | 0 | 0 | 0 | 1 | 0 | 1 | No Change
3 | 0 | 1 | 0 | 1 | 0 | 1 | No change
4 | 1 | 0 | 0 | 1 | 0 | 1 | Reset
5 | 1 | 1 | 0 | 1 | 1 | 0 | set
CLOCK DIAGRAM
Q̄=1
Q̄=0
Q=1
Q=0
D=1
D=0
C=1
C=0
y-axis
x axis

J-K FLIP FLOP:

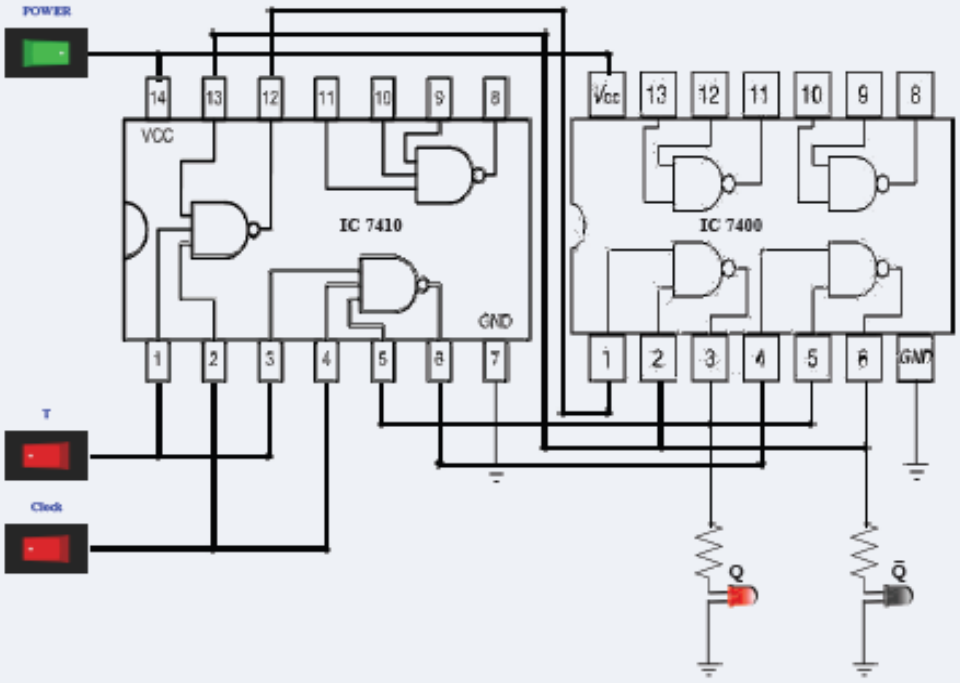


Serial No.	clock	J	K	Q(n-1)	$\bar{Q}$(n-1)	Q	$\bar{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	0	0	0	0	1	0	1	No Change
3	1	0	0	0	1	0	1	No change
4	1	0	1	0	1	0	1	Reset
5	1	1	0	0	1	1	0	set
6	1	1	1	1	0	0	1	toggle

T FLIP FLOP:

INSTRUCTIONS

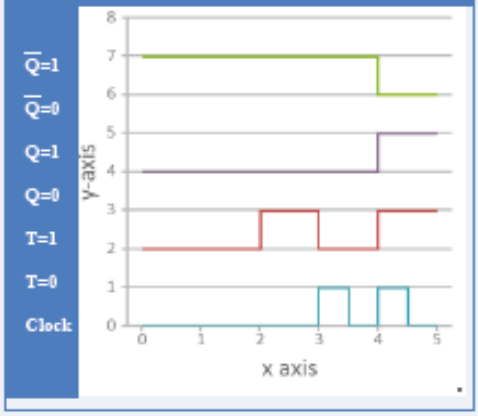
Experiment to perform T Flip Flop on kit



TRUTH TABLE Add Print

Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	0	0	0	1	0	1	No Change
3	0	1	0	1	0	1	No Change
4	1	0	0	1	0	1	No change
5	1	1	0	1	1	0	Toggle

TIMING DIAGRAM



- **CALCULATIONS:**

- Truth Table of SR Flip Flop:

- **TRUTH TABLE**

Serial No.	clock	S	R	Q(n-1)	$\bar{Q}$(n-1)	Q	$\bar{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	0	0	0	0	1	0	1	No Change
3	1	0	0	0	1	0	1	No change
4	1	0	1	0	1	0	1	Reset
5	1	1	0	0	1	1	0	set
6	1	1	1	1	0	0	0	INVALID

- Truth Table of D Flip Flop:

- **TRUTH TABLE**

Serial No.	clock	D	Q(n-1)	Q'(n-1)	Q	Q'	Remark
1	0	0	X	X	0	1	No Change
2	0	0	0	1	0	1	No Change
3	0	1	0	1	0	1	No change
4	1	0	0	1	0	1	Reset
5	1	1	0	1	1	0	set

- ## Truth Table of J-K Flip Flop:

- **TRUTH TABLE**

Serial No.	clock	J	K	Q(n-1)	$\bar{Q}$(n-1)	Q	$\bar{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	0	0	0	0	1	0	1	No Change
3	1	0	0	0	1	0	1	No change
4	1	0	1	0	1	0	1	Reset
5	1	1	0	0	1	1	0	set
6	1	1	1	1	0	0	1	toggle

- ## Truth Table of T Flip Flop:

- **TRUTH TABLE**

Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	0	0	0	1	0	1	No Change
3	0	1	0	1	0	1	No Change
4	1	0	0	1	0	1	No change
5	1	1	0	1	1	0	Toggle

- **RESULTS:**

- Verified the Truth Table of SR FLIP FLOP.
- Verified the Truth Table of D FLIP FLOP.
- Verified the Truth Table of J-K FLIP FLOP.
- Verified the Truth Table of T FLIP FLOP.

- **PRECAUTIONS:**

• All the connections should be made properly as per the circuit diagram.

• Connections should be tight and easy to inspect.

- Power supply should be 5v.

• Keep the switch turned off while making connections.