EXPERIMENT NO. 9

TITLE: DESIGN AND VERIFY THE 4-BIT SYNCHRONOUS / ASYBCHRONOUS COUNTER USING JK FLIP FLOP.

- **OBJECTIVE:**

To verify the truth table and timing diagram of 4-bit synchronous parallel counter and 4-bit asynchronous parallel counter by using JK flip flop ICs and analyses the circuit of 4-bit synchronous parallel counter and 4-bit asynchronous parallel counter with the help of LEDs display.

- **APPARATUS REQUIRED:**

• Switches
• Power supply
• Resistances
• LEDs
• IC 7476 etc.

- **THEORY:**

- ASYNCHRONOUS COUNTER:

  In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following counters is driven by output of previous flip flops. We can understand it by following diagram-

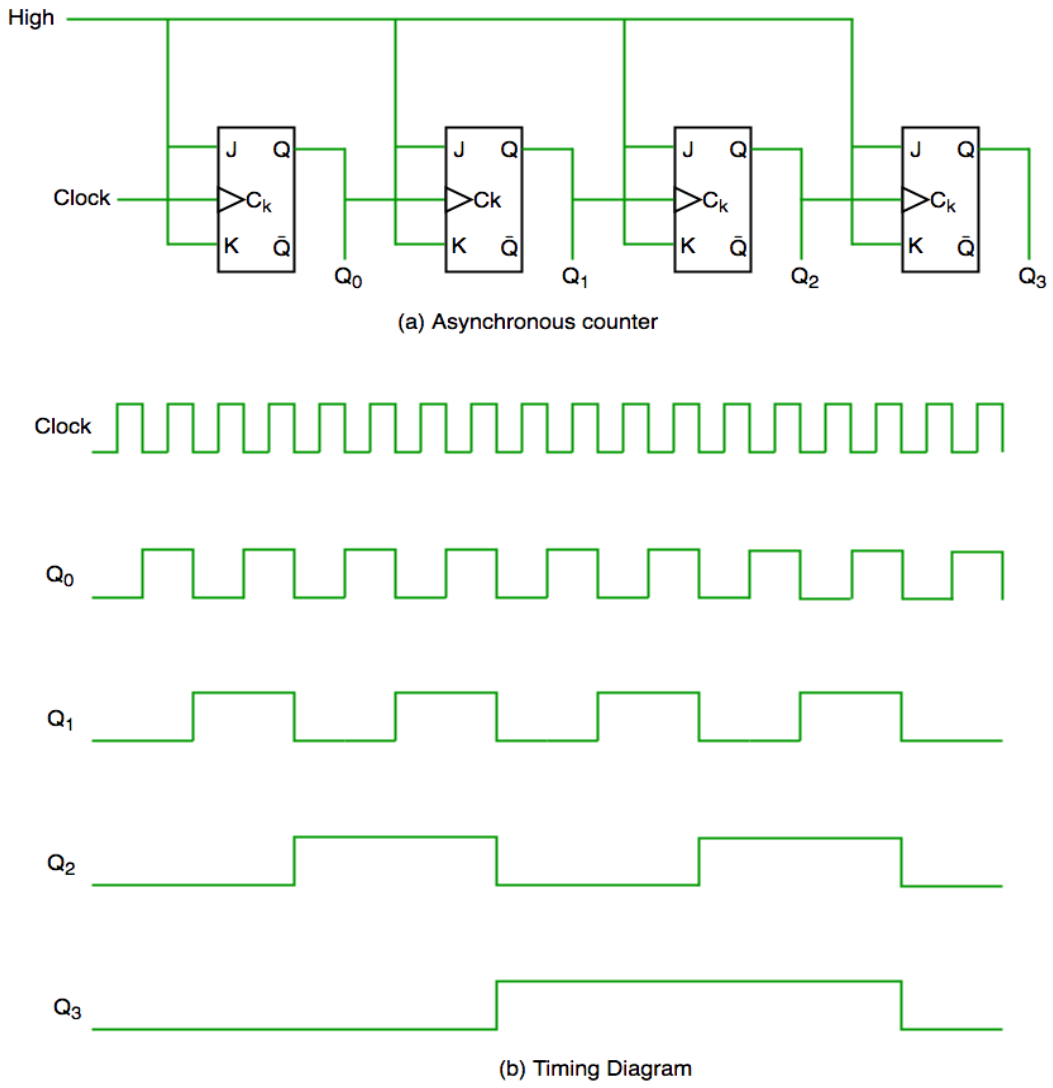


Figure-1: Asynchronous Counter Circuit and Timing Diagram

- SYNCHRONOUS COUNTER:

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.

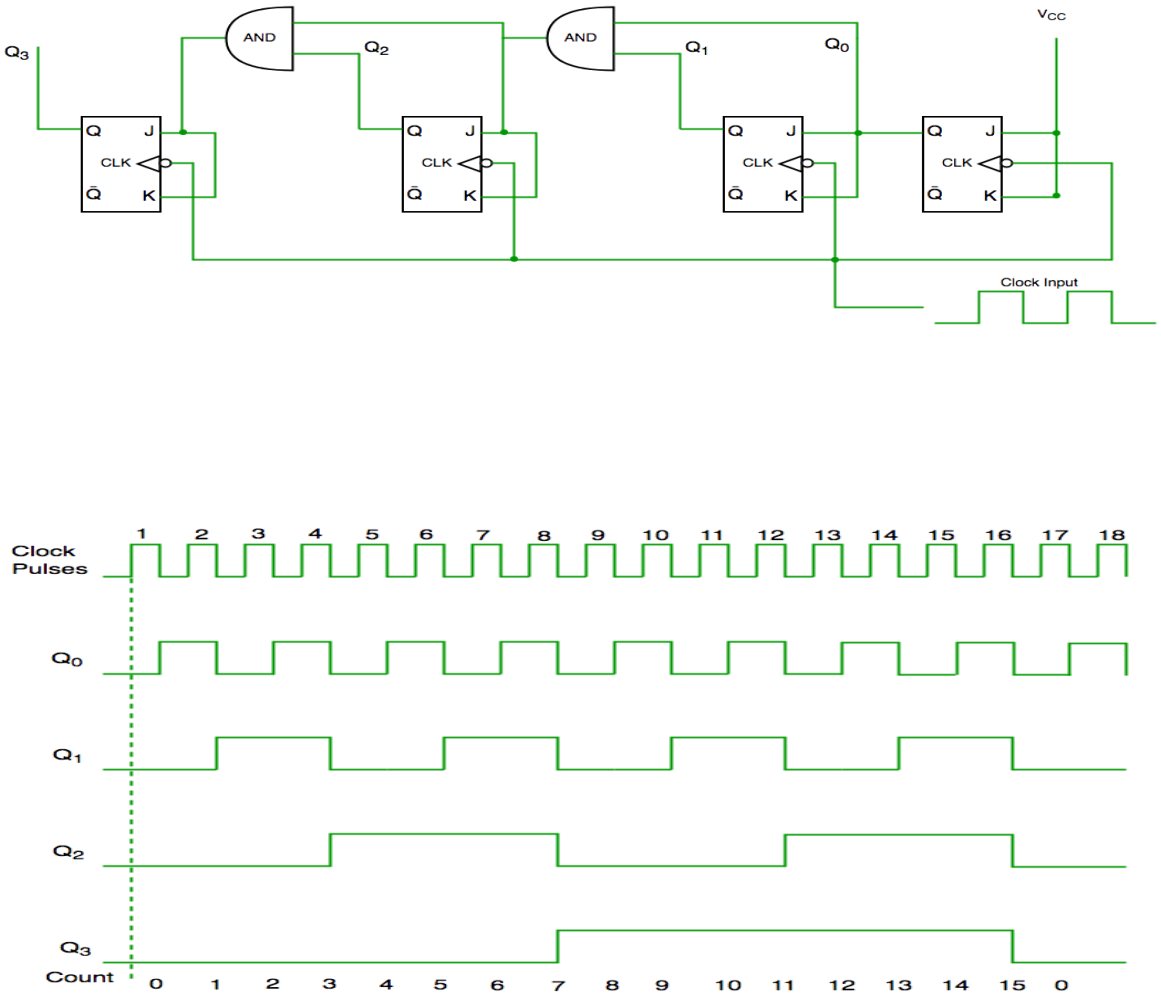
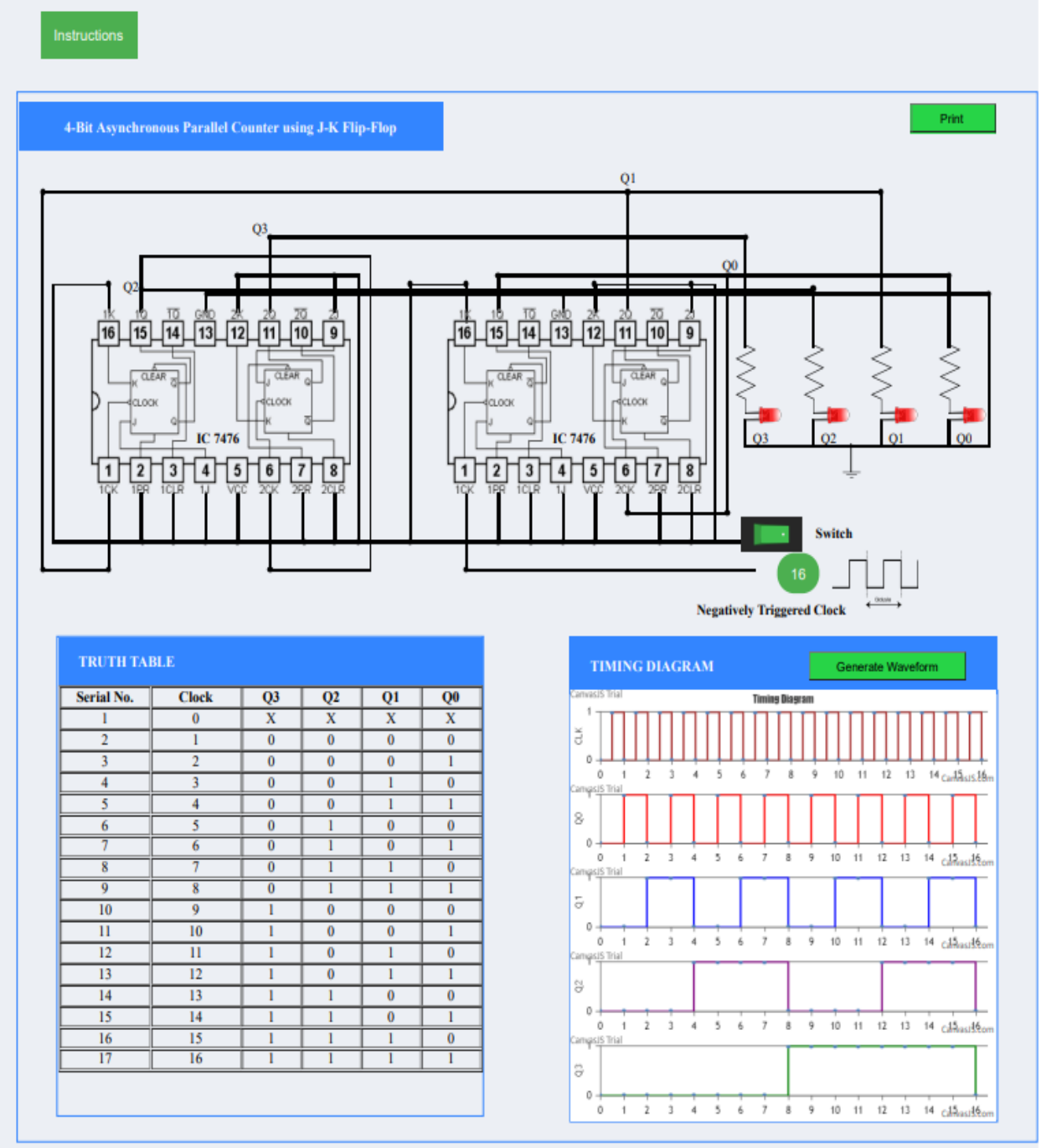


Figure-2: Synchronous Counter Circuit and Timing Diagram

- **CIRCUIT DIAGRAM:**

- **ASYNCHRONOUS COUNTER:**



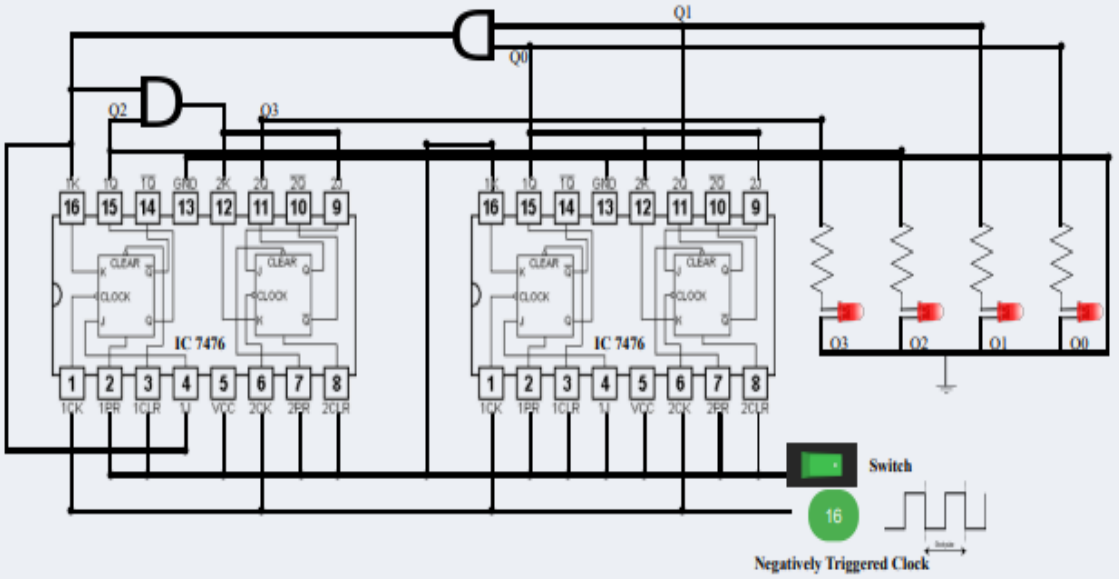
Serial No.	Clock	Q3	Q2	Q1	Q0
1	0	X	X	X	X
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

- **SYNCHRONOUS COUNTER:**

Instructions

4-Bit Synchronous Parallel Counter using J-K Flip-Flop

Print

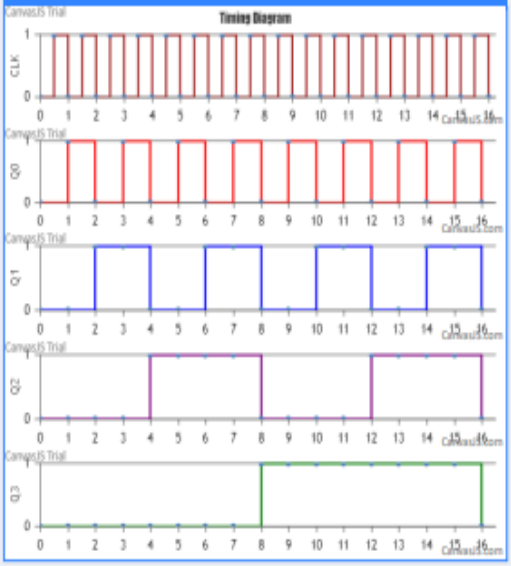


TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	0	X	X	X	X
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

TIMING DIAGRAM

Generate Waveform

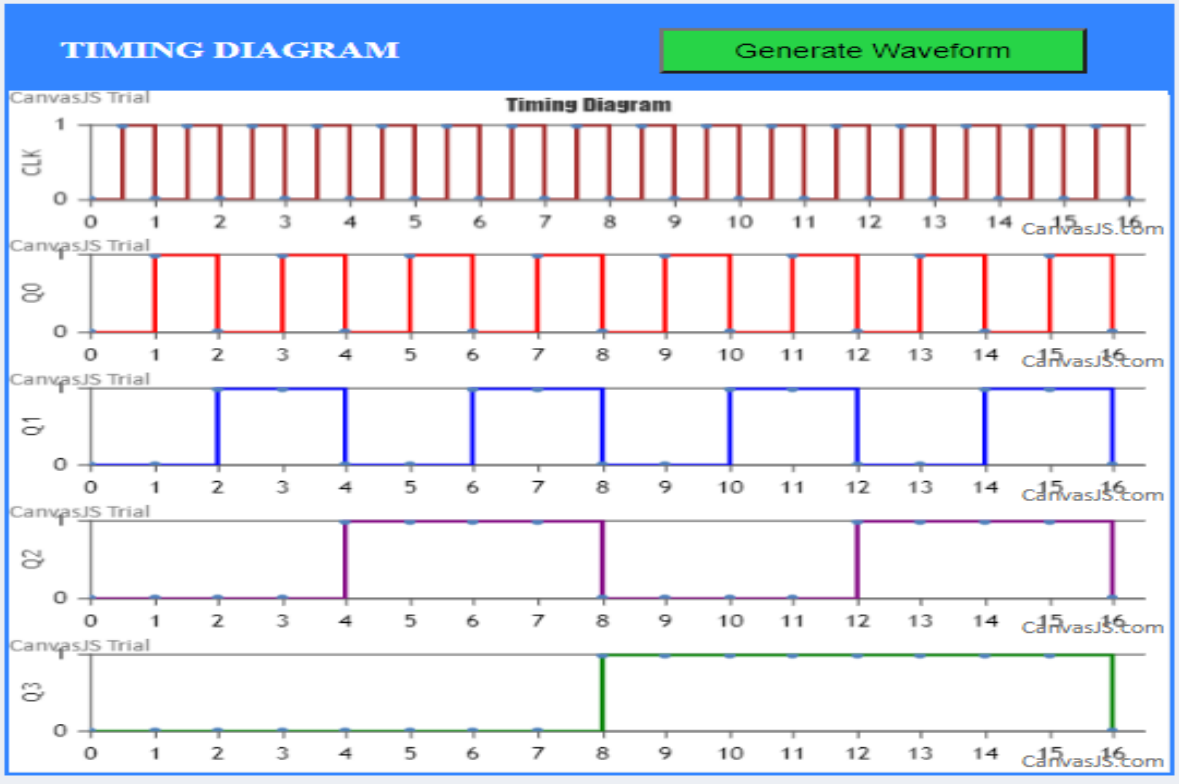


- **CALCULATIONS:**
- ASYNCHRONOUS COUNTER:

TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	0	X	X	X	X
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

TIMING DIAGRAM

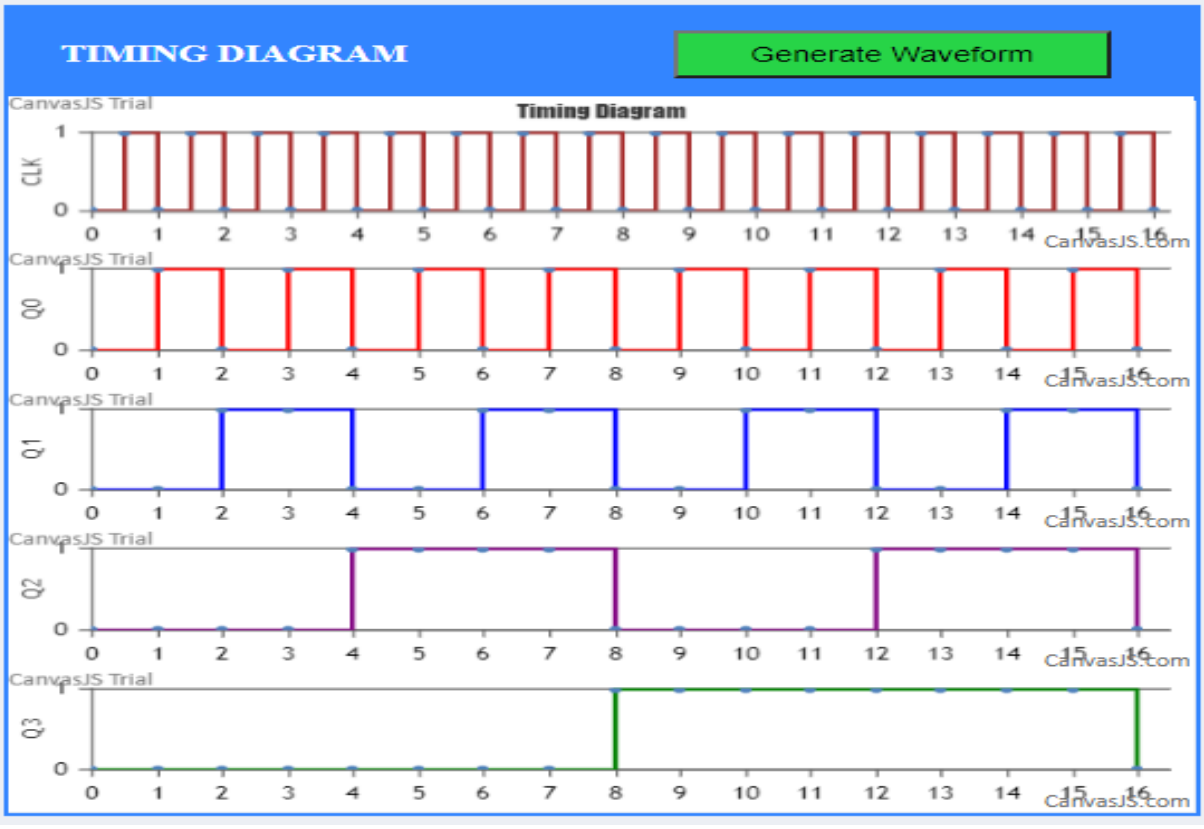


- SYNCHRONOUS COUNTER:

TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	0	X	X	X	X
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

TIMING DIAGRAM



RESULTS:

- Verified the truth table and timing diagram of 4-bit asynchronous parallel counter.
- Verified the truth table and timing diagram of 4-bit synchronous parallel counter.

PRECAUTIONS:

- All the connections should be made properly as per the circuit diagram.
- Connections should be tight and easy to inspect.
- Power supply should be 5v.
- Keep the switch turned off while making connections.