EXPERIMENT NO. 10

TITLE: DESIGN AND VERIFY THE 4-BIT SERIAL IN PARALLEL OUT SHIFT REGISTERS.

- **OBJECTIVE:**

To analyses the circuit and truth table of 4-bit SIPO (serial input parallel output) shift register by IC 7474 (D flip flop).

- **APPARATUS REQUIRED:**

• Switches
• Power supply
• Resistances
• LEDs
• IC 7474(D flip flop) etc.

- **THEORY:**

In Serial In Parallel Out (SIPO) shift registers, the data is stored into the register serially while it is retrieved from it

in parallel-fashion. Figure 1 shows an n-bit synchronous SIPO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D1 of FF1). It is also seen that the inputs of all other flip-flops (except the first flip-flop FF1) are driven by the outputs of the preceding ones like the input of FF2 is driven by the output of FF1. In this kind of shift register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q1 to Qn).

Table I Data Movement in Right-Shift SIPO Shift Register

Clock Cycle	Data in	Q_1	Q_2	...	Q_n
1	B_1	B_1	0	...	0
2	B_2	B_2	B_1	...	0
3	B_3	B_3	B_2	...	0
4	B_4	B_4	B_3	...	0
5	B_5	B_5	B_4	...	0
6	B_6	B_6	B_5	...	0
.	.	.	.	...	.
.	.	.	.	...	.
.	.	.	.	...	.
n	B_n	B_n	B_{n-1}	...	B_1

Output of SIPO (right-shift) Shift Register

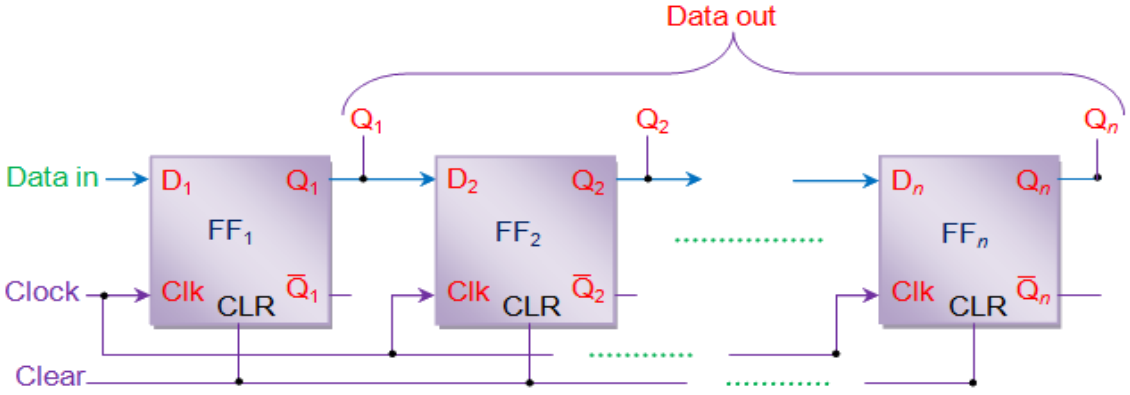


Figure 1 *n*-bit Serial-In Parallel-Out Right-Shift Shift Register

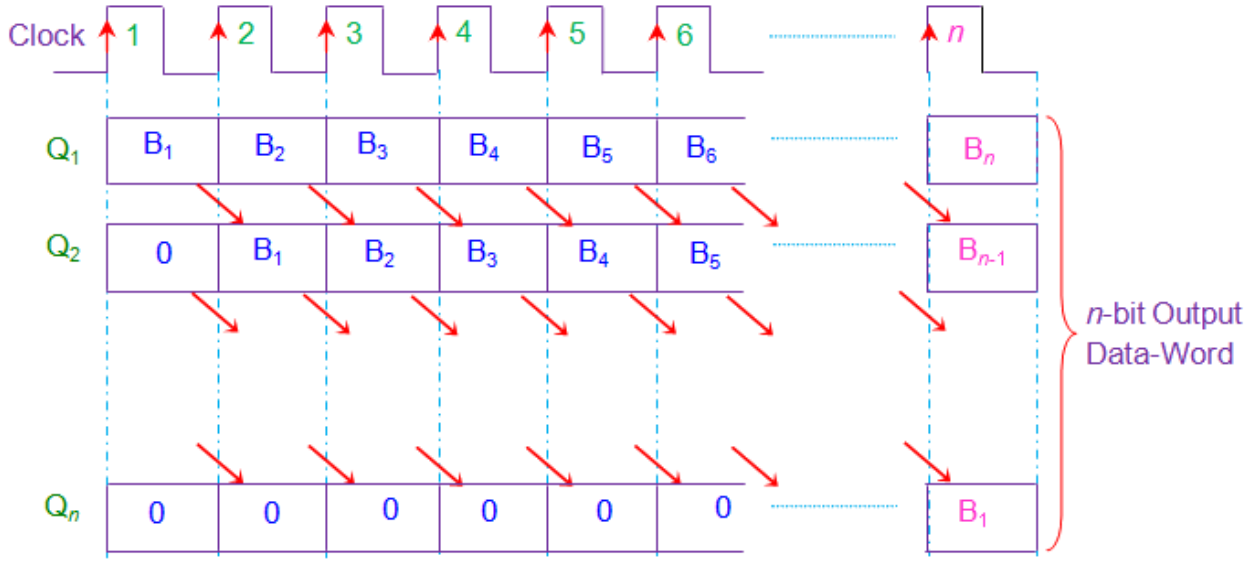


Figure 2 Output Waveform of *n*-bit Right-Shift SIPO Shift Register

In the right-shift SIPO shift-register, data bits shift from left to right for each clock pulse. However if the data bits are made to shift from right to left in the same design, one gets a left-shift SIPO shift-register as shown by figure 3. Nevertheless the basic working principle remains the same except the fact that now Bn down to B1 is stored in Qn down to Q1 i.e. Q1 = B1, Q2 = B2 … Qn = Bn at the nth clock pulse

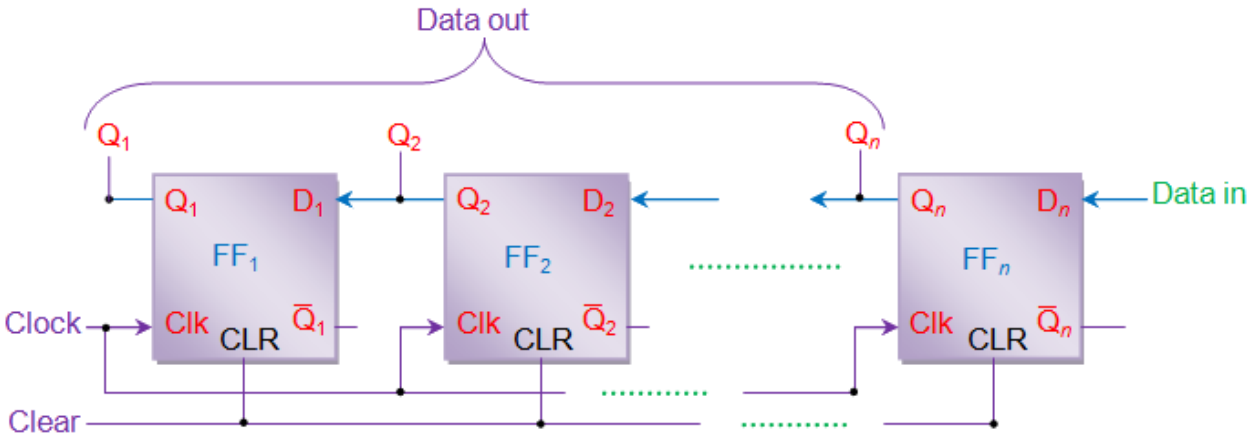
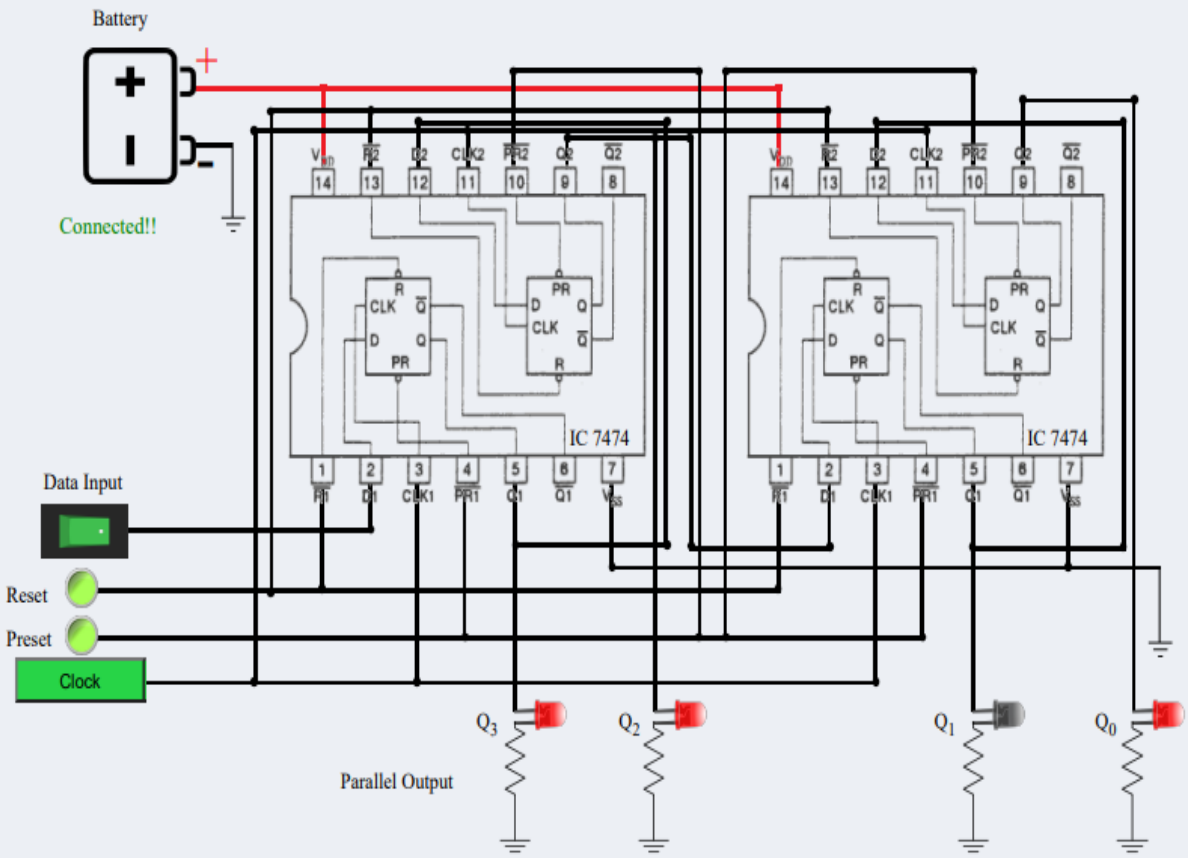


Figure 3 *n*-bit Serial-In Parallel-Out Left-Shift Shift Register

- **CIRCUIT DIAGRAM:**

Design and verification of 4-Bit Serial In Parallel Out Shift Register



Add Print

TRUTH TABLE

Serial No.	Clock	Data Input	Q_3	Q_2	Q_1	Q_0
1	1	1	1	0	0	0
2	2	0	0	1	0	0
3	3	1	1	0	1	0
4	4	1	1	1	0	1

▪ CALCULATIONS:

▪ TRUTH TABLE

Serial No.	Clock	Data Input	Q_3	Q_2	Q_1	Q_0
1	1	1	1	0	0	0
2	2	0	0	1	0	0
3	3	1	1	0	1	0
4	4	1	1	1	0	1

▪ RESULTS:

- Verified the truth table of 4-bit SIPO (serial input parallel output) shift register by IC 7474 (D flip flop).

▪ PRECAUTIONS:

- All the connections should be made properly as per the circuit diagram.
- Connections should be tight and easy to inspect.
- Power supply should be 5v.
- Keep the switch turned off while making connections.