**Computer Architecture (COL 216)**

# II Semester 2019-2020

**Assignment 11: Floating Point Addition**

**Submission Deadline: 19 August 2020, 11:59 PM**

**INDIVIDUAL (not group) ASSIGNMENT**

[Substitute for Minor 2 examination]

You will be awarded marks according to your design and the test cases you developed to evaluate the design. Extensive testing is expected as a part of the Assignment

In this assignment you will do a software implementation of the Floating Point Adder whose algorithm was covered in class, and is outlined in Figure 3.14 (Page 205 of the textbook). Assume that each of the boxes numbered 1, 2, 3, and 4 require one clock cycle, and the condition checks require zero time.

**Inputs** to the program will be:

1. A text file with each line containing a pair of floating point numbers to be added, in binary representation (a string of '0' and '1' characters in the file). See sample below.

**Outputs** from the program will be:

1. A sequence of addition results, each line containing one result (a string of '0' and '1' characters) and the number of clock cycles required for performing the addition.

**Deliverables**:

1. Software implementation of the floating point adder referred to above.
2. Test files used to verify your program. Remember to test for special cases such as Overflow, Underflow, Normalised result, etc.
3. A document explaining the different test cases.

**Sample Input File (each line contains the representation for 2 floating point numbers, both 32 bits wide)**:

11001100110011001111110011001100 11001100110011001111110011001100
01001110110011001111110011001101 11001100110111001101110011001110

**Sample Output File (just examples. These are not be the computed outputs for the above input file)**:

11001110110011001111110011001101
01001110110011001111110011001101