CoolRunner XPLA3 CPLD

DS012 (v2.5) May 26, 2009 **Product Specification**

Features

- Fast Zero Power (FZP) design technique provides ultra-low power and very high speed
  - Typical Standby Current of 17 to 18 µA at 25°C
- Innovative CoolRunner™ XPLA3 architecture combines high speed with extreme flexibility
- Based on industry's first TotalCMOS PLD — both CMOS design and process technologies
- Advanced 0.35µ five layer metal EEPROM process
  - 1,000 erase/program cycles guaranteed
  - 20 years data retention guaranteed
- 3V, In-System Programmable (ISP) using JTAG IEEE 1149.1 interface
  - Full Boundary-Scan Test (IEEE 1149.1)
  - Fast programming times
- Support for complex asynchronous clocking
  - 16 product term clocks and four local control term clocks per function block
  - Four global clocks and one universal control term clock per device
- Excellent pin retention during design changes
- Available in commercial grade and extended voltage (2.7V to 3.6V) industrial grade
- 5V tolerant I/O pins
- Input register setup time of 2.5 ns
- Single pass logic expandable to 48 product terms
- High-speed pin-to-pin delays of 5.0 ns
- Slew rate control per output
- 100% routable
- Security bit prevents unauthorized access
- Supports hot-plugging capability
- Design entry/verification using Xilinx or industry standard CAE tools
- Innovative Control Term structure provides:
  - Asynchronous macrocell clocking
  - Asynchronous macrocell register preset/reset
  - Clock enable control per macrocell
- Four output enable controls per function block
- Foldback NAND for synthesis optimization
- Universal 3-state which facilitates "bed of nails" testing
- Available in Chip-scale BGA, Fineline BGA, and QFP packages. Pb-free available for most package types. See **Xilinx Packaging** for more information.

Table 1: **CoolRunner XPLA3 Device Family**

	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL	XCR3512XL
Macrocells	32	64	128	256	384	512
Usable Gates	750	1,500	3,000	6,000	9,000	12,000
Registers	32	64	128	256	384	512
T_{PD} (ns)	4.5	5.5	5.5	7.0	7.0	7.0
T_{SU} (ns)	3.0	3.5	3.5	4.3	4.3	3.8
T_{CO} (ns)	3.5	4	4	4.5	4.5	5.0
F_{system} (MHz)	213	192	175	154	135	135
I_{CCSB} (µA)	17	17	17	18	18	18

Table 2: **CoolRunner XPLA3 Packages and User I/O Pins**

	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL	XCR3512XL
44-pin VQFP	36	36	-	-	-	-
48-pin 0.8mm CSP	36	40	-	-	-	-
56-pin 0.5mm CSP	-	48	-	-	-	-
100-pin VQFP	-	68	84	-	-	-
144-pin 0.8mm CSP	-	-	108	-	-	-
144-pin TQFP	-	-	108	120	118(1)	-
208-pin PQFP	-	-	-	164	172	180
256-pin Fineline BGA	-	-	-	164	212	212
280-pin 0.8mm CSP	-	-	-	164	-	-
324-pin Fineline BGA	-	-	-	-	220	260

1. XCR3384XL TQ144 JTAG pins are not compatible with other members of the CoolRunner XPLA3 family in the TQ144 package.
2. Most packages are available in Pb-Free option. See individual data sheets for more details.
3. The 44-pin PLCC package is discontinued per XCN07022.

Family Overview

The CoolRunner XPLA3 (eXtended Programmable Logic Array) family of CPLDs is targeted for low power systems that include portable, handheld, and power sensitive applications. Each member of the CoolRunner XPLA3 family includes Fast Zero Power (FZP) design technology that combines low power and high speed. With this design technique, the CoolRunner XPLA3 family offers true pin-to-pin speeds of 5.0 ns, while simultaneously delivering power that is less than 56 µW at standby without the need for "turbo bits" or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any other CPLD. CoolRunner devices are the only TotalCMOS PLDs, as they use both a CMOS process technology and the patented full CMOS FZP design technique. The FZP design technique combines fast nonvolatile memory cells with ultra-low power SRAM shadow memory to deliver the industry's lowest power 3.3V CPLD family.

The CoolRunner XPLA3 family employs a full PLA structure for logic allocation within a function block. The PLA provides maximum flexibility and logic density, with superior pin locking capability, while maintaining deterministic timing.

CoolRunner XPLA3 CPLDs are supported by Xilinx® WebPACK™ software and industry standard CAE tools (Mentor, Cadence/OrCAD, Exemplar Logic, Synopsys, Viewlogic, and Synplicity), using HDL editors with ABEL, VHDL, and Verilog, and/or schematic capture design entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on multiple personal computer (PC), Sun, and HP platforms.

The CoolRunner XPLA3 family features also include the industry-standard, IEEE 1149.1, JTAG interface through which boundary-scan testing, In-System Programming (ISP), and reprogramming of the device can occur. The CoolRunner XPLA3 CPLD is electrically reprogrammable using industry standard device programmers.

CoolRunner XPLA3 Architecture

Figure 1 shows a high-level block diagram of a 128 macrocell device implementing the CoolRunner XPLA3 architecture. The CoolRunner XPLA3 architecture consists of function blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each function block has 40 inputs from the ZIA and contains 16 macrocells.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner XPLA3 family unique is logic allocation inside each function block, and the design technique used to implement product terms.

Function Block Architecture

Figure 3 illustrates the function block architecture. Each function block contains a PLA array that generates control terms, clock terms, and logic cells. A PLA differs from a PAL in that the PLA has a fully programmable AND array followed by a fully programmable OR array. A PAL array has a fixed OR array, limiting flexibility. Refer to Figure 2 for an example of a PAL and a PLA array. The PLA array receives its inputs directly from the ZIA. There are 40 pairs of true and complement inputs from the ZIA that feed the 48 product terms in the array. Within the 48 P-terms there are eight local control terms (LCT[0:7]) available as control signals to each macrocell for use as asynchronous clocks, resets, presets and output enables. If not needed as control terms, these P-Terms can join the other 40 P-Terms as additional logic resources.

In each function block there are eight foldback NAND product terms that can be used to synthesize increased logic density in support of wider logic equations. This feature can be disabled in software by the user. As with unused control P-Terms, unused foldback NAND P-Terms can be used as additional logic resources.

Sixteen high-speed P-Terms are available at each macrocell for speed critical logic. If wider than a single P-Term logic is required at a macrocell, 47 additional P-Terms can be summed in prior to the VFM (Variable Function Multiplexer). The VFM increases logic optimization by implementing some two input logic functions before entering the macrocell (see Figure 4).

Each macrocell can support combinatorial or registered logic. The macrocell register accommodates asynchronous presets and resets, and "power on" initial state. A hardware clock enable is also provided for either D or T type registers, and the register clock input is used as a latch enable when the macrocell register is configured as a latch function.

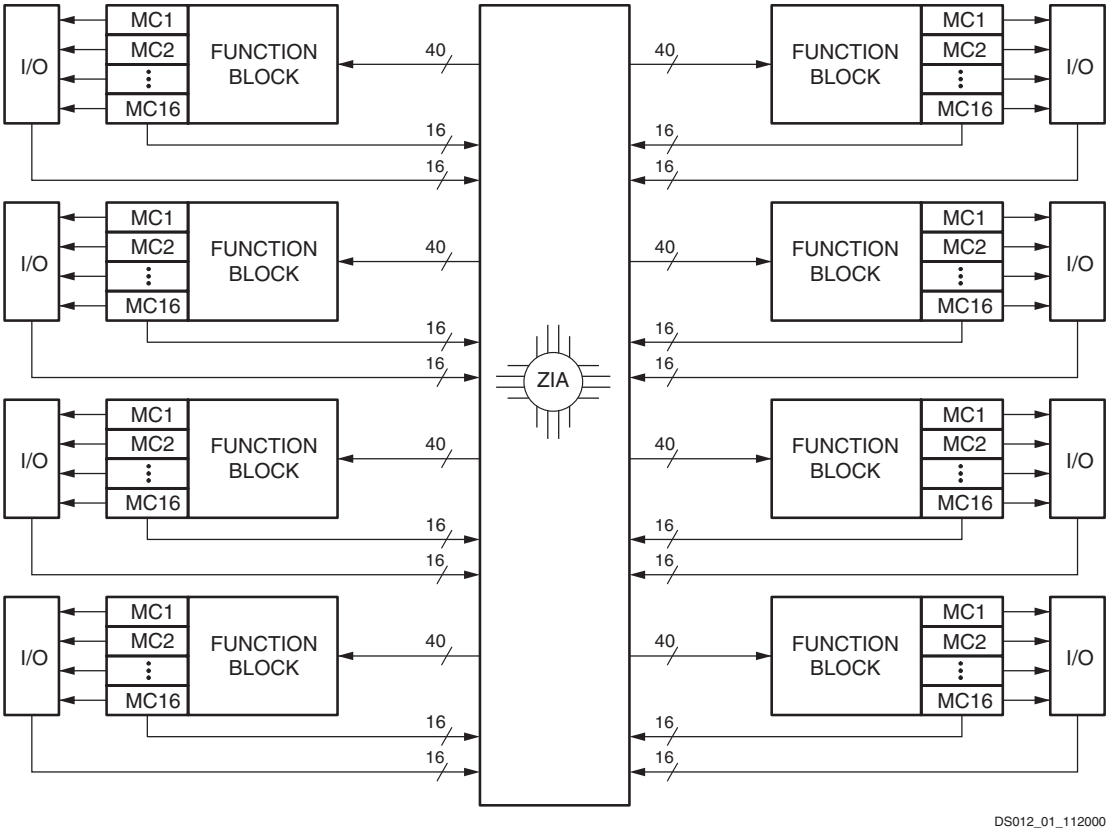


Figure 1: **Xilinx XPLA3 CPLD Architecture**

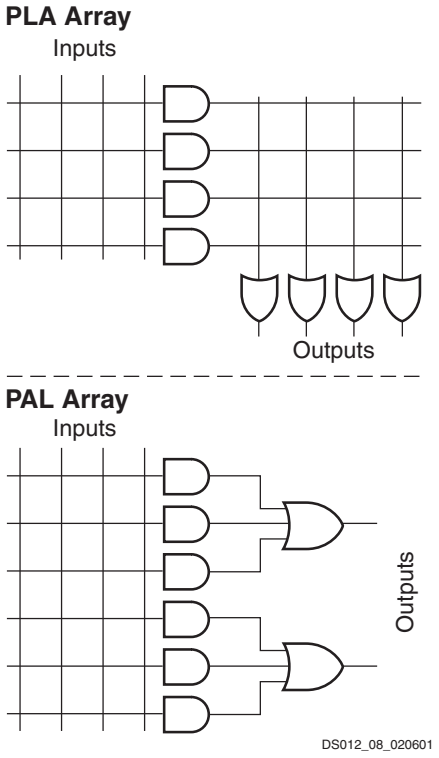


Figure 2: **PLA and PAL Array Example**

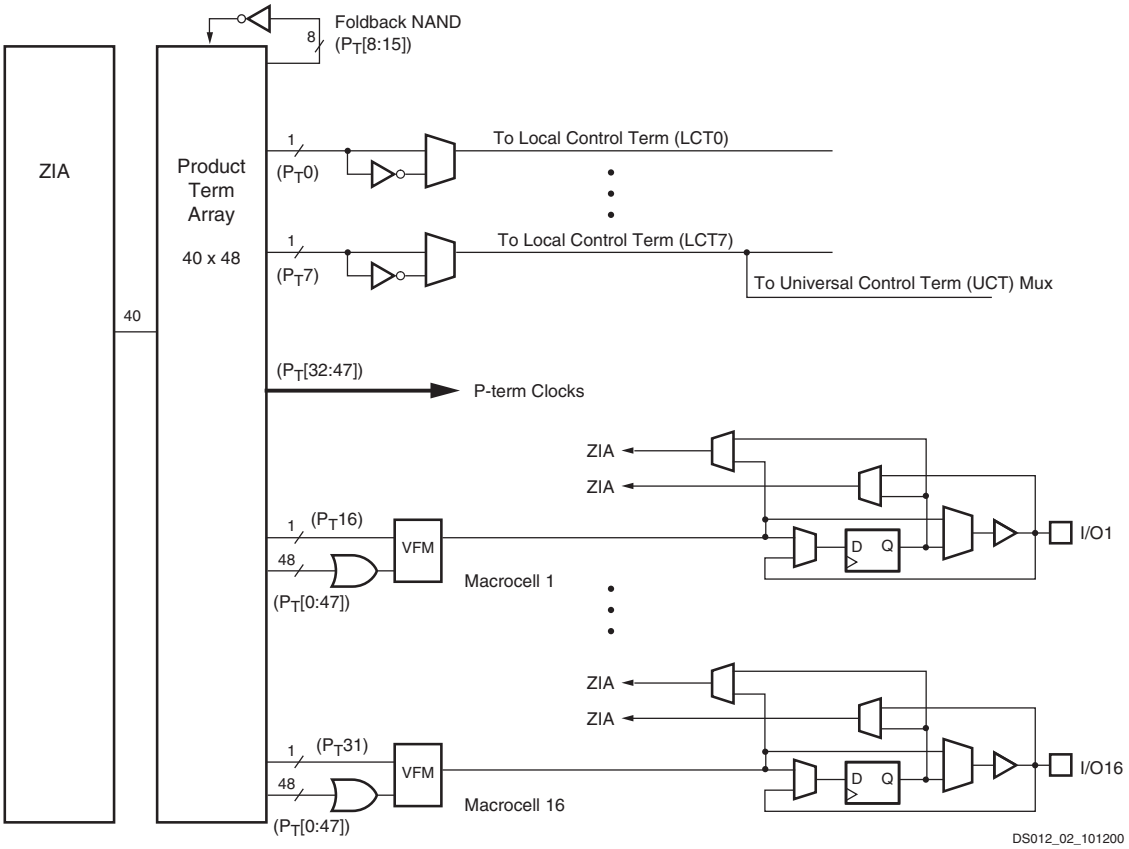


Figure 3: **Xilinx CoolRunner XPLA3 Function Block Architecture**

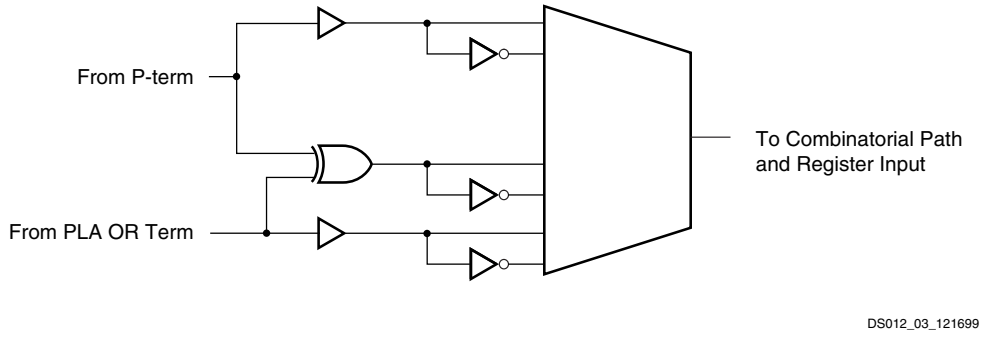


Figure 4: **Variable Function Multiplexer**

Macrocell Architecture

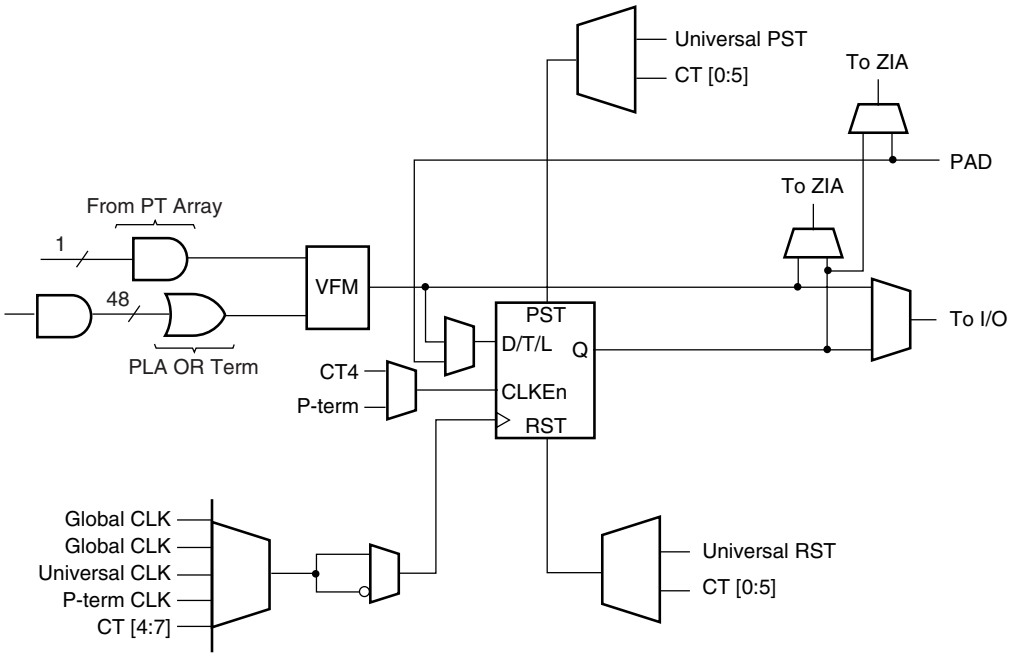
Figure 5 shows the architecture of the macrocell used in the CoolRunner XPLA3 CPLD. Any macrocell can be reset or preset on power-up. Each macrocell register can be configured as a D-, T-, or Latch-type flip-flop, or bypassed if the macrocell is required as a combinatorial logic function.

Each of these flip-flops can be clocked from any one of eight sources or their complements. There are two global synchronous clocks that are selected from the four external clock pins. There is one universal clock signal. The clock input signals CT[4:7] (Local Control Terms) can be individually configured as either a PRODUCT term or SUM term equation created from the 40 signals available inside the function block.

There are two muxed paths to the ZIA. One mux selects from either the output of the VFM or the output of the register. The other mux selects from the output of the register or from the I/O pad of the macrocell. When the I/O pin is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feed back the logic implemented in the macrocell. When an I/O pin is used as an input, the output buffer is 3-stated and the input signal is fed into the ZIA via the I/O feedback path. The logic imple-

mented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path.

If a macrocell pin is configured as a registered input, there is a direct path to the register to provide a fast input setup time. If the macrocell is configured as a latch, the register clock input functions as the latch enable, with the latch transparent when this signal is High. The hardwired clock enable is non-functional when the macrocell is configured as a latch.



Note: Global CLK signals come from pins.

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Figure 5: **XPLA3 Macrocell Architecture**

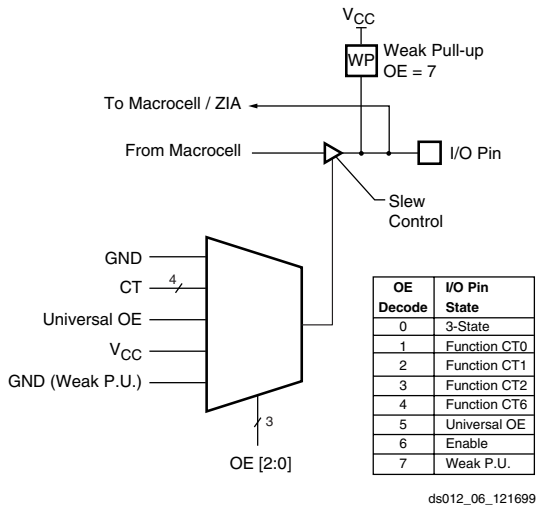
I/O Cell

The OE (Output Enable) multiplexer has eight possible modes (Figure 6). When the I/O Cell is configured as an input (or 3-stated output), a half latch feature exists. This half latch pulls the input High (through a weak pull-up) if the input should float and cross the threshold. This protects the input from staying in the linear region and causing an increased amount of power consumption. This same weak pull-up can be enabled in software such that it is always on when the I/O Cell is configured as an input. This weak pull up is automatically turned on when a pin is unused by the design.

The I/O Cell is 5V tolerant when the device is powered. Each output has independent slew rate control (fast or slow) which assists in reducing EMI emissions.

See individual device data sheets for 3.3V PCI electrical specification compatibility.

Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the weak pull-up resistors will be turned on. It is recommended that any unused I/O pins on the CoolRunner XPLA3 family of CPLDs be left unconnected. Dedicated input pins (CLKx/INx) do not have on-chip weak pull-up resistors; therefore unused dedicated input pins must have external termination. As with all CMOS devices, do not allow inputs to float.



OE Decode	I/O Pin State
0	3-State
1	Function CT0
2	Function CT1
3	Function CT2
4	Function CT6
5	Universal OE
6	Enable
7	Weak P.U.

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Figure 6: **I/O Cell**