What are Field Programmable Gate Arrays (FPGAs)?

- Like PLDs programmable at users site
- Two dimensional array of customizable logic block placed in an interconnect array
- Employs logic and interconnect structure capable of implementing multi-level logic
- Scalable in proportion with logic removing many of the size limitations of PLD derived two level architecture

Why Field Programmable Gate Arrays (FPGAs)?

- Fast-turnaround prototype implementation
- Supported by CAD/EDA tools
- High density
- High speed
- Programmable and versatile
- Flexible
- Reusable
- Large amounts of logic gates, registers, RAM and routing resources
- Quick time-to-market
- SRAM FPGA provide the benefits of custom CMOS

Field Programmable Gate Arrays (FPGAs)

FPGA Developers

ALTERA, Lattice Semiconductor Corporation, Lucent Technologies Bell Labs Innovations, ATMEL, MICROCHIP, Microsemi, Texas Instruments, CYPRESS, QuickLogic, XILINX ALL PROGRAMMABLE, ALDEC THE DESIGN VERIFICATION COMPANY

CPLDs vs FPGAs

- CPLDs, with their PAL-derived, easy-to-understand AND-OR structure, offer a single-chip solution with fast pin-to-pin delays, even for wide input functions
- The limited complexity (< 500 flip-flops) means that most CPLDs are used for "glue logic" functions
- FPGAs offer much higher complexity, up to 150,000 flip-flops, and their idle power consumption is reasonably low, although it is sharply increasing in the newest families
- FPGAs offer more logic flexibility and more sophisticated system features than CPLDs: clock management, on-chip RAM, DSP functions, (multipliers), and even on-chip microprocessors and Multi-Gigabit Transceivers.
- Use CPLDs for small designs
- Use FPGAs for larger and more complex designs

ASIC Vs FPGA

- ASIC
  - Low cost for large volume
  - Area and power efficient
  - High frequencies can be achieved
  - Huge testing cost in term of time and money
- FPGA
  - Low development cost solution
  - Larger area, power and speed
  - Less design and testing time
  - Short time to market

Applications of FPGAs

- For design prototyping
- For emulation
- As hardware accelerator
- In place of ASIC
  - Less time to market
- Complete System on Chip (SoC) solution

Programming technology

- Anti-fuse based
  - All the contacts or open initially
  - Programming converts selected locations as conducting
  - One time programmable (OTP)
- SRAM based
- EEROM or Flash based
- Tradeoffs
  - Anti-fuse is less area, less power consuming
  - EERAM takes more time for programming
  - SRAM is technology leaders

Major FPGA Vendors

- SRAM-based FPGAs
  - **Xilinx Inc.**
  - **Altera Corp.**
  - Atmel
  - Lattice Semiconductor
- Flash & antifuse FPGAs
  - Actel Corp.
  - Quick Logic Corp.
- Xilinx + Altera $\rightarrow$ Share over $\approx 60\%$ of the market

Structure of FPGA